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Renesas Electronics Corporation

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# H8/300H SLP Series

## Address Break

### Introduction

An LED connected to P93 is turned on, and the LED is turned off by means of address break interrupt processing.

### Target Device

H8/38076R

### Contents

1. Specifications ..... 2
2. Functions Used ..... 2
3. Principles of Operation ..... 4
4. Description of Software ..... 5
5. Flowcharts ..... 8

# 1. Specifications

1. The LED is turned on in the initial state.
2. Turning on a switch connected to port B0 passes control to a processing routine in which an address break is set.
3. Address break interrupt processing is initiated, and the LED is turned off.
4. The LED is connected to the P93 output pin of port 9.
5. A sample connection diagram is shown in figure 1.

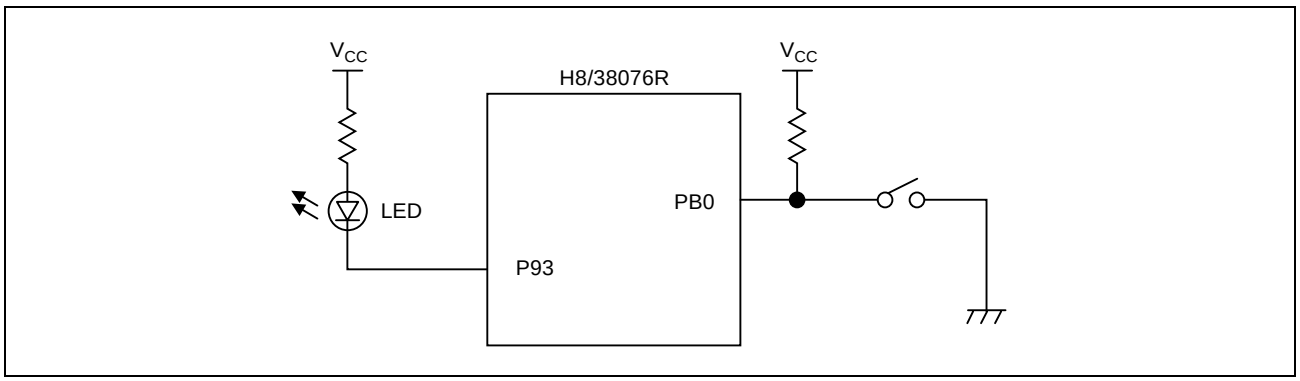



**Figure 1 Example of Connections for This Sample Task**

# 2. Functions Used

## 2.1 Functions

In this sample task, address break interrupt processing is performed. A block diagram of the address break function is shown in figure 2.

- Address break control register 2 (ABRKCR2)

  Sets address break conditions. In this sample task, an instruction execution cycle is set as a break condition, and the condition is established after instruction execution indicated by the address set in break address register 2.
- Address break status register 2 (ABRKSR2)

  Comprises an address break interrupt request flag and associated enable bit.
- Break address register 2 (BAR2H, BAR2L)

  Used to set an address for generating an address break interrupt as 16 bits. When an instruction execution cycle is set as an address break condition, the address of the first byte of the instruction is set.
- Break data register 2 (BDR2H, BDR2L)

  A 16-bit register used to set data for generating an address break interrupt. BDR2H is compared with the upper 8 bits of the data bus, and BDR2L with the lower 8 bits. In the case of byte access, the upper 8 data bus bits are used for data transfer for both even and odd addresses, and therefore a BDR2H setting should be made. Not used in this sample task.

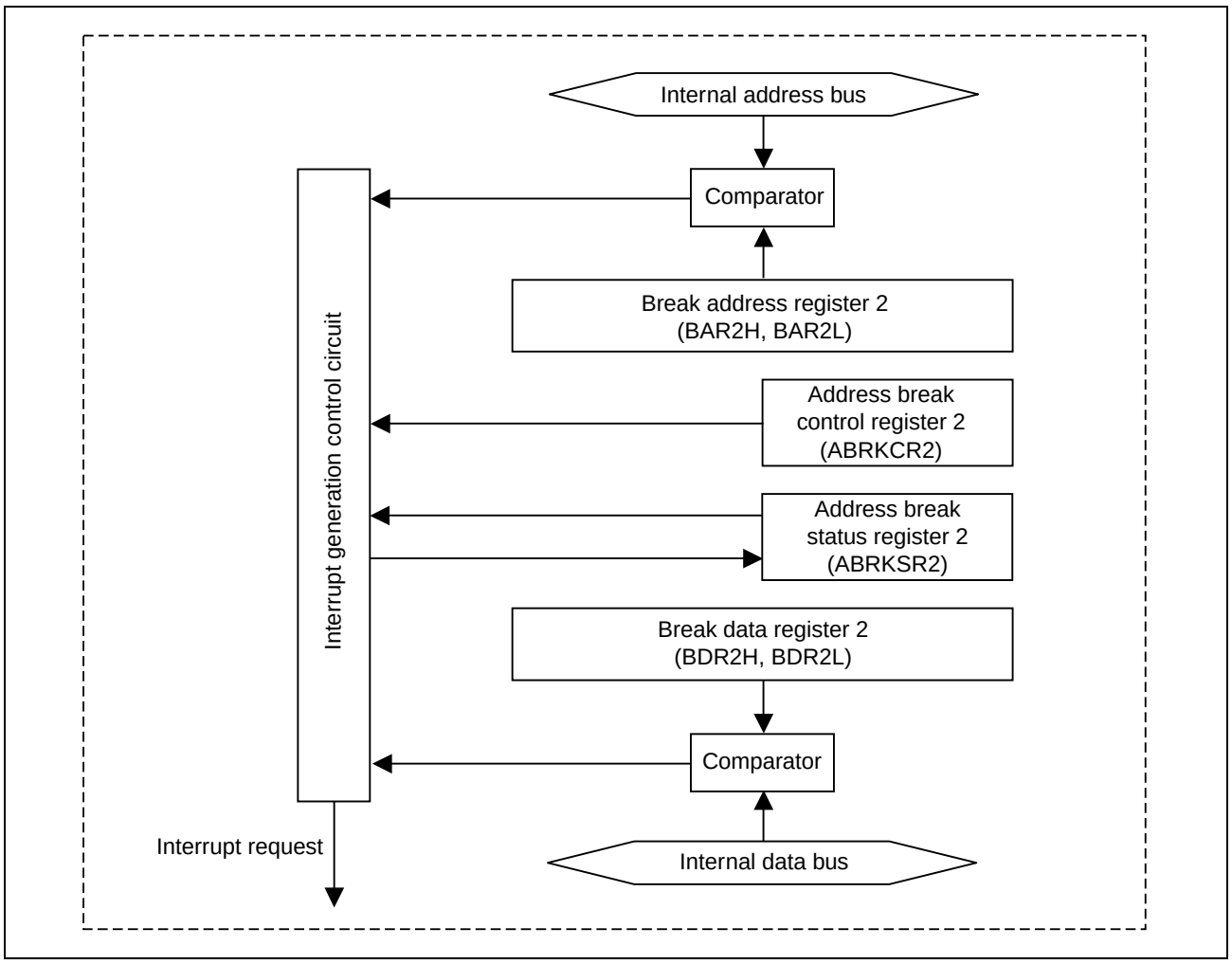



**Figure 2 Block Diagram of Address Break Function**

## 2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, an illuminated LED connected to P93 is turned off by means of the address break function.

**Table 1 Assignment of Functions**

| Elements | Description |
|---|---|
| ABRKCR2 | Sets instruction execution cycle as address break condition<br>RTE interrupt enabled<br>Condition satisfied after execution of instruction indicated by address set in BAR2 |
| BAR2<br>(BAR2H, BAR2L) | Used to set address for generating address break interrupt as 16 bits<br>Upper address is indicated by BAR2H, and lower address BAR2L |
| ABRKSR2 | Comprises flag (ABIF2) indicating satisfaction of address break condition, and enable bit (ABIE2) for enabling/disabling that interrupt |

## 3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, an illuminated LED connected to P93 is turned off by means of the address break function.

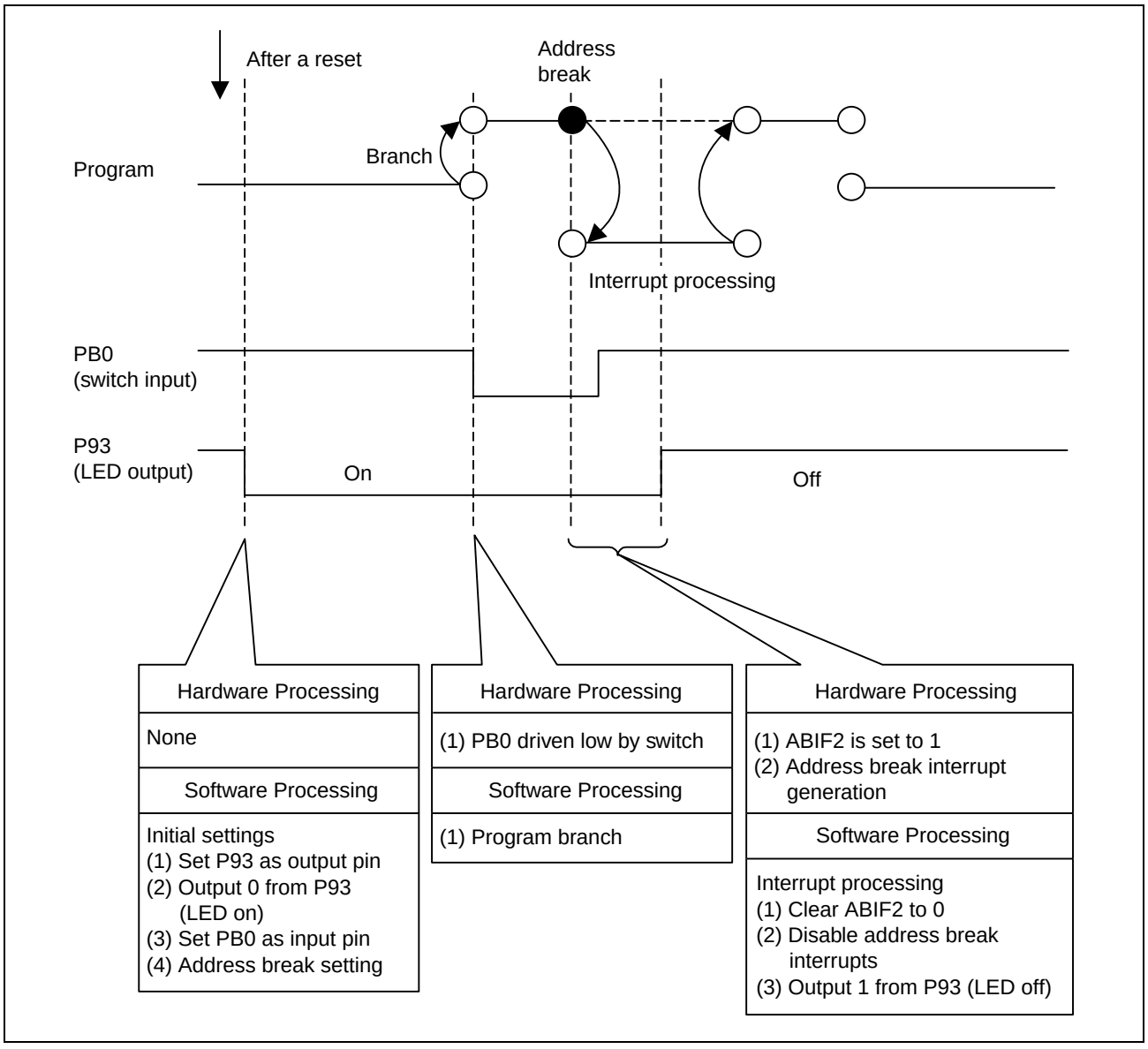



**Figure 3 Principles of Operation**

# 4. Description of Software

## 4.1 Modules

Table 2 shows the modules used in this sample task.

**Table 2 Modules**

| Function Name | Description |
|---|---|
| main | Sets the address break, set P93 as output pin, and outputs 0 (LED on) |
| dummy | Dummy routine (break address setting) |
| int_abrk | Address break interrupt processing, 1 output from P93 (LED off) |

## 4.2 Arguments

No arguments are used in this sample task.

## 4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- ABRKCR2 Address break control register 2 Address: H'F096

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 7 | RTINTE2 | 1 | R/W | RTE interrupt enable<br>1: Interrupt immediately after RTE instruction execution is not masked |
| 6 | CSEL21 | 0 | R/W | Condition select 1, 0 |
| 5 | CSEL20 | 0 | R/W | Set the address break condition.<br>CSEL21 = 0, CSEL20 = 0: Instruction execution cycle (data not compared) |
| 4 | ACMP22 | 0 | R/W | Address compare 2 to 0 |
| 3 | ACMP21 | 0 | R/W | Set condition for comparison between BAR2 and internal address bus. |
| 2 | ACMP20 | 0 | R/W | ACMP22 = 0, ACMP21 = 0, ACMP20 = 0: 16-bit comparison |
| 1 | DCMP21 | 0 | R/W | Data compare 1, 0 |
| 0 | DCMP20 | 0 | R/W | Set condition for comparison between BDR2 and internal data bus.<br>DCMP21 = 0, DCMP20 = 0: Data is not compared |

- ABRKSR2 Address break status register 2 Address: H'F097

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 7 | ABIF2 | 0 | R/W | Address break interrupt flag<br>[Setting condition]<br>When condition set in ABRKCR2 is satisfied<br>[Clearing condition]<br>When 0 is written to ABIF2 after reading 1 from ABIF2 |
| 6 | ABIE2 | 1 | R/W | Address break interrupt enable<br>When this bit is set to 1, address break interrupt requests are enabled. |

- BAR2 Break address register 2 Address: H'F098

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 15 | Bit15 | — | R/W | Break address register 2<br>Used to set address for generating address break interrupt as 16 bits. When an instruction execution cycle is set as an address break condition, the address of the first byte of the instruction is set. |
| 14 | Bit14 | — | R/W | |
| 13 | Bit13 | — | R/W | |
| 12 | Bit12 | — | R/W | |
| 11 | Bit11 | — | R/W | |
| 10 | Bit10 | — | R/W | |
| 9 | Bit9 | — | R/W | |
| 8 | Bit8 | — | R/W | |
| 7 | Bit7 | — | R/W | |
| 6 | Bit6 | — | R/W | |
| 5 | Bit5 | — | R/W | |
| 4 | Bit4 | — | R/W | |
| 3 | Bit3 | — | R/W | |
| 2 | Bit2 | — | R/W | |
| 1 | Bit1 | — | R/W | |
| 0 | Bit0 | — | R/W | |

- PDR9 Port data register 9 Address: H'FFDC

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 3 | P93 | 0 | R/W | P93 data register<br>Register that stores P93 data. If P93 is read while PCR93 bit is set to 1, the value stored in P93 is read, regardless of the actual pin state. If P93 is read while PCR93 bit is cleared to 0, the pin state are read. |

- PDRB Port data register B Address: H'FFDE

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 0 | PB0 | Undefined | R | PB data register<br>Register that stores PB0 data. When PB0 is read the state of PB0 is always returned. |

- PCR9 Port control register 9 Address: H'FFEC

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 3 | PCR93 | 1 | W | P93 control register<br>Controls P93 input/output. P93 is an output pin when PCR93 is set to 1, and an input pin when PCR93 is cleared to 0. PCR9 is a write-only register, and will always return a value of 1 if read. |

## 4.4 Constants Used

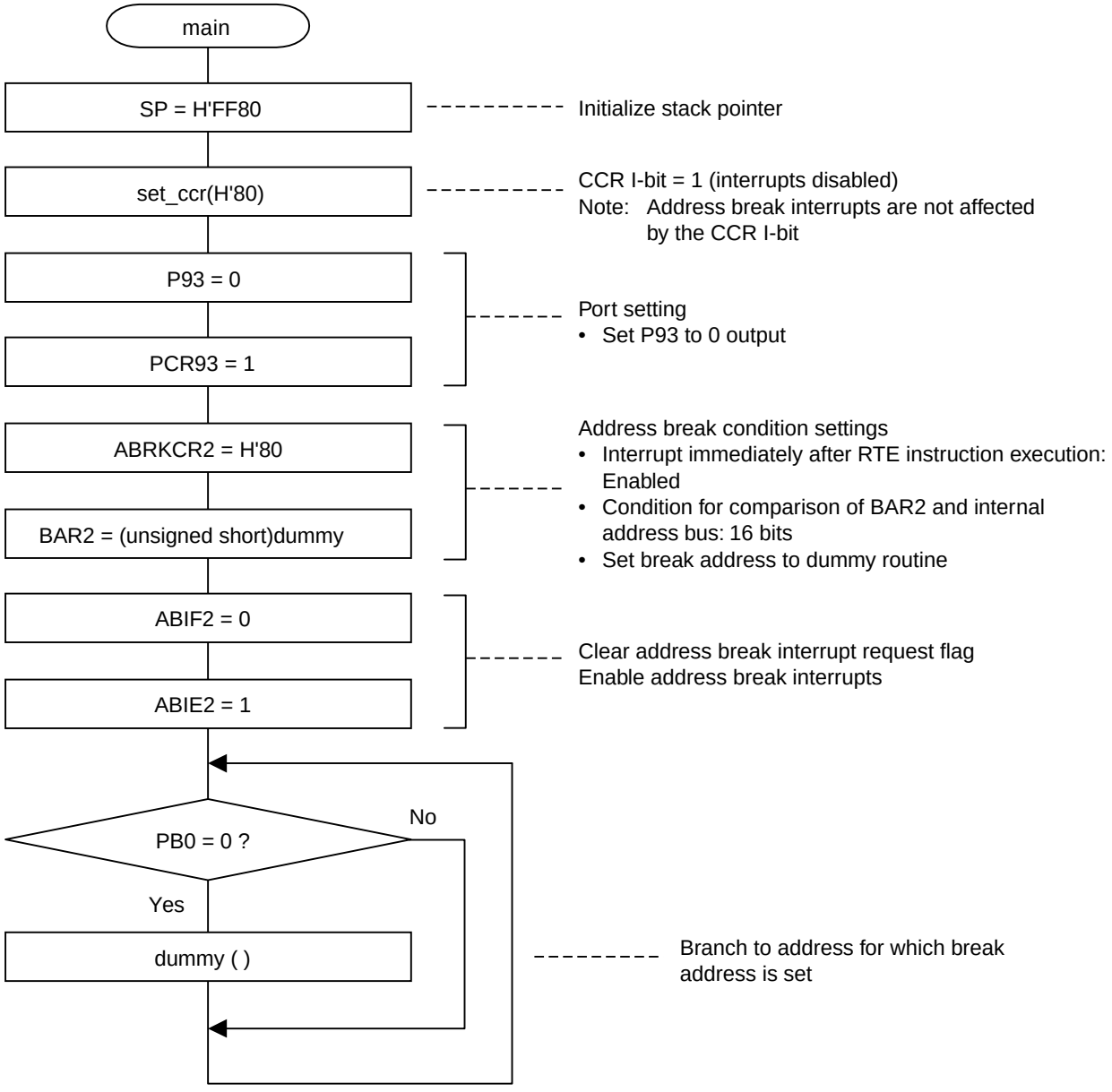
No constants are used in this sample task.

## 4.5 RAM Usage

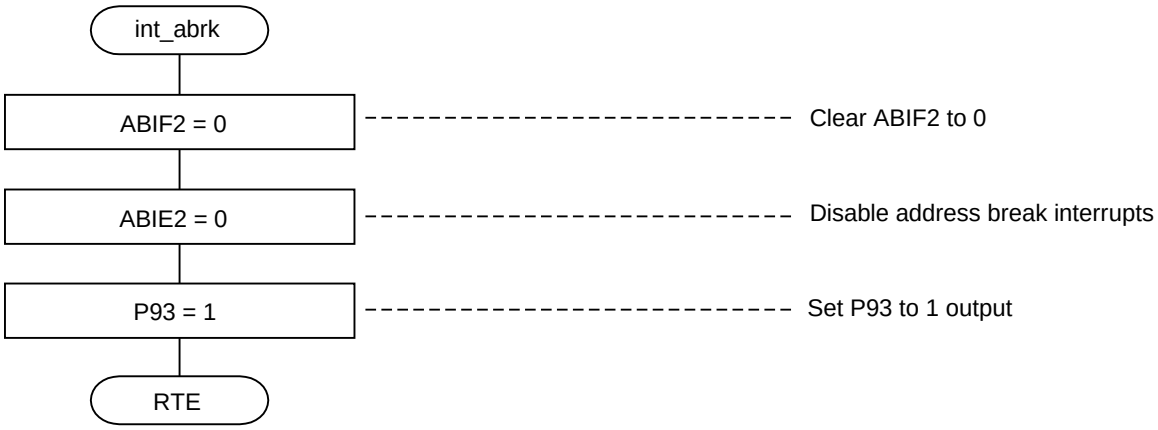
No RAM is used in this sample task.

# 5. Flowcharts

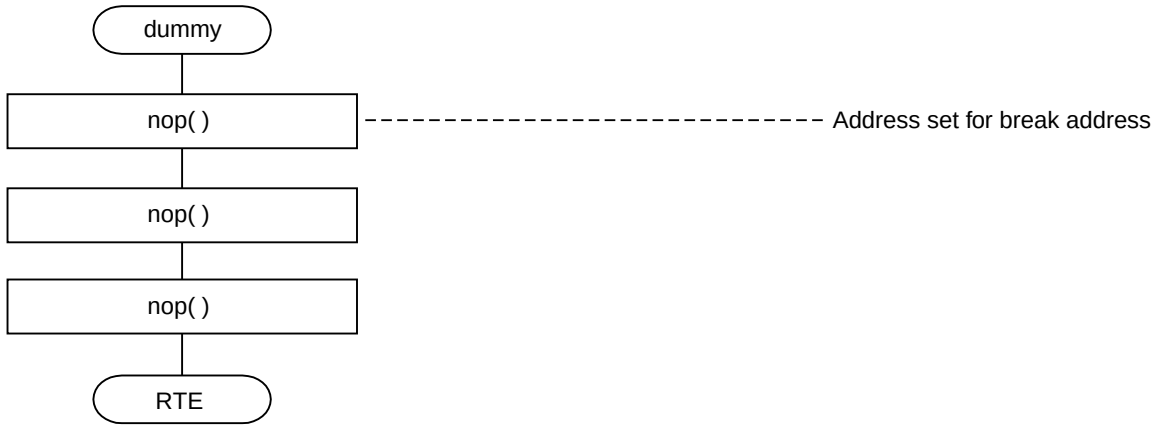
## 5.1 main



## 5.2 int_abrk




## 5.3 dummy




- Link Address Specifications

| Section Name | Address |
|---|---|
| CV1 | H'0000 |
| CV2 | H'000A |
| P | H'0100 |

## Revision Record

| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| 1.00 | Sep.16.04 | — | First edition issued |
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