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H8/300H SLP Series

3-Phase PWM Output

Introduction

The PWM mode 2 function of the 16-bit timer pulse unit (TPU) is used to output 3-phase PWM waveforms.

Target Device

H8/38076R

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2. Functions Used 3
3. Principles of Operation 7
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1. Specifications

- The PWM mode 2 function of the 16-bit timer pulse unit (TPU) is used to output 3-phase PWM waveforms from the TGRA_1 PWM output pin (TIOCA1), TGRB_1 PWM output pin (TIOCB1), and TGRA_2 PWM output pin (TIOCA2).
- TPU channels 1 and 2 are set to synchronous operation and PWM mode 2, synchronous clearing is set as the channel 1 counter clearing source, and TGRB_2 compare match as the channel 2 counter clearing source.
- For channel 1 and 2 TCNT, synchronous presetting is performed and synchronous clearing is performed by a TGRB_1 compare match, the data set in TGRB_2 is the period, and the data set in TGRA_1, TGRB_1, and TGRA_2 are the duty cycles.
- The 3-phase PWM waveforms are set to a 16-ms period and duty cycles of 75% for TIOCA1 pin output, 50% for TIOCB1 pin output, and 25% for TIOCA2 pin output.
- An example of 3-phase PWM output by means of the PWM mode 2 function is shown in figure 1.

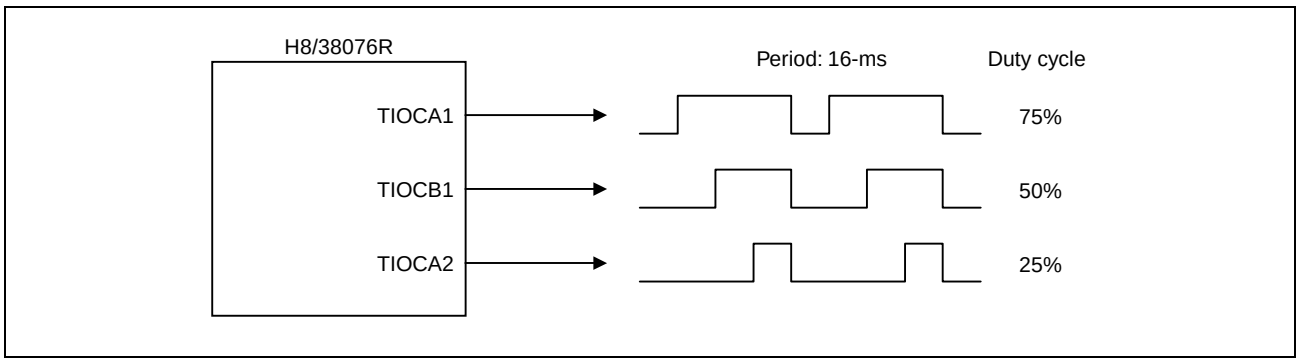


Figure 1 Example of 3-Phase PWM Output Using PWM Mode 2 Function

2. Functions Used

2.1 PWM Mode 2 Function

In this sample task, the PWM mode 2 function of the TPU is used to output 3-phase PWM waveforms from the TGRA_1 PWM output pin (TIOCA1), TGRB_1 PWM output pin (TIOCB1), and TGRA_2 PWM output pin (TIOCA2). A block diagram of the PWM mode 2 function of the TPU is shown in figure 2. The block diagram of the PWM mode 2 function of the TPU is explained below.

- System clock (ϕ)

  10-MHz clock used as the reference clock for operating the CPU and peripheral function modules.
- Timer control register_1 (TCR_1), timer control register_2 (TCR_2)

  These registers select timer counter_1 (TCNT_1), timer counter_2 (TCNT_2) counter clearing source, input clock edge, and clock source.
- Timer mode register_1 (TMDR_1), timer mode register_2 (TMDR_2)

  These registers set the operating modes of channels 1 and 2.
- Timer I/O control register_1 (TIOR_1), timer I/O control register_2 (TIOR_2)

  These register control timer general register A_1 (TGRA_1), timer general register B_1 (TGRB_1), timer general register A_2 (TGRA_2), and timer general register B_2 (TGRB_2).
- Timer counter_1 (TCNT_1), timer counter_2 (TCNT_2)

  16-bit readable/writable counters that count using the rising edge of internal clock ϕ/4
- Timer general register A_1 (TGRA_1)

  A 16-bit readable/writable output compare register that is used to set the duty cycle of the PWM waveform output from the TIOCA1 pin
- Timer general register B_1 (TGRB_1)

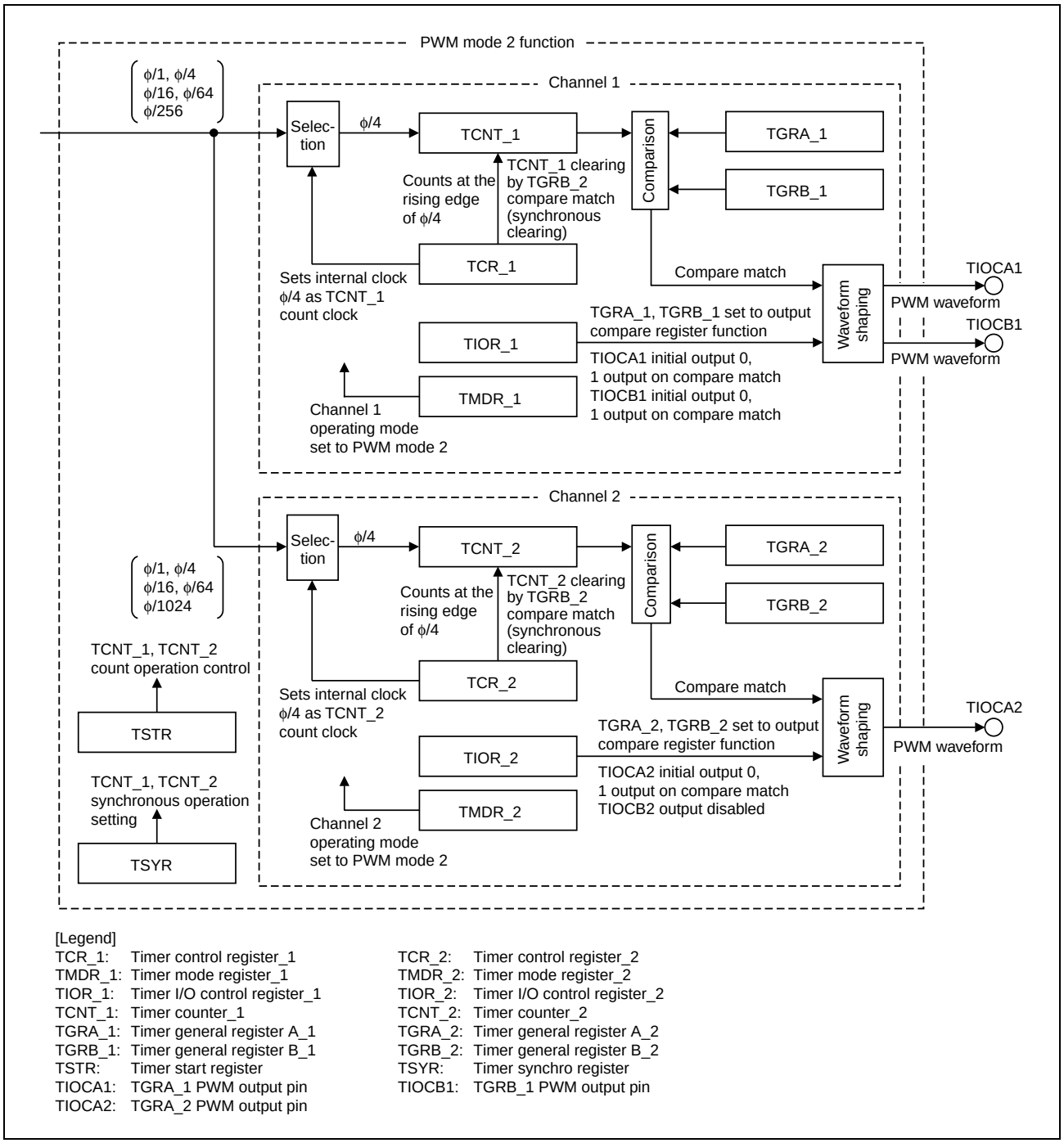
  A 16-bit readable/writable output compare register that is used to set the duty cycle of the PWM waveform output from the TIOCB1 pin
- Timer general register A_2 (TGRA_2)

  A 16-bit readable/writable output compare register that is used to set the phase difference of the PWM waveform output from the TIOCA2 pin
- Timer general register B_2 (TGRB_2)

  A 16-bit readable/writable output compare register that is used to set the period of the PWM waveforms output from the TIOCA1, TIOCB1, and TIOCA2 pins
- Timer start register (TSTR)

  Controls operation/stopping of timer counter_1 (TCNT_1) and timer counter_2 (TCNT_2).
- Timer synchro register (TSYR)

  Selects independent operation or synchronous operation of timer counter_1 (TCNT_1) and timer counter_2 (TCNT_2).



[Legend]

TCR_1:	Timer control register_1	TCR_2:	Timer control register_2
TMDR_1:	Timer mode register_1	TMDR_2:	Timer mode register_2
TIOR_1:	Timer I/O control register_1	TIOR_2:	Timer I/O control register_2
TCNT_1:	Timer counter_1	TCNT_2:	Timer counter_2
TGRA_1:	Timer general register A_1	TGRA_2:	Timer general register A_2
TGRB_1:	Timer general register B_1	TGRB_2:	Timer general register B_2
TSTR:	Timer start register	TSYR:	Timer synchro register
TIOCA1:	TGRA_1 PWM output pin	TIOCB1:	TGRB_1 PWM output pin
TIOCA2:	TGRA_2 PWM output pin		

Figure 2 Block Diagram of PWM Mode 2 Function

- Sample settings for 3-phase PWM waveforms output from the TIOCA1 pin, TIOCB1 pin, and TIOCA2 pin are shown below.

  Period of PWM waveforms output from TIOCA1, TIOCB1, and TIOCA2 pins:

$$\text{3-phase PWM waveform period} = \frac{\text{TGRB\_2 set value} + 1}{\text{TCNT\_2 input clock}} = \frac{\text{H'9C3F (39999)} + 1}{\text{10 MHz / 4}} = 16 \text{ ms}$$

  Duty cycle (low output width) of PWM waveforms output from TIOCA1, TIOCB1, and TIOCA2 pins:

$$\text{TIOCA1 output duty cycle} = \frac{\text{TGRA\_1 set value} + 1}{\text{TCNT\_1 input clock}} = \frac{\text{H'270F (9999)} + 1}{\text{10 MHz / 4}} = 4 \text{ ms}$$

$$\text{TIOCB1 output duty cycle} = \frac{\text{TGRB\_1 set value} + 1}{\text{TCNT\_1 input clock}} = \frac{\text{H'4E1F (19999)} + 1}{\text{10 MHz / 4}} = 8 \text{ ms}$$

$$\text{TIOCA2 output duty cycle} = \frac{\text{TGRA\_2 set value} + 1}{\text{TCNT\_2 input clock}} = \frac{\text{H'752F (29999)} + 1}{\text{10 MHz / 4}} = 12 \text{ ms}$$

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, 3-phase PWM output is performed by means of the PWM mode 2 function of the TPU.

Table 1 Assignment of Functions

Elements	Description
TCR_1	Sets counter clearing of other synchronous clearing/synchronous operation channel as TCNT_1 counter clearing source, rising edge as TCNT_1 input clock edge, and internal clock ϕ/4 as TCNT_1 counter clock
TCR_2	Sets TGRB_2 compare match as TCNT_2 counter clearing source, rising edge as TCNT_2 input clock edge, and internal clock ϕ/4 as TCNT_2 counter clock
TMDR_1	Sets PWM mode 2 as TPU channel 1 operating mode
TMDR_2	Sets PWM mode 2 as TPU channel 2 operating mode
TIOR_1	Sets output compare register as TGRA_1 function, initial output 0 and 1 output on compare match for TIOCA1 pin function. Sets output compare register as TGRB_1 function, initial output 0 and 1 output on compare match for TIOCB1 pin function
TIOR_2	Sets output compare register as TGRA_2 function, initial output 0 and 1 output on compare match for TIOCA2 pin function. Sets output compare register as TGRB_2 function, initial output 0 and 1 output on compare match for TIOCB2 pin function
TCNT_1	16-bit timer counter incremented by rising edge of internal clock ϕ/4
TCNT_2	16-bit timer counter incremented by rising edge of internal clock ϕ/4
TGRA_1	16-bit output compare register, used to set duty cycle of PWM waveform output from TIOCA1 pin
TGRB_1	16-bit output compare register, used to set duty cycle of PWM waveform output from TIOCB1 pin
TGRA_2	16-bit output compare register, used to set duty cycle of PWM waveform output from TIOCA2 pin
TGRB_2	16-bit output compare register, used to set cycle of PWM waveforms output from TIOCA1, TIOCB1, and TIOCA2 pins
TSTR	Controls operation/stopping of TCNT_1 and TCNT_2 count
TSYR	Sets synchronous operation of channels 1 and 2
TIOCA1	TGRA_1 PWM waveform output pin
TIOCB1	TGRB_1 PWM waveform output pin
TIOCA2	TGRA_2 PWM waveform output pin

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, PWM output is performed by means of the TPU synchronous operation function.

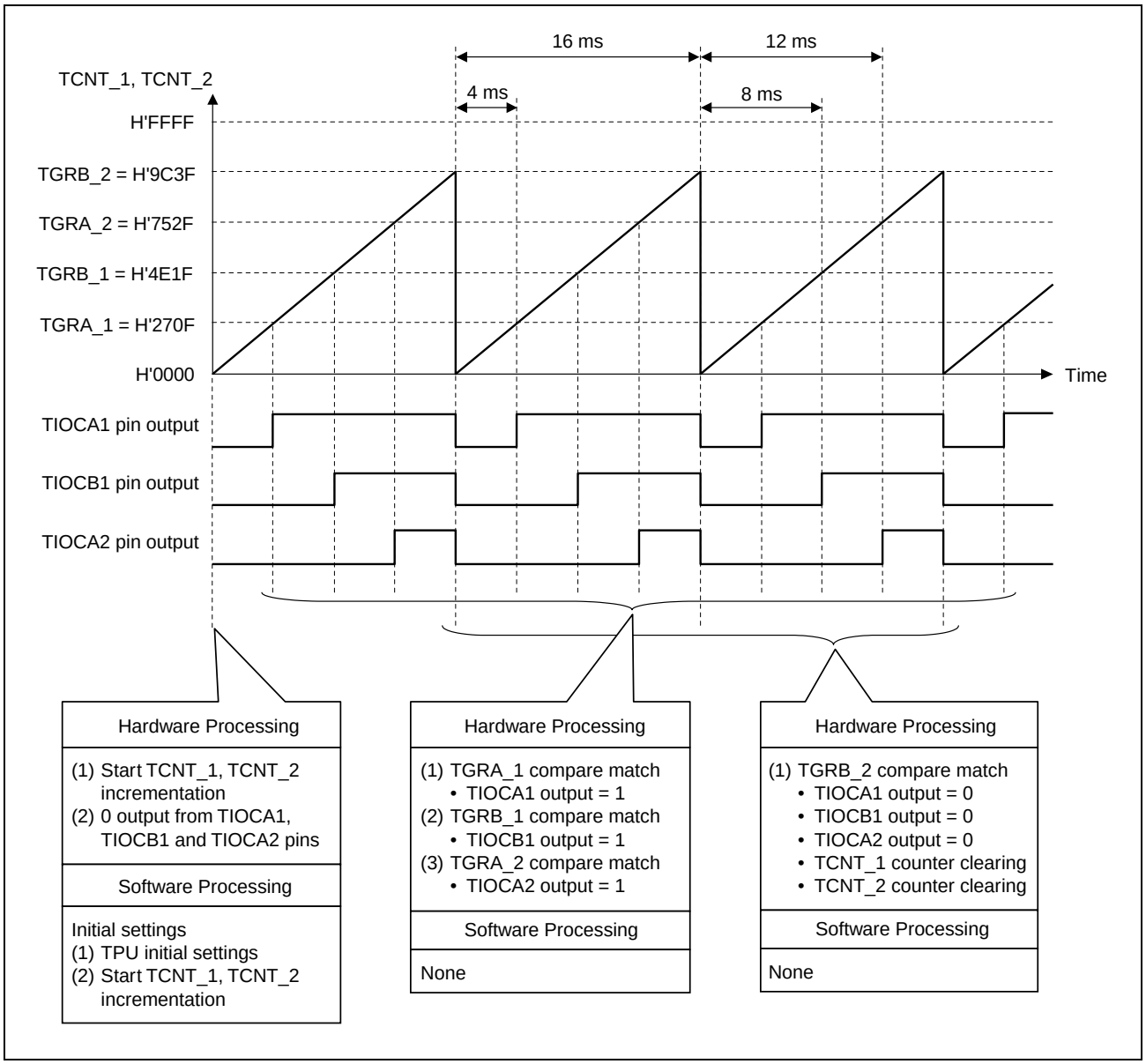


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	TPU initial settings, TCNT_1 and TCNT_2 count operation start

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- TSTR Timer start register Address: H'F030

Bit	Bit Name	Set Value	R/W	Description
2	CST2	1	R/W	Counter start 2 Selects TCNT_2 operation or stopping. CST2 = 1: TCNT_2 performs count operation
1	CST1	1	R/W	Counter start 1 Selects TCNT_1 operation or stopping. CST1 = 1: TCNT_1 performs count operation

- TSYR Timer synchro register Address: H'F031

Bit	Bit Name	Set Value	R/W	Description
2	SYNC2	1	R/W	Timer synchronization 2 Selects independent operation from, or synchronous operation with, the other channel. SYNC2 = 1: TCNT_2 performs synchronous operation (TCNT synchronous presetting/synchronous clearing possible)
1	CYNC1	1	R/W	Timer synchronization 1 Selects independent operation from, or synchronous operation with, the other channel. SYNC1 = 1: TCNT_1 performs synchronous operation (TCNT synchronous presetting/synchronous clearing possible)

- TCR_1 Timer control register_1 Address: H'F040

Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	1	R/W	Counter clear 1, 0
5	CCLR0	1	R/W	Select the TCNT_1 counter clearing source. CCLR1 = 1, CCLR0 = 1: TCNT_1 cleared by counter clearing of other synchronous clearing/synchronous operation channel
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_1 input clock edge. CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	0	R/W	Timer prescaler 2, 1, 0
1	TPSC1	0	R/W	Select the TCNT_1 clock source.
0	TPSC0	1	R/W	TPSC2 = 0, TPSC1 = 0, TPSC0 = 1: Counts on internal clock ϕ/4

- TMDR_1 Timer mode register_1 Address: H'F041

Bit	Bit Name	Set Value	R/W	Description
1	MD1	1	R/W	Mode 1, 0
0	MD0	1	R/W	Select the TPU_1 operating mode. MD1 = 1, MD0 = 1: TPU_1 set to PWM mode 2

- TIOR_1 Timer I/O control register_1 Address: H'F042

Bit	Bit Name	Set Value	R/W	Description
7	IOB3	0	R/W	I/O control B3 to B0
6	IOB2	0	R/W	Select the function of TGRB_1.
5	IOB1	1	R/W	IOB3 = 0, IOB2 = 0, IOB1 = 1, IOB0 = 0: TGRB_1 function is output compare register, TIOCB1 pin function is 1 output on compare match with initial output = 0
4	IOB0	0	R/W	
3	IOA3	0	R/W	I/O control B3 to B0
2	IOA2	0	R/W	Select the function of TGRA_1.
1	IOA1	1	R/W	IOA3 = 0, IOA2 = 0, IOA1 = 1, IOA0 = 0: TGRA_1 function is output compare register, TIOCA1 pin function is 1 output on compare match with initial output = 0
0	IOA0	0	R/W	

- TCNT_1 Timer counter_1 Address: H'F046

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer counter_1
14	Bit 14	0	R/W	16-bit readable/writable counter. TCNT_1 is initialized to H'0000 at a reset. TCNT_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- TGRA_1 Timer general register A_1 Address: H'F048

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer general register A_1
14	Bit 14	0	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRA_1 is initialized to H'FFFF at a reset. TGRA_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	1	R/W	
12	Bit 12	0	R/W	
11	Bit 11	0	R/W	Note: Set value: H'270F
10	Bit 10	1	R/W	
9	Bit 9	1	R/W	
8	Bit 8	1	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	1	R/W	
2	Bit 2	1	R/W	
1	Bit 1	1	R/W	
0	Bit 0	1	R/W	

- TGRB_1 Timer general register B_1 Address: H'F04A

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer general register A_1
14	Bit 14	1	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRB_1 is initialized to H'FFFF at a reset. TGRB_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	
11	Bit 11	1	R/W	Note: Set value: H'4E1F
10	Bit 10	1	R/W	
9	Bit 9	1	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	1	R/W	
3	Bit 3	1	R/W	
2	Bit 2	1	R/W	
1	Bit 1	1	R/W	
0	Bit 0	1	R/W	

- TCR_2 Timer control register_2 Address: H'F050

Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	1	R/W	Counter clear 1, 0
5	CCLR0	0	R/W	Select the TCNT_2 counter clearing source. CCLR1 = 1, CCLR0 = 0: TCNT_2 cleared by TGRB_2 compare match of other synchronous clearing/synchronous operation channel
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_2 input clock edge. CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	0	R/W	Timer prescaler 2, 1, 0
1	TPSC1	0	R/W	Select the TCNT_2 clock source.
0	TPSC0	1	R/W	TPSC2 = 0, TPSC1 = 0, TPSC0 = 1: Counts on internal clock ϕ/4

- TMDR_2 Timer mode register_2 Address: H'F051

Bit	Bit Name	Set Value	R/W	Description
1	MD1	1	R/W	Mode 1, 0
0	MD0	1	R/W	Select the TPU_2 operating mode. MD1 = 1, MD0 = 1: TPU_2 set to PWM mode 2

- TIOR_2 Timer I/O control register_2 Address: H'F052

Bit	Bit Name	Set Value	R/W	Description
7	IOB3	0	R/W	I/O control B3 to B0
6	IOB2	0	R/W	Select the function of TGRB_2.
5	IOB1	0	R/W	IOB3 = 0, IOB2 = 0, IOB1 = 0, IOB0 = 0: TGRB_2 function is output compare register, TIOCB2 pin function is output disabled
4	IOB0	0	R/W	
3	IOA3	0	R/W	I/O control A3 to A0
2	IOA2	0	R/W	Select the function of TGRA_2.
1	IOA1	1	R/W	IOA3 = 0, IOA2 = 0, IOA1 = 1, IOA0 = 0: TGRA_2 function is output compare register, TIOCA2 pin function is 1 output on compare match with initial output = 0
0	IOA0	0	R/W	

- TCNT_2 Timer counter_2 Address: H'F056

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer counter_2
14	Bit 14	0	R/W	16-bit readable/writable counter. TCNT_2 is initialized to H'0000 at a reset. TCNT_2 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- TGRA_2 Timer general register A_2 Address: H'F058

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer general register A_2
14	Bit 14	1	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRA_2 is initialized to H'FFFF at a reset. TGRA_2 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	1	R/W	
12	Bit 12	1	R/W	
11	Bit 11	0	R/W	Note: Set value: H'752F
10	Bit 10	1	R/W	
9	Bit 9	0	R/W	
8	Bit 8	1	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	1	R/W	
4	Bit 4	0	R/W	
3	Bit 3	1	R/W	
2	Bit 2	1	R/W	
1	Bit 1	1	R/W	
0	Bit 0	1	R/W	

- TGRB_2 Timer general register B_2 Address: H'F05A

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	1	R/W	Timer general register B_2
14	Bit 14	0	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRB_2 is initialized to H'FFFF at a reset. TGRB_2 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	0	R/W	
12	Bit 12	1	R/W	
11	Bit 11	1	R/W	Note: Set value: H'9C3F
10	Bit 10	1	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	1	R/W	
4	Bit 4	1	R/W	
3	Bit 3	1	R/W	
2	Bit 2	1	R/W	
1	Bit 1	1	R/W	
0	Bit 0	1	R/W	

4.4 Constants Used

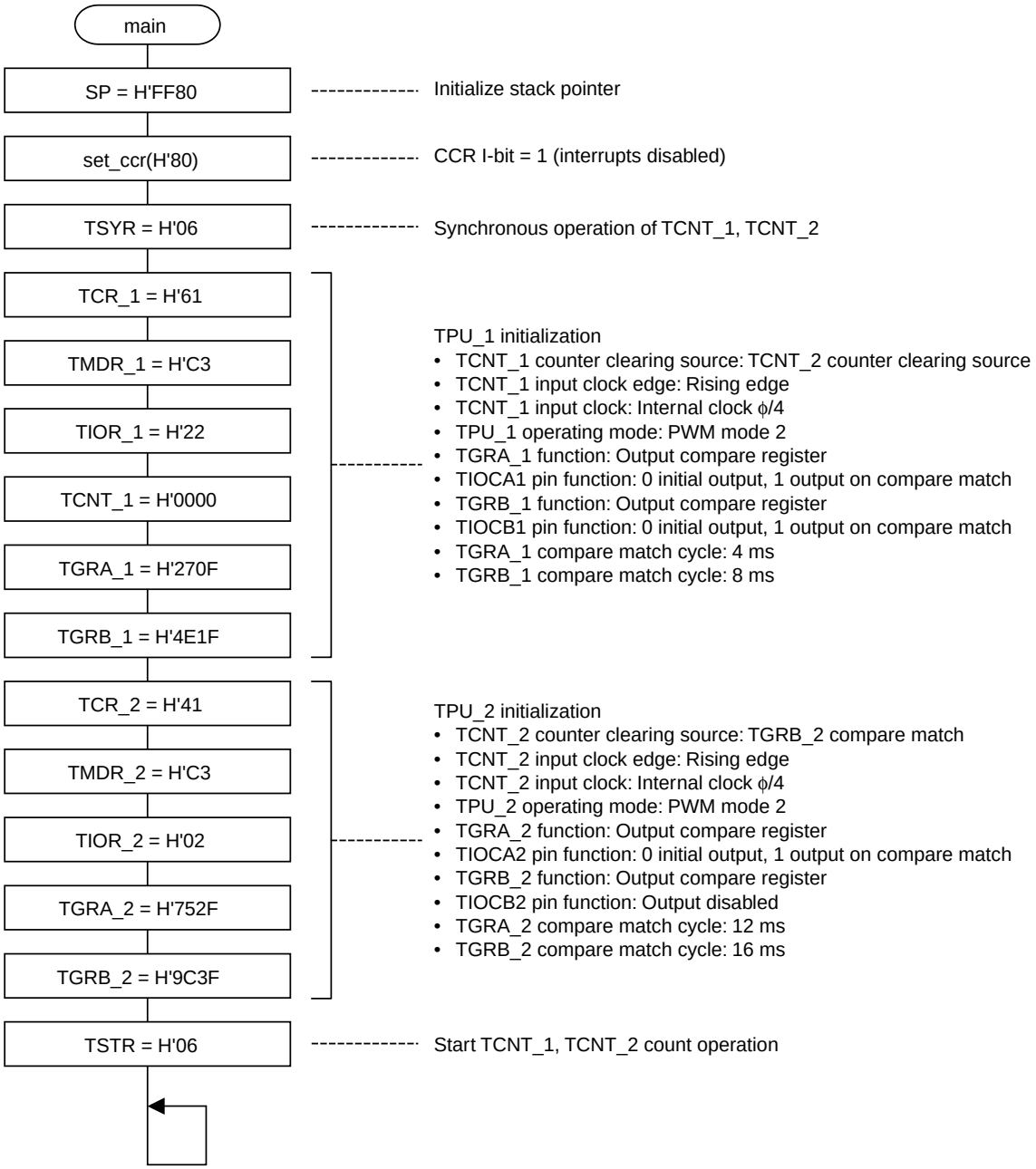
No constants are used in this sample task.

4.5 RAM Usage

No RAM is used in this sample task.

5. Flowcharts

5.1 main



- Link Address Specifications

Section Name	Address
CV1	H'0000
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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