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April 1st, 2010
Renesas Electronics Corporation

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H8SX Family

Generating 15-Phase PWM Output

Introduction

15 phases of PWM waveforms with desired duty cycles are output.

Target Device

H8SX/1663

Contents

1. Specifications

15-phase PWM waveforms with desired duty cycles are output as shown in figure 1.

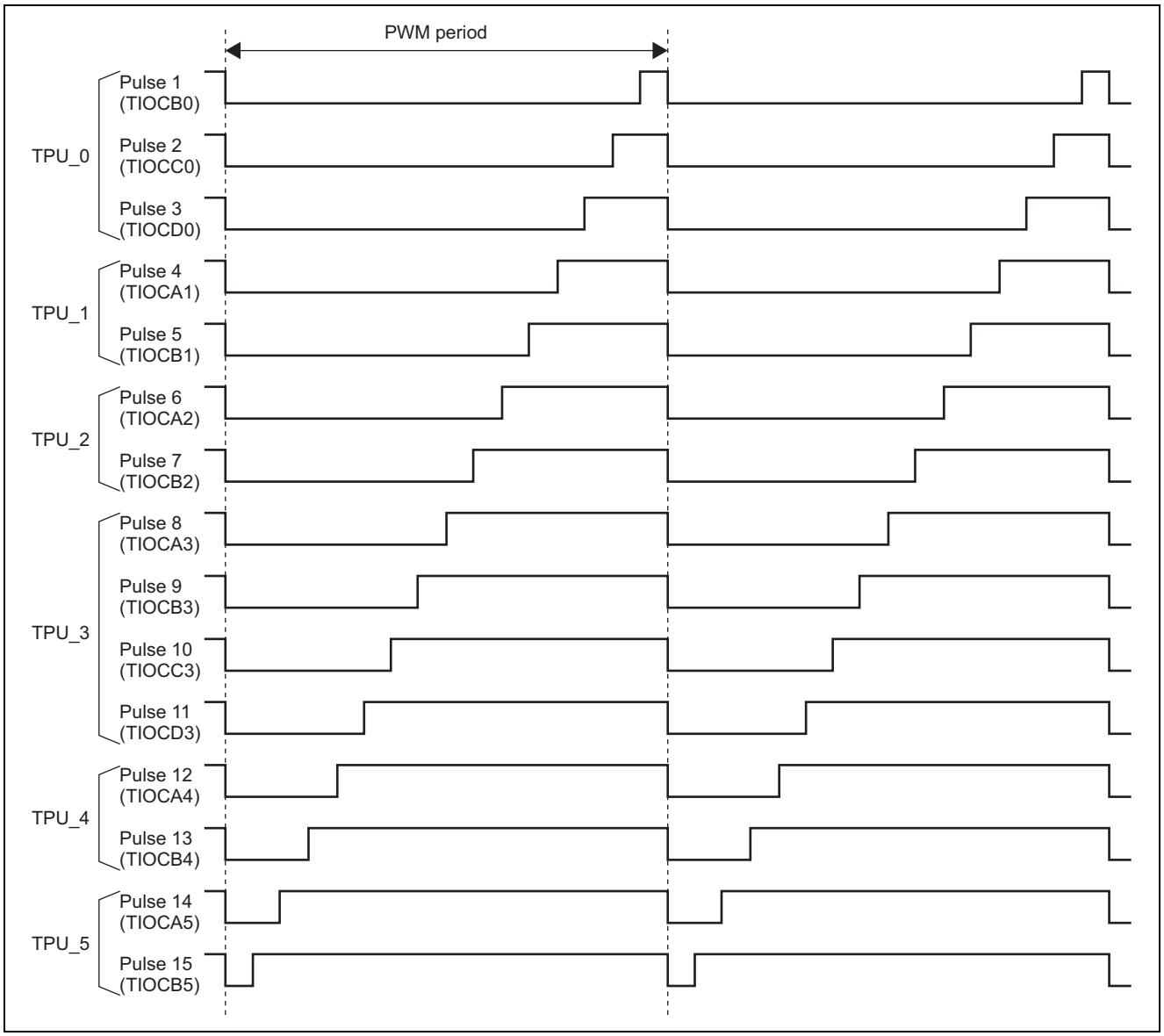


Figure 1 Example of 15-Phase PWM Output

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents	
Operating frequency	Input clock:	12 MHz
	System clock (Iϕ):	48 MHz
	Peripheral module clock (Pϕ):	24 MHz
	External bus clock (Bϕ):	48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)	
Development tool	High-performance Embedded Workshop Version 4.00.03	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 2 Section Setting

Address	Section Name	Description
H'001000	P	Program area

3. Description of Modules Used

3.1 Modules Used

15-phase PWM waveforms are output by TPU channels 0 to 5 in synchronous operation. Figure 2 shows a block diagram. The TPU registers are described below.

- Timer start register (TSTR)
  TSTR starts or stops TCNT operation for channels 0 to 5. Before setting the operating mode in TMDR or setting the TCNT counter clock in TCR, counting by TCNT should be stopped.

- Timer control register (TCR)
  TCR controls the TCNT on each channel. The TPU has a total of six TCR registers, one for each channel. TCR register settings should be made only while TCNT operation is stopped.

- Timer I/O control register (TIOR)
  TIOR controls timer general registers (TGR). The TPU has eight TIOR registers, two each for channels 0 and 3, and one each for channels 1, 2, 4, and 5. Care is required since TIOR is affected by the TMDR setting.
  The initial output specified by TIOR is applied while the counter is stopped (the CST bit in TSTR is cleared to 0). In PWM mode 2, TIOR specifies the output at the point when the counter is cleared to 0.
  When TIOR is set to specify TGRC or TGRD for buffer operation, the above setting becomes invalid and the TGR register operates as a buffer register.
  When TIOR is set to configure an input capture function, the DDR and ICR bits for the corresponding pin should be set to 0 and 1, respectively.

- Timer counter (TCNT)
  TCNT is a 16-bit readable/writable counter. The TPU has six TCNT counters, one for each channel. TCNT is initialized to H'0000 by a reset or in hardware standby mode. TCNT cannot be accessed in 8-bit units and must always be accessed in 16-bit units.

- Timer general register (TGR)
  TGR is a 16-bit readable/writable register that can be used as either an output-compare or input-capture register. The TPU has 16 general registers, four each for channels 0 and 3, and two each for channels 1, 2, 4, and 5. TGRC and TGRD for channels 0 and 3 can also be designated as buffer registers. TGR cannot be accessed in 8-bit units and must always be accessed in 16-bit units.

- Timer synchronous register (TSYR)
  TSYR selects independent operation or synchronous operation for the TCNT counters of channels 0 to 5.

- Timer mode register (TMDR)
  TMDR sets the operating mode for each channel. The TPU has six TMDR registers, one for each channel. TMDR register settings should be made only while TCNT operation is stopped.

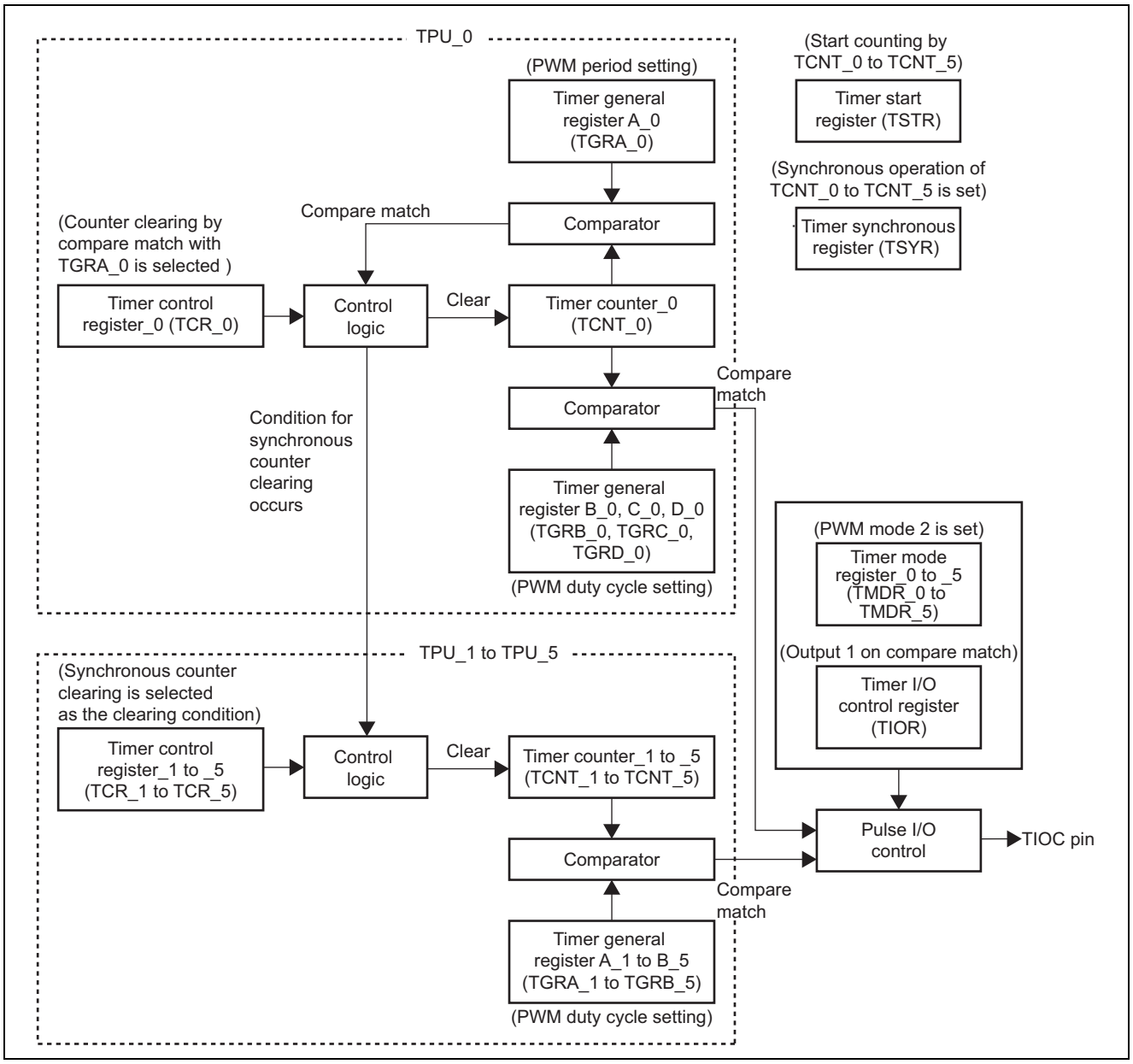


Figure 2 Block Diagram of 15-Phase PWM Output

3.2 PWM Mode 2

In PWM mode 2, PWM outputs are generated using one TGR as the period register and the other TGRs as duty cycle registers. The output is generated as specified in TIOR, driven by compare match. When the counter is cleared on compare match with the period register, each pin outputs the initial value specified by TIOR. If the settings of the period and duty cycle registers are identical, the output value does not change when a compare match occurs.

In PWM mode 2, generation of a maximum of 15 phases of PWM output is possible by through the use of synchronous operation.

4. Description of Operation

Figure 3 illustrates operation of 15-phase PWM output. The hardware processing and software processing of figure 3 are explained in table 3.

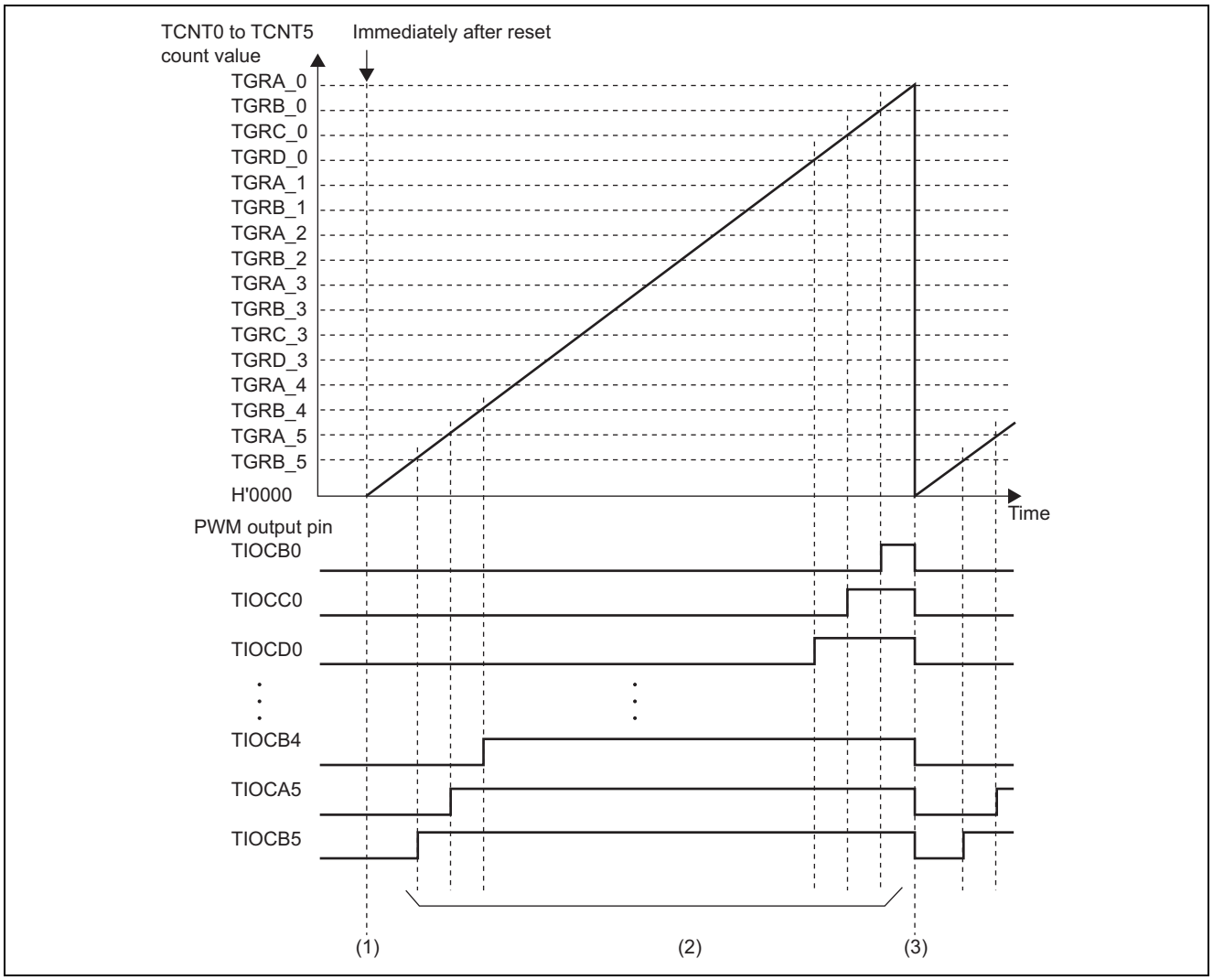


Figure 3 Operation of 15-Phase PWM Output

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings: (a) Select ϕ as the counter clock. (b) Select compare match with TGRA_0 as the condition for clearing TCNT_0. (c) Specify TGR as output compare registers, and set so that the initial value of TIOC pin output is 0 and the output value on compare match is 1. (d) Set the operating mode as PWM mode 2. (e) Set the pulse period in TGRA_0 and the duty cycle in the other TGR registers. Start counting operation.
(2)	(a) Output 1 from the TIOC pin on compare match with the corresponding TGR.	No processing
(3)	(a) Clear the counters (TCNT_0 to TCNT_5) on compare match with TGRA_0. (b) Output 0 from all TIOC pins.	No processing

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, cancels the module stop mode, and calls the main function.
main	Main routine Makes synchronous settings for TPU channels 0 to 5 and performs PWM output in PWM mode 2.

5.2 Vector Table

Table 5 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	main

5.3 Description of Functions

5.3.1 init Function

(1) Functional overview

Initialization routine which cancels the module stop mode, sets up the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	0	R/W	supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

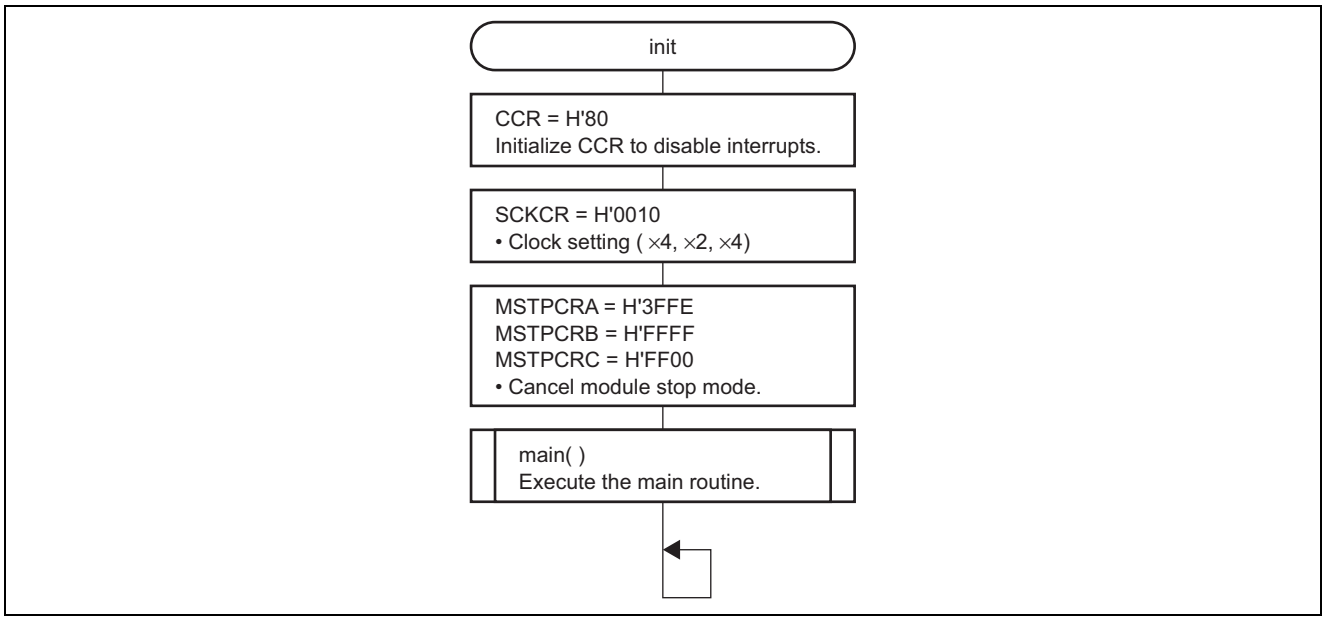
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart



5.3.2 main Function

(1) Functional overview

Main routine which makes settings for synchronous operation of TPU channels 0 to 5 and performs processing to produce PWM output in PWM mode 2.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Timer control register_0 (TCR_0) Address: H'FFFFC0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT_0 counter clearing condition.
5	CCLR0	1	R/W	001: TCNT_0 is cleared by TGRA_0 compare match/input capture
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting. 00: Falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT_0 counter clock.
0	TPSC0	0	R/W	000: Internal clock Pϕ/1

- Timer control register_1 (TCR_1) Address: H'FFFFD0
- Timer control register_2 (TCR_2) Address: H'FFFFE0
- Timer control register_3 (TCR_3) Address: H'FFFFF0
- Timer control register_4 (TCR_4) Address: H'FFFEE0
- Timer control register_5 (TCR_5) Address: H'FFFEF0

Bit	Bit Name	Setting	R/W	Function
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	1	R/W	These bits select the TCNT counter clearing condition.
5	CCLR0	1	R/W	011: TCNT is cleared by clearing of a counter on another channel configured for synchronous clearing or synchronous operation
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge for counting. 00: Falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock.
0	TPSC0	0	R/W	000: Internal clock Pϕ/1

- Timer mode register_0 (TMDR_0) Address: H'FFFFC1
- Timer mode register_1 (TMDR_1) Address: H'FFFFD1
- Timer mode register_2 (TMDR_2) Address: H'FFFFE1
- Timer mode register_3 (TMDR_3) Address: H'FFFFF1
- Timer mode register_4 (TMDR_4) Address: H'FFFEE1
- Timer mode register_5 (TMDR_5) Address: H'FFFEF1

Bit	Bit Name	Setting	R/W	Function
3	MD3	0	R/W	Modes 3 to 0
2	MD2	0	R/W	These bits set the timer operating mode.
1	MD1	1	R/W	0011: PWM mode 2
0	MD0	1	R/W	

- Timer I/O control register H_0 (TIORH_0) Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Function
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	These bits specify the function of TGRB_0.
5	IOB1	1	R/W	0010: TGRB_0 functions as an output compare register.
4	IOB0	0	R/W	In PWM mode 2, the TIOCB0 pin outputs 1 on compare match.
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the function of TGRA_0.
1	IOA1	0	R/W	0000: TGRA_0 functions as an output compare register.
0	IOA0	0	R/W	TIOCA0 pin output is disabled.

- Timer I/O control register_1 (TIOR_1) Address: H'FFFFD2
- Timer I/O control register_2 (TIOR_2) Address: H'FFFFE2
- Timer I/O control register H_3 (TIORH_3) Address: H'FFFFF2
- Timer I/O control register_4 (TIOR_4) Address: H'FFFEE2
- Timer I/O control register_5 (TIOR_5) Address: H'FFFEF2

Bit	Bit Name	Setting	R/W	Function
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	These bits specify the function of TGRB.
5	IOB1	1	R/W	0010: TGRB functions as an output compare register.
4	IOB0	0	R/W	In PWM mode 2, the TIOCB pin outputs 1 on compare match.
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the function of TGRA.
1	IOA1	1	R/W	0010: TGRA functions as an output compare register.
0	IOA0	0	R/W	In PWM mode 2, the TIOCA pin outputs 1 on compare match.

- Timer I/O control register L_0 (TIORL_0) Address: H'FFFFC3
- Timer I/O control register L_3 (TIORL_3) Address: H'FFFFF3

Bit	Bit Name	Setting	R/W	Function
7	IOD3	0	R/W	I/O Control D3 to D0
6	IOD2	0	R/W	These bits specify the function of TGRD.
5	IOD1	1	R/W	0010: TGRD functions as an output compare register.
4	IOD0	0	R/W	In PWM mode 2, the TIOCD pin outputs 1 on compare match.
3	IOC3	0	R/W	I/O Control C3 to C0
2	IOC2	0	R/W	These bits specify the function of TGRC.
1	IOC1	1	R/W	0010: TGRC functions as an output compare register.
0	IOC0	0	R/W	In PWM mode 2, the TIOCC pin outputs 1 on compare match.

- Timer general register A_0 (TGRA_0) Address: H'FFFFC8

  Function: Used as an output compare register. Sets the period of the PWM waveforms.
  Setting: H'00FF

- Timer general register B_0 (TGRB_0) Address: H'FFFFCA
- Timer general register C_0 (TGRC_0) Address: H'FFFFCC
- Timer general register D_0 (TGRD_0) Address: H'FFFFCE
- Timer general register A_1 (TGRA_1) Address: H'FFFFD8
- Timer general register B_1 (TGRB_1) Address: H'FFFFDA
- Timer general register A_2 (TGRA_2) Address: H'FFFFE8
- Timer general register B_2 (TGRB_2) Address: H'FFFFEA
- Timer general register A_3 (TGRA_3) Address: H'FFFFF8
- Timer general register B_3 (TGRB_3) Address: H'FFFFFA
- Timer general register C_3 (TGRC_3) Address: H'FFFFFC
- Timer general register D_3 (TGRD_3) Address: H'FFFFFE
- Timer general register A_4 (TGRA_4) Address: H'FFFEE8
- Timer general register B_4 (TGRB_4) Address: H'FFFEEA
- Timer general register A_5 (TGRA_5) Address: H'FFFEF8
- Timer general register B_5 (TGRB_5) Address: H'FFFEFA

  Function: Used as an output compare register. Sets the low-level width of the PWM waveforms.
  Settings: TGRB_0 = H'0EFF, TGRC_0 = H'0DFF, TGRD_0 = H'0CFF, TGRA_1 = H'0BFF, TGRB_1 = H'0AFF, TGRA_2 = H'09FF, TGRB_2 = H'08FF, TGRA_3 = H'07FF, TGRB_3 = H'06FF, TGRC_3 = H'05FF, TGRD_3 = H'04FF, TGRA_4 = H'03FF, TGRB_4 = H'02FF, TGRA_5 = H'01FF, TGRB_5 = H'00FF

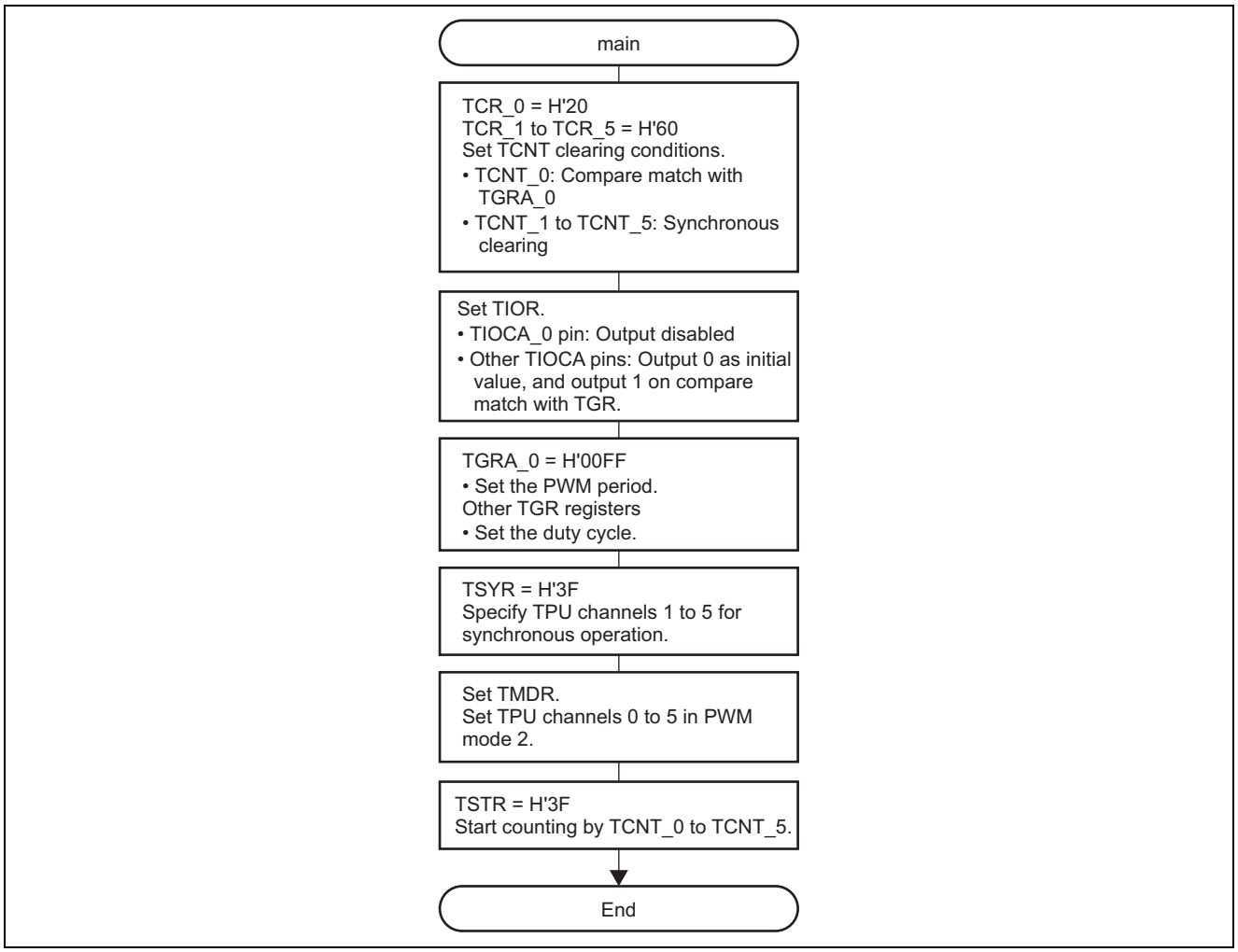
- Timer start register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Function
5	CST5	1	R/W	Counter Start 5 to 0
4	CST4	1	R/W	These bits start or stop the operation of the corresponding TCNT.
3	CST3	1	R/W	0: Stops counting by TCNT_5 to TCNT_0
2	CST2	1	R/W	1: Starts counting by TCNT_5 to TCNT_0
1	CST1	1	R/W	
0	CST0	1	R/W	

- Timer synchronous register (TSYR) Address: H'FFFFBD

Bit	Bit Name	Setting	R/W	Function
5	SYNC5	1	R/W	Timer Synchronization 5 to 0
4	SYNC4	1	R/W	These bits select whether TCNT operation is independent of
3	SYNC3	1	R/W	or synchronized with other channels.
2	SYNC2	1	R/W	0: TCNT_5 to TCNT_0 operate independently
1	SYNC1	1	R/W	1: TCNT_5 to TCNT_0 perform synchronous operation
0	SYNC0	1	R/W	

(5) Flowchart



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1.00	Sep.11.06	—	First edition issued

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