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H8SX Series

Four-Phase Pulse Output Using a PPG

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

Contents

1. Overview

One channel of the 16-bit pulse unit (TPU) and one output group of the programmable pulse generator (PPG) of the H8SX series are used to output four-phase pulses. You can use all four timer channels, TPU0 to TPU3, and PPG output groups 0 to 3 to output four-channel 4-bit asynchronous pulses.

The TPU compare matches are used as the PPG start factors. You can also set a non-overlap period between multiple pulse outputs.

2. Configuration

The example shown below uses channel 3 (TPU3) of the 16-bit timer pulse unit and output group 3 of the programmable pulse generator (PPG). This sample uses the compare matches of TPU3 timer general registers A (TGRA_3) and B (TGRB_3) as pulse output triggers. When compare match B occurs, the PPG changes the pulse output level from high to low. When compare match A occurs, it changes the pulse output level from low to high. The time between the occurrences of compare matches B and A becomes the non-overlap period. The update processing of the PPG next data register (NDR) is performed not between the occurrences of compare matches from B to A, but between those of compare matches from A to B (this processing is implemented as part of the compare match A interrupt processing). You can set any pulse output timing within the range of values that can be set in the timer general registers. When the peripheral module clock (Pϕ) is 25 MHz and the count clock is Pϕ/1, you can set up to 2.62 msec in each timer general register. Figure 1 is a block diagram.

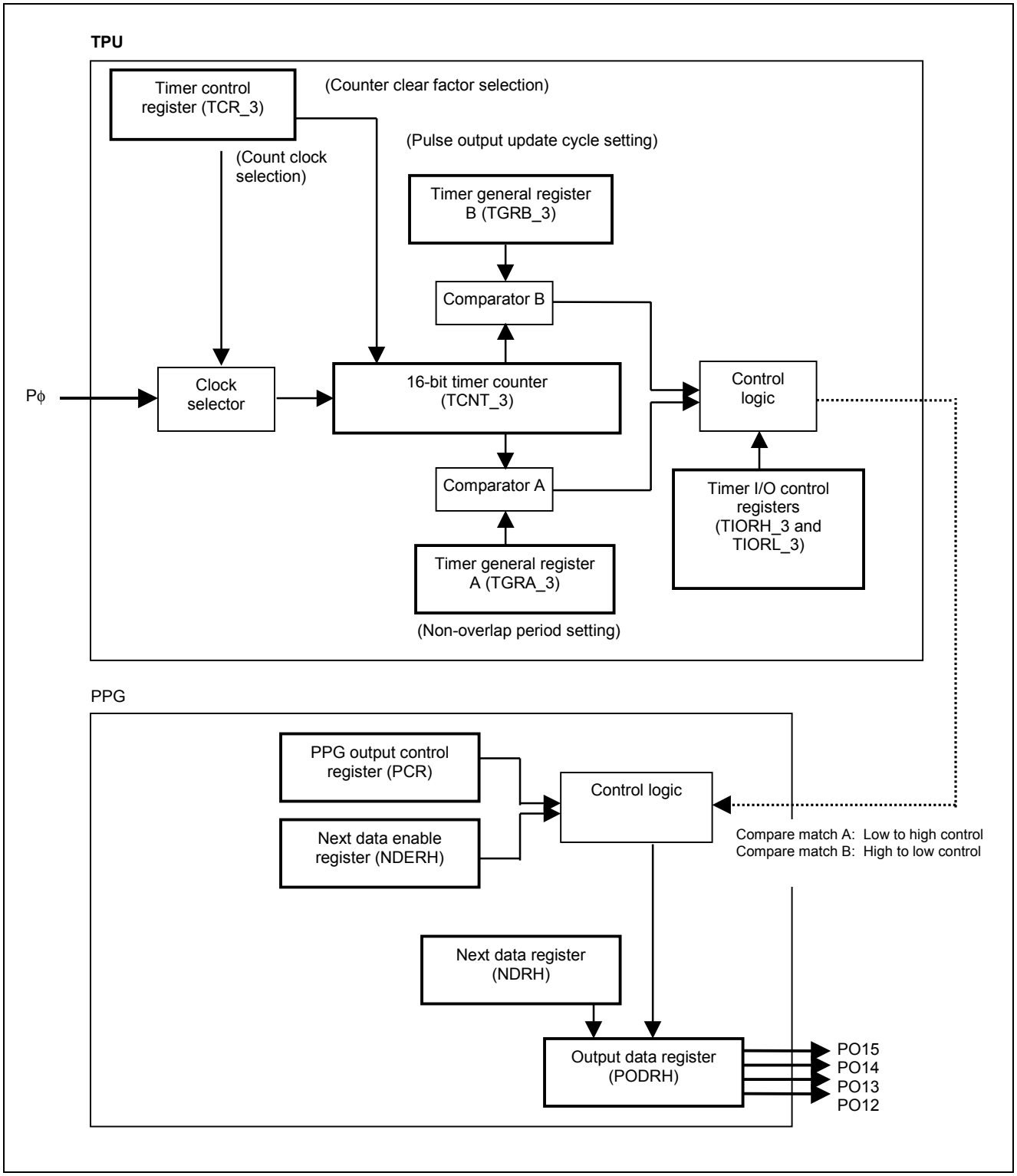


Figure 1 Block Diagram of Four-Phase Pulse Output Using the PPG

Figure 2 shows an example of non-overlap four-phase pulse output.

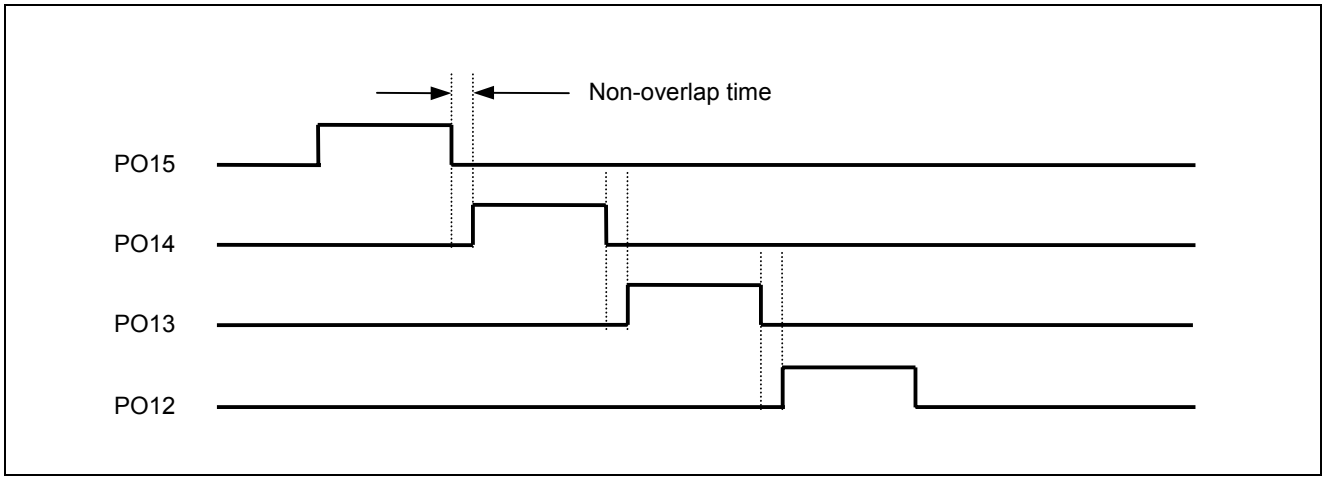


Figure 2 Example of Non-Overlap Four-Phase Pulse Output

3. Sample Program

3.1 Function

The timer count value for each of the pulse output trigger cycle (pulse output update cycle) and non-overlap period is set in each of timer general registers B and A respectively. You can calculate the timer values for the two times by using the following equations:

trigger-cycle = timer-value-set-in-TGRB_3 × TPU3-count-clock
non-overlap-period = timer-value-set-in-TGRA_3 × TPU3-count-clock

Assume that the TPU3 count clock is peripheral module (Pϕ)/1. When Pϕ is 25 MHz, the TPU3 count clock is 40 nsec. The non-overlap period must be shorter than the trigger cycle (TGRA_3 < TGRB_3). Figure 3 shows an example of operation.

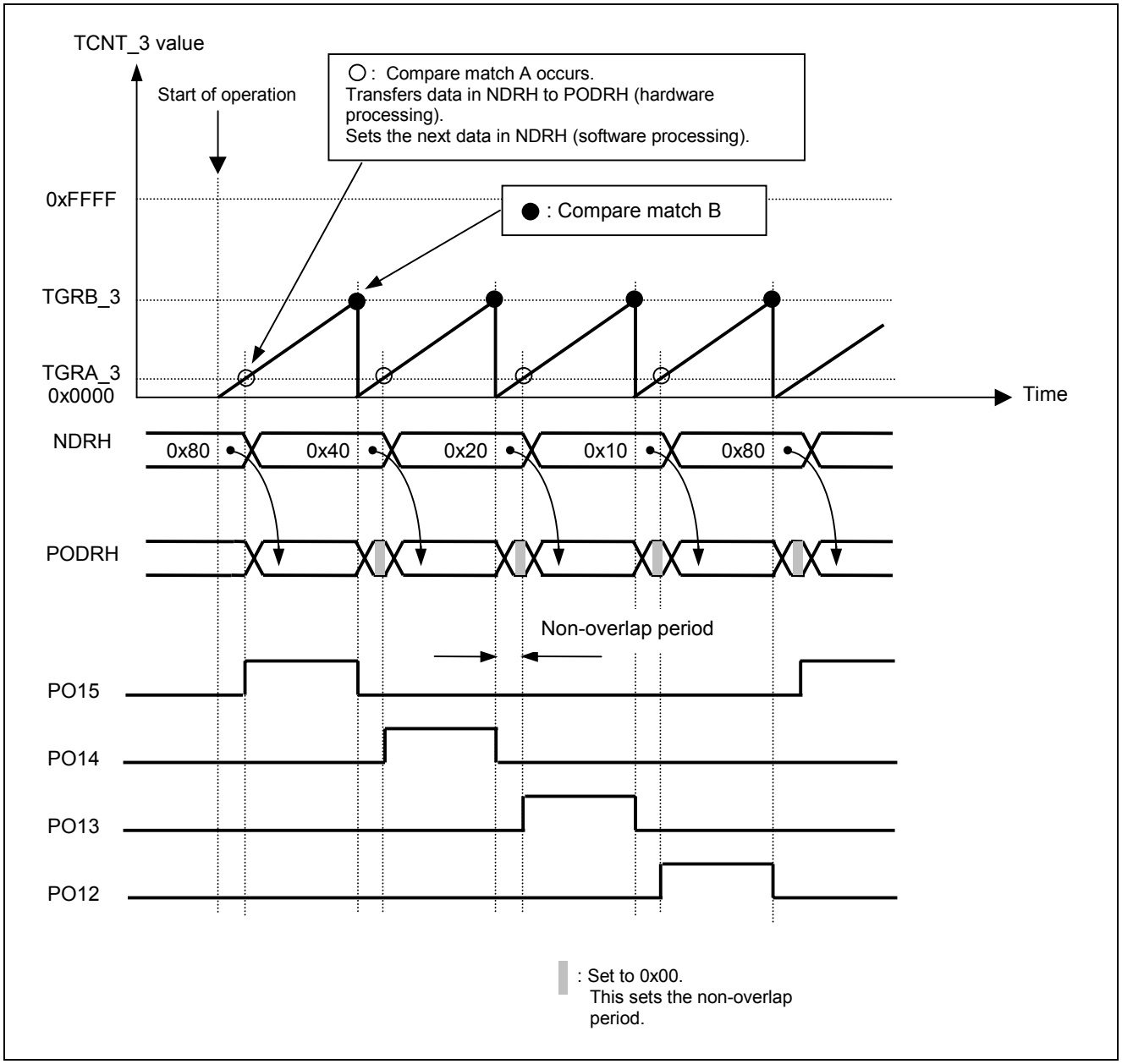


Figure 3 Example of Non-Overlap Four-Phase Pulse Output Operation

Table 1 lists the function allocations used TPU3 and PPG.

Table 1 Function Allocation in TPU3 and PPG

Type		Name	Function
Common	Register	MSTPCRA	Cancels the TPU and PPG module stop mode.
		TSTR	Specifies whether to start or stop the TPU3 timer count operation.
TPU3	Register	TCR_3	Sets the TCNT_3 count clock and counter clear factor.
		TGRA_3	Compare match counter value for the non-overlap period
		TGRB_3	Compare match counter value for the pulse output trigger period
		TIORH_3	Sets the no output when a compare match occurs.
		TIER_3	Enables interrupts by compare match A.
PPG	Register	PMR	Sets non-overlap mode.
		PCR	Sets the pulse output trigger.
		NDERH	Enables PO15 to PO12 pulse output.
		NDRH	Stores the next output data of PO15 to PO12.
		PODRH	Stores output data of PO15 to PO12.
	Output pin	PO15 to PO12	Pulse output pin

3.2 Function Specifications

The functions that set pulse output are shown as a sample program. The function specifications are listed below.

(1) Routine for setting four-pulse output using the PPG

```
void  ppg4_set ( unsigned short non_overlap_count, unsigned short
trigger_count )
```

Argument	Description
non_overlap_count	Specifies the timer value for the non-overlap period. If non_overlap_count is greater than or equal to trigger_count, normal operation is not performed. The count clock is fixed to Pϕ/1.
trigger_count	Specifies the timer value for the pulse output trigger cycle. If trigger_count is smaller than or equal to non_overlap_count, normal operation is not performed. The count clock is fixed to Pϕ/1.

Return value	Description
None	—

(2) Compare match A interrupt handler

```
void  inthdr_compareA ( void )
```

This function has neither an argument nor return value because it is a TPU3 interrupt handler. You must register this interrupt handler in the interrupt vector table.

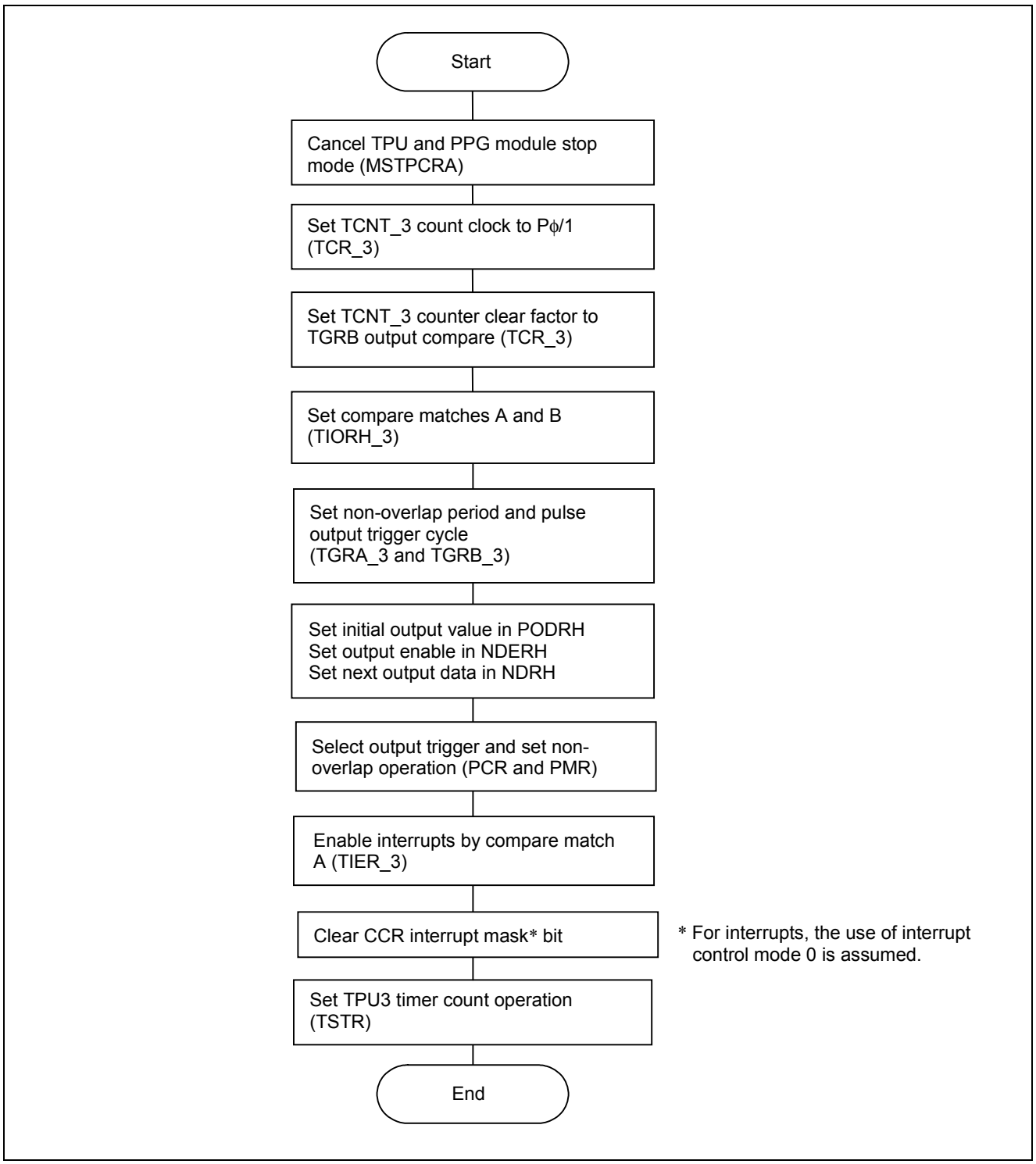
Example)

```
#define TRIGGER_TIME      2000        // Delay:  2000 µsec
#define NON_OVERLAP_TIME   100        // High width:  100 µsec
#define P_CLOCK             25        // Pϕ (MHz)
                                      // External function reference declaration
extern void  ppg4_set ( unsigned short, unsigned short );
void   main( void )                   // Main routine
{
   unsigned short  trigger;
   unsigned short  nonoverlap;

   trigger    = ((unsigned short)TRIGGER_TIME      *P_CLOCK);
   nonoverlap = ((unsigned short) NON_OVERLAP_TIME *P_CLOCK);
                                      // Sets non-overlap pulse output.
   ppg4_set ( nonoverlap, trigger );

   ...

}
```

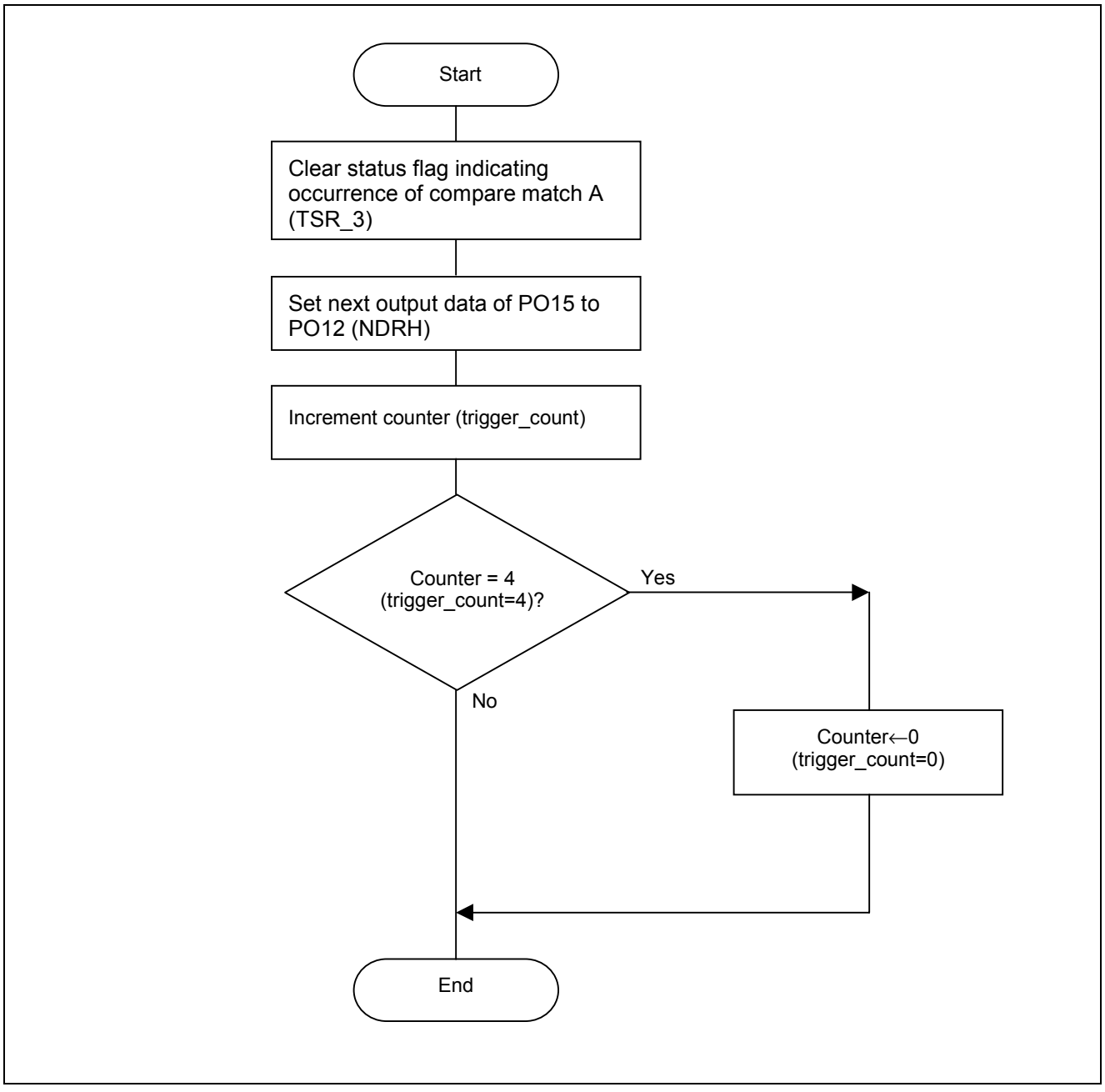
3.3 Flowchart

The processing flow is shown below.

(1) void ppg4_set (unsigned short, unsigned short)



(2) void inthdr_compareA (void)



3.4 Program Listing

A source program listing is shown below. In this source program, Renesas's standard definition (file automatically generated by High-performance Embedded Workshop: iodefine.h) defines the I/O register structure. If you want to specify your own definition, change the I/O register structure in the sample program.

```
/************************************************************/
/* include file                                             */
/************************************************************/
#include <machine.h>
#include "iodefine.h"

/************************************************************/
/* function prototype                                       */
/************************************************************/
void ppg4_set( unsigned short, unsigned short );

/************************************************************/
/* static variable                                          */
/************************************************************/
static const unsigned char  next_data[4]
                            = { 0x80, 0x40, 0x20, 0x10 };
static unsigned char  trigger_count;

/************************************************************/
/* function definition                                      */
/************************************************************/
void ppg4_set( unsigned short non_overlap_count,
               unsigned short trigger_count )
{
    P_MSTPCRA.BIT.MSTPA0  = 0;   // reset module-standby for TPU
    P_MSTPCRB.BIT.MSTPB15 = 0;   // reset module-standby for PPG
    P_TPU3.TCR.BIT.TPSC   = 0;   // set TPU3 countup clock source
    P_TPU3.TCR.BIT.CCLR   = 2;   // set TPU3 counter clear cause
    P_TPU3.TIOR.BIT.IOA   = 0;   // set TPU3 compare-match-A
    P_TPU3.TIOR.BIT.IOB   = 0;   // set TPU3 compare-match-B
    P_TPU3.TGRA = (unsigned int)non_overlap_count;
    P_TPU3.TGRB = (unsigned int) trigger_count;
    P_PPG.PODR.BIT.POD15  = 0;   // set PPG initial pulse data
    P_PPG.PODR.BIT.POD14  = 0;
    P_PPG.PODR.BIT.POD13  = 0;
    P_PPG.PODR.BIT.POD12  = 0;
    trigger_count    = 0;        // set PPG next pulse data
    P_PPG.NDRH1.BYTE = next_data[trigger_count++];
    P_PPG.NDER.BIT.NDER15 = 1;   // set PPG next pulse enable
    P_PPG.NDER.BIT.NDER14 = 1;
    P_PPG.NDER.BIT.NDER13 = 1;
    P_PPG.NDER.BIT.NDER12 = 1;
    P_PPG.PMR.BIT.G3NOV = 1;     // set PPG non-overlap mode
    P_PPG.PCR.BIT.G3CMS = 3;     // set PPG output trigger
    P_TPU3.TIER.BIT.TGIEA = 1;   // set TGI3A-interrupt enable
    set_imask_ccr(0);            // clear interrupt mask
    P_TPU.TSTR.BIT.CST3   = 1;   // start TPU3
```

```
}

/************************************************************/
/* interrupt handler definition                             */
/************************************************************/
#pragma interrupt ( inthdr_compareA )
void inthdr_compareA( void )
{
    volatile unsigned char  dummy;
    dummy = P_TPU3.TSR.BYTE;     // read TPU3 interrupt status
    P_TPU3.TSR.BIT.TGFA = 0;     // clear TGI3A-interrupt status
                                 // set PPG next pulse data
    P_PPG.NDRH1.BYTE = next_data[trigger_count++];
    if ( 4 <= trigger_count )     trigger_count = 0;
}
```

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sept.19.03	—	First edition issued

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