Macrocell Editor

Abstract

This application shows how to create the Verilog Code automatically using the Macrocell Editor in the software. The Macrocell feature will let you assemble and configure your design graphically using a library of numerous Blocks ranging from different Logic Gates, Sequential Logic Blocks, in-built IP Blocks.

This application note comes complete with design files which can be found in the References section

Contents

1. Terms and Definitions

CLB	Configuration Logic Block
HDL	Editor Workspace where Verilog code is entered
FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection
ForgeFPGA	Window Main FPGA project window for debug and IO programming

2. References

For related documents and software, please visit: ForgeFPGA Low-density FPGA: Small-scale Programmable Logic Device | Renesas. Download our free ForgeFPGA™ Designer software [1] to open the .ffpga design files [2] and view the proposed circuit design.

[1] ForgeFPGA Designer Software, Software Download and User Guide

[2] AN-FG-003 Macrocell Editor.ffpga, ForgeFPGA Design File, Renesas Electronics

[3] SLG47910, Datasheet, Renesas Electronics

3. Introduction

The Macrocell Editor works on the same lines as the GreenPAK software. This feature will let you assemble and configure your design graphically using a library of numerous Blocks ranging from different Logic Gates, Sequential Logic Blocks, in-built IP Blocks. You'll be able to generate the Verilog Code using the schematics that you create with the Macrocell Editor and use it in our toolchain.

This tool allows you to take advantage of the flexibility of FPGAs even without knowledge of Verilog Code. Launch the tool by clicking the corresponding button on the toolbar or go to the main menu, *Windows → Macrocell Editor*

4. Ingredients

- Latest Revision of ForgeFPGA Workshop software

5. Verilog Code

The autogenerated top module is called **macrocellmode_autogen**. The Verilog code displays how to connect different modules under one top module using synchronous style of Verilog coding. Below is the code generated automatically for the Macrocells used in creating this design (See Figure 3)

```
module mcm_adder_2bit (
  input  [1:0] A,          // 2-bit operand A
  input  [1:0] B,          // 2-bit operand B
  output [2:0] sum         // 2-bit sum
);

  assign  sum = A + B;

endmodule

module mcm_and_2(input a, b, output y);
  and(y, a, b);
endmodule

module mcm_nand_2(input a, b, output y);
  wire Yd;
  and(Yd, a, b);
  not(y, Yd);
endmodule

module mcm_comparator_2bit(
  input [1:0] A,  // 2-bit input A
  input [1:0] B,  // 2-bit input B
  output      EQ, // 1 if A == B
  output      GT, // 1 if A > B
  output      LT  // 1 if A < B
);

  assign EQ = (A == B); // Equality check
  assign GT = (A > B);  // Greater than check
  assign LT = (A < B);  // Less-than check

endmodule

module mcm_d_flip_flop(input clk, d, output reg q);
  always @(posedge clk)
    q <= d;
endmodule
```

6. Design Steps

1. Open the ForgeFPGA Workshop software in GreenPAK and select the SLG47910 device From the ForgeFPGA tool bar, select the FPGA Editor Tab (see Figure 1).

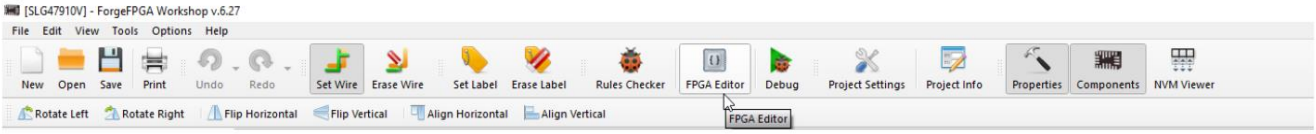

Figure 1.ForgeFPGA Tool Bar

2. Launch the Macro Cell Editor Window from the toolbar on the top.

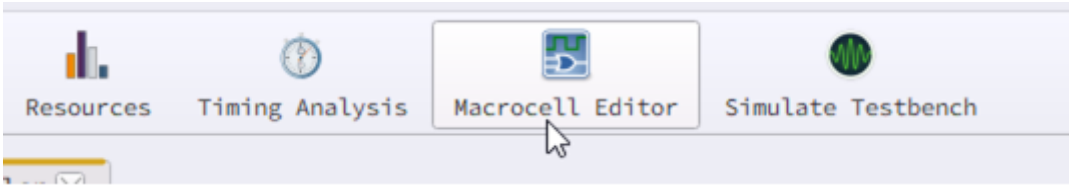

Figure 2.Macrocell Editor Icon

3. In the Macrocell Editor Window, create the design of your choice by dragging and dropping the blocks from the library on the right side of the window and connecting the ports through the wires.

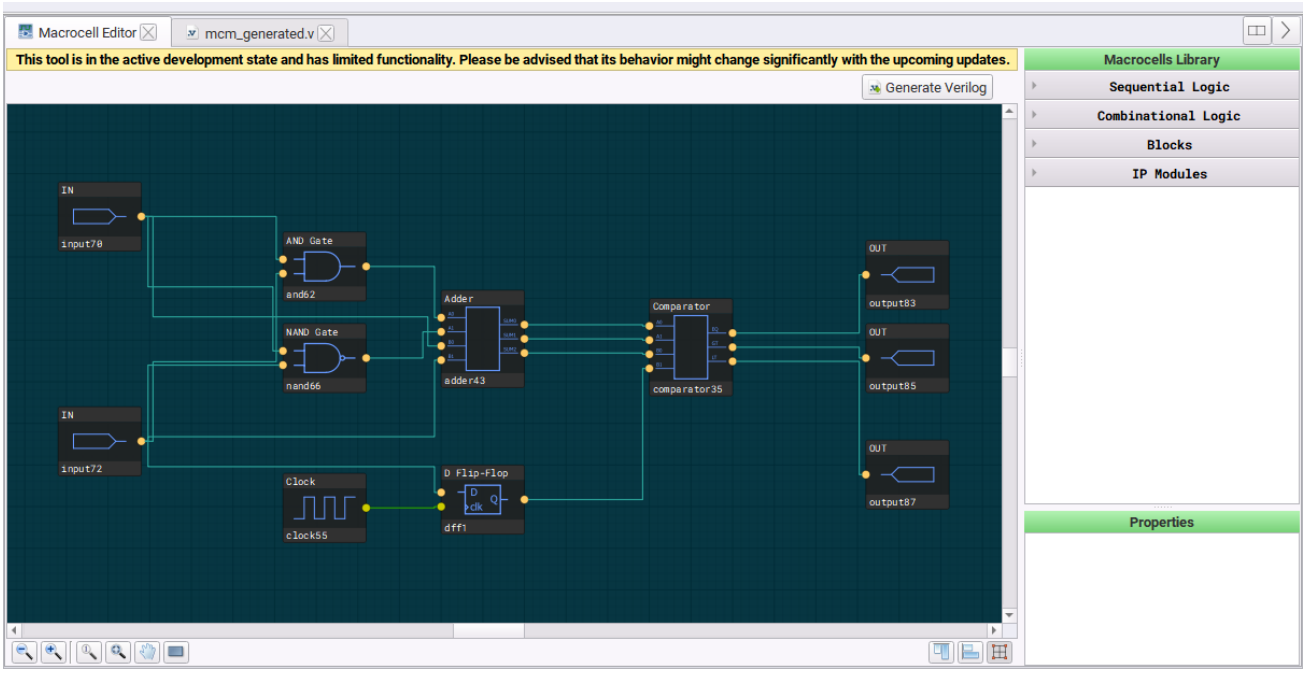

Figure 3.Macrocell Editor and Library

4. The P*roperties* panel shows the details for one selected Macrocell or connection. The *Name* field is editable (double-click the filed or the Macrocell).

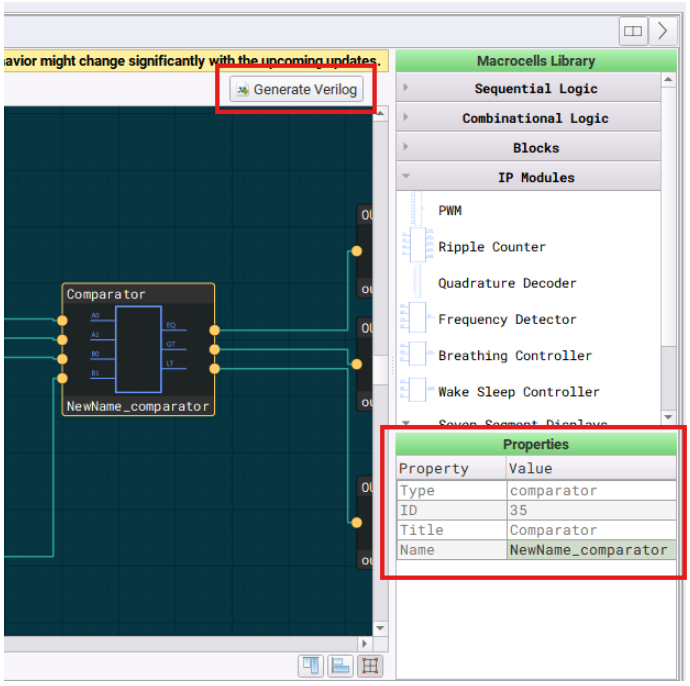

Figure 4.Macrocell Properties

5. After the user has created the desired design, click on the *Generate Verilog* button on the right to automatically generate the Verilog code for the design created in Macrocell Editor (See Figure 4). The name of the generated Verilog code is by default *mcm_generated.v* and it's listed under Custom Code section of the Control panel.
6. User can notice that the Macrocells may have clock and logic port types, which can be distinguished by color, clicking two ports of the same type created the connection between the Macrocell (See Figure 5)

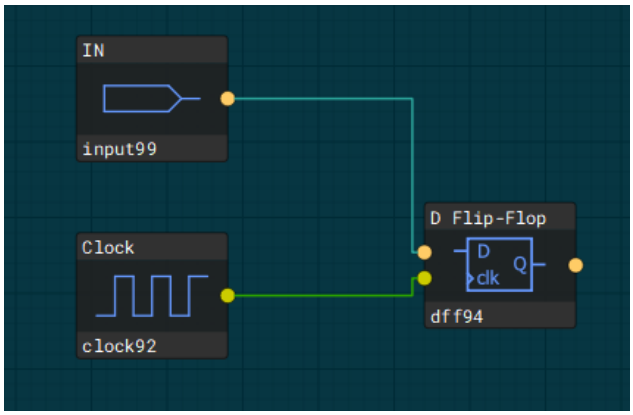

Figure 5.Connection between Macrocell

7. User can save the Verilog code automatically created or edit it as per the need. The user can then Synthesize the design and create a testbench to check the functionality of the design.

7. Conclusion

This Application Note outlines how to create a design in the Macrocell Editor and how to create its Verilog code automatically. This feature in the GoConfigure Software will help the user to bypass the process of writing Verilog code and aide in creating circuit designs using Schematic View.

If interested, please contact ForgeFPGA Business Support Team.

8. Revision History

Revision	Date	Description
1.00	Dec 10, 2021	Initial release.
1.01	Feb 20, 2024	Revised according to BB revision
1.02	Oct 15,2025	Revised according to the updated Macrocell library

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