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H8SX Family

Externally Triggered Output of Pulse Trains with Seven Phases

Introduction

Pulse trains with seven phases are output in synchronization with the falling edge of an external signal.

Target Device

H8SX/1663

Contents

1. Specification

Figure 1 illustrates the output of pulse trains with seven phases in synchronization with the falling edge of an external signal.

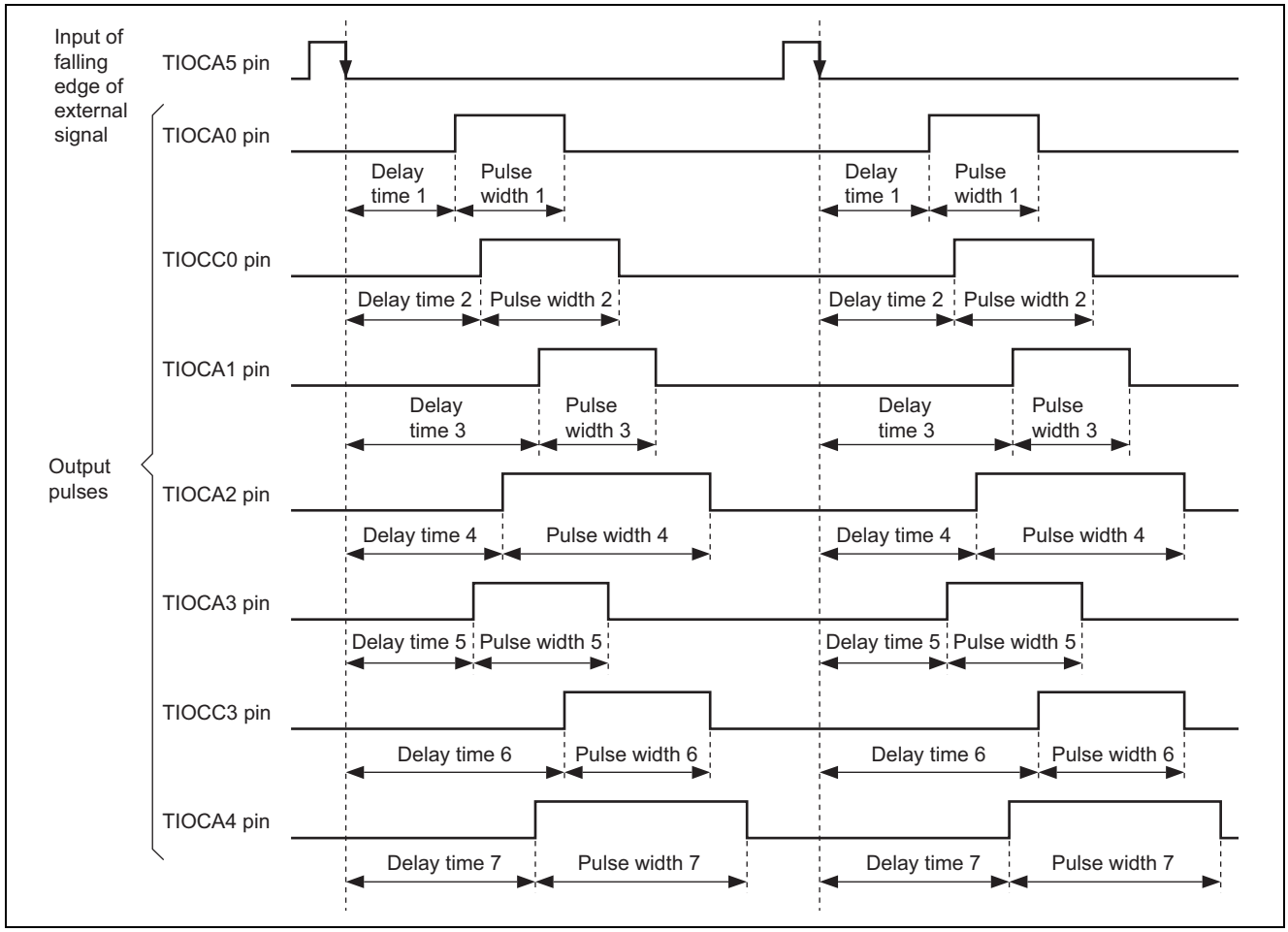


Figure 1 Example of the Output of Synchronized Pulses

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
Operating Frequency	Input clock	: 12 MHz
	System clock (Iϕ)	: 48 MHz
	Peripheral module clock (Pϕ)	: 24 MHz
	External bus clock (Bϕ)	: 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)	

3. Description of Functions Used

3.1 Functions Used

In this sample task, the following functions of TPU are used to output pulse trains with seven phases in synchronization with an external signal.

- Clearing of the timer counter on detection of the falling edge of a pulse
- Simultaneous clearing of multiple timer counters
- Generation of PWM output by using TGRA and TGRB, and TGRC and TGRD, as respective pairs

A block diagram of the TPU is given as figure 2, with descriptions overleaf.

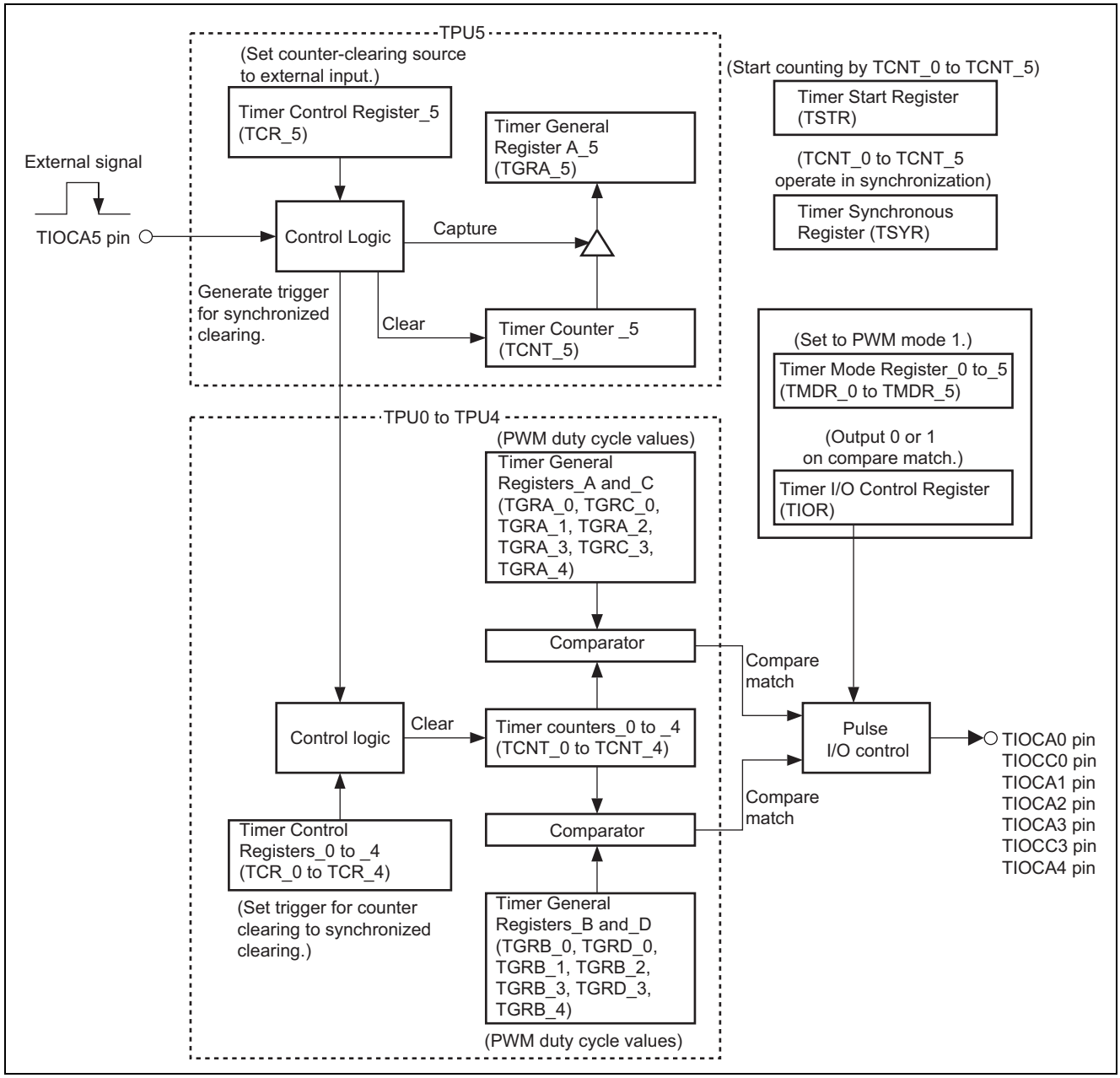


Figure 2 Block Diagram

- Timer Start Register (TSTR)
  TSTR starts or stops operation for channels 0 to 5. Stop the TCNT counter before setting the operating mode in TMDR or the clock for counting in TCR.

- Timer Control Register (TCR)
  TCR controls the TCNT operation for each channel. The TPU has a total of six TCR registers, one for each channel. TCR register settings should only be made while TCNT operation is stopped.

- Timer I/O Control Register (TIOR)
  TIOR controls TGR. The TPU has eight TIOR registers, two each for channels 0 and 3, and one each for channels 1, 2, 4, and 5. Care is required since TIOR is affected by the TMDR setting.
  The initial output specification for TIOR becomes effective when the counter is stopped (the CST bit in TSTR is cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter is cleared to 0 is specified.
  When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.
  To designate the input capture pin in TIOR, the DDR bit and ICR bit for the corresponding pin should be set to 0 and 1, respectively.

- Timer Counter (TCNT)
  TCNT is a 16-bit readable/writable counter. The TPU has six TCNT counters, one for each channel. TCNT is initialized to H'0000 by a reset or in hardware standby mode. TCNT cannot be accessed in 8-bit units. TCNT must always be accessed in 16-bit units.

- Timer General Register (TGR)
  TGR is a 16-bit readable/writable register and has a dual function as an output compare or input capture register. The TPU has 16 TGR registers, four each for channels 0 and 3 and two each for channels 1, 2, 4, and 5. TGRC and TGRD for channels 0 and 3 can also be designated for operation as buffer registers.
  The TGR registers cannot be accessed in 8-bit units; they must always be accessed in 16-bit units.

- Timer Synchronous Register (TSYR)
  TSYR selects independent or synchronized operation for the TCNT counters of channels 0 to 5.

- Timer Mode Register (TMDR)
  TMDR sets the operating mode for each channel. The TPU has six TMDR registers, one for each channel. TMDR register settings should only be made while TCNT operation is stopped.

3.2 PWM Mode 1

In PWM mode 1, output signals are generated from the TIOCA and TIOCC pins by using TGRA and TGRB, and TGRC and TGRD, as respective pairs. Compare matches A and C cause the signals specified by bits IOA3 to IOA0 and IOC3 to IOC0 in TIOR, respectively, to be output from TIOCA and TIOCC and IOC3 to IOC0 in TIOR. Compare matches B and D cause the output of signals specified by bits IOB3 to IOB0 and IOD3 to IOD0 in TIOR, respectively. The initial output value is the value set for TGRA and TGRC. If the output setting for the other TGR in a pair is the same as the initial value, the output value will not change even when matches occur.

Output of PWM signals with up to eight phases is possible in PWM mode 1.

4. Principles of Operation

Figure 3 illustrates operation for the output of pulse trains with seven phases in synchronization with an output trigger. The hardware and software processing is described in table 2 overleaf.

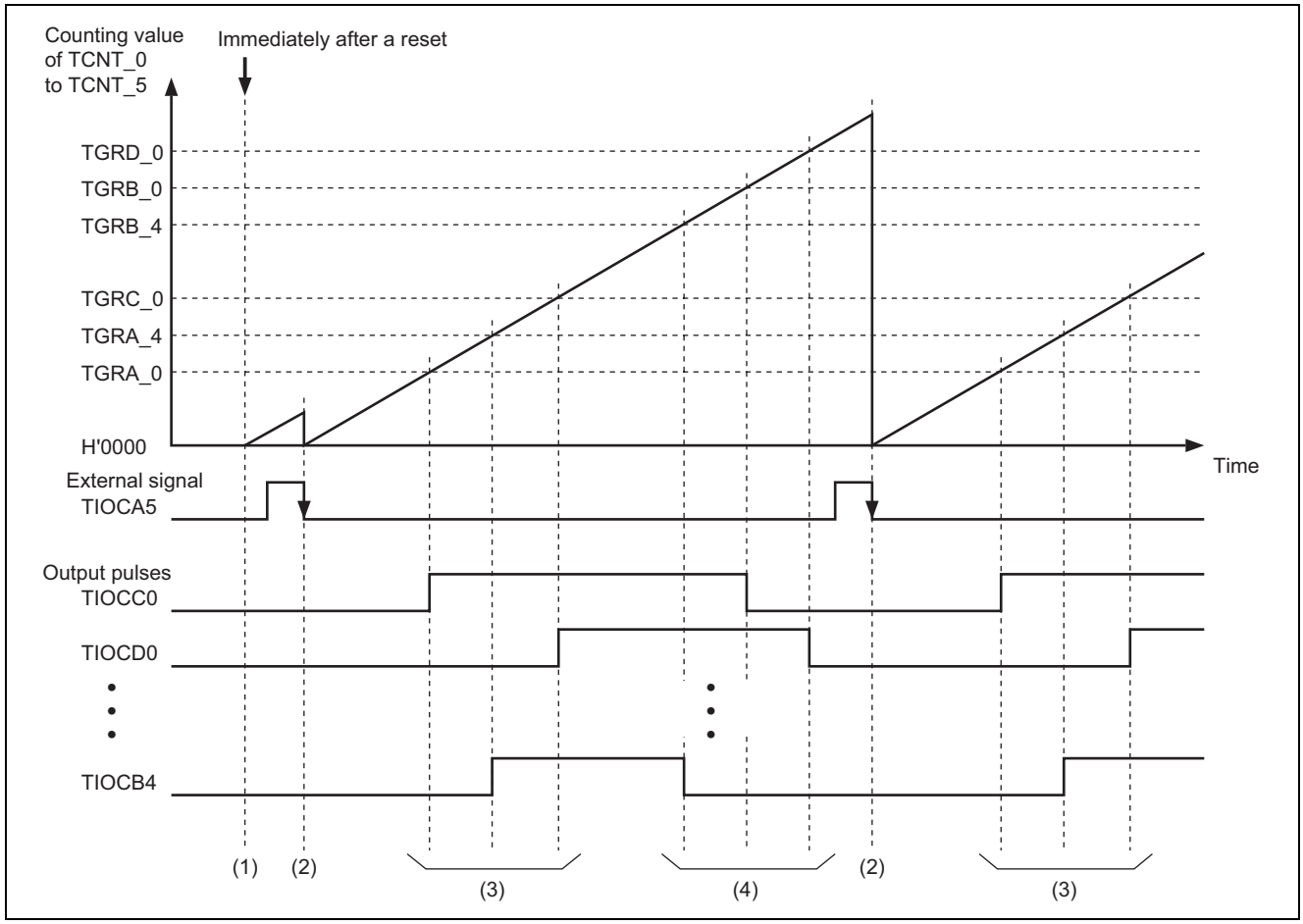


Figure 3 Operation for the Output of Pulse Signals

Table 2 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	(a) Initial settings*
(2)	(a) Input capture in TGR1A (b) Synchronized clearing of TCNT_0 to TCNT_5	No processing
(3)	(a) Compare match with TGR0C (b) Output 1 from the TIOCC0 pin.	No processing
(4)	(a) Compare match with TGR0D (b) Output 0 from the TIOCC0 pin.	No processing

Note: * Initial settings
(a) Set the counter clock to ϕ
(b) Set TGRA_5 as the trigger for clearing of TCNT.
(c) Set TGRA_5 as an input capture register and the other TGRs as output compare registers. Select the initial values and output values.
(d) Set PWM mode 1 as the operating mode.
(e) Set the delay times for output pulses in TGRA_0 to TGRA_4, TGRC_0, and TGRC_3. Set the pulse widths (high level) in TGRB_0 to TGRB_4, TGRD_0, and TGRD_3.
(f) Start counting.

5. Description of Software

5.1 Operating Environment

Table 3 Operating environment

Item	Description
Development tool	High-performance Embedded Workshop Ver.4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.01 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Data table

Table 5 Vector Table for Interrupt Exception Processing

Exception Processing Source	Vector No.	Vector Table Address	Destination Function
Reset	0	H'000000	init

5.2 List of Functions

Table 6 List of Functions

Function Name	Function
init	Initialization routine Sets the CCR and configures the clocks, releases modules from the module stop mode, and calls the main function.
main	Main routine Synchronously clears TPU_0 to TPU_5 and sets up the pulse output.

5.3 RAM Usage

In this sample task, the only RAM usage is for the stack.

5.4 Constants

Table 7 List of Constants

Type	Name of Variable	Setting	Description	Used in Function
unsigned short	set_dly[7]	0x0001, 0xFFFE, 0x003F, 0x0018, 0x000F, 0x0007, 0x0007,	Delay times for output pulses Sets the delay times between the falling edge of the external input and pulse output.	main
unsigned short	set_wid[7]	0x0002, 0x0001, 0x0060, 0x001F, 0x00F0, 0x00E0, 0x00C0,	Pulse width (high level)	main

5.5 Calculation Formulae

a. Delay time of output pulse

Delay time = timer counter value (TCNT)/TCNT counter clock
= TCNT/Pϕ/1 = TCNT/Pϕ

b. Pulse width (high level)

Pulse width = timer counter value (TCNT)/TCNT counter clock
= TCNT / Pϕ/1 = TCNT/Pϕ

5.6 Description of Functions

5.6.1 init Function

1. Functional overview
   Initialization routine which releases the modules from module stop mode, configures the clocks, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latch is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0 These bits indicate the operating mode selected by the mode pins (MD2 to MD0; see table 8). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latch is released by a reset.
10	MDS2	Undefined*	R	
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD3 to MD0.

Table 8 Values of bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select These bits select the frequency of the system clock provided to the CPU, DMAC, and DTC. 000: Input clock × 4
9	ICK1	0	R/W	
8	ICK0	0	R/W	
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select These bits select the frequency of the peripheral module clock. 001: Input clock × 2
5	PCK1	0	R/W	
4	PCK0	1	R/W	
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select These bits select the frequency of the external bus clock. 000: Input clock × 4
1	BCK1	0	R/W	
0	BCK0	0	R/W	

- MSTPCRA, MSTPCRB, and MSTPCRC control the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping the operation of bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode 1: Enabled all-module-clock-stop mode
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

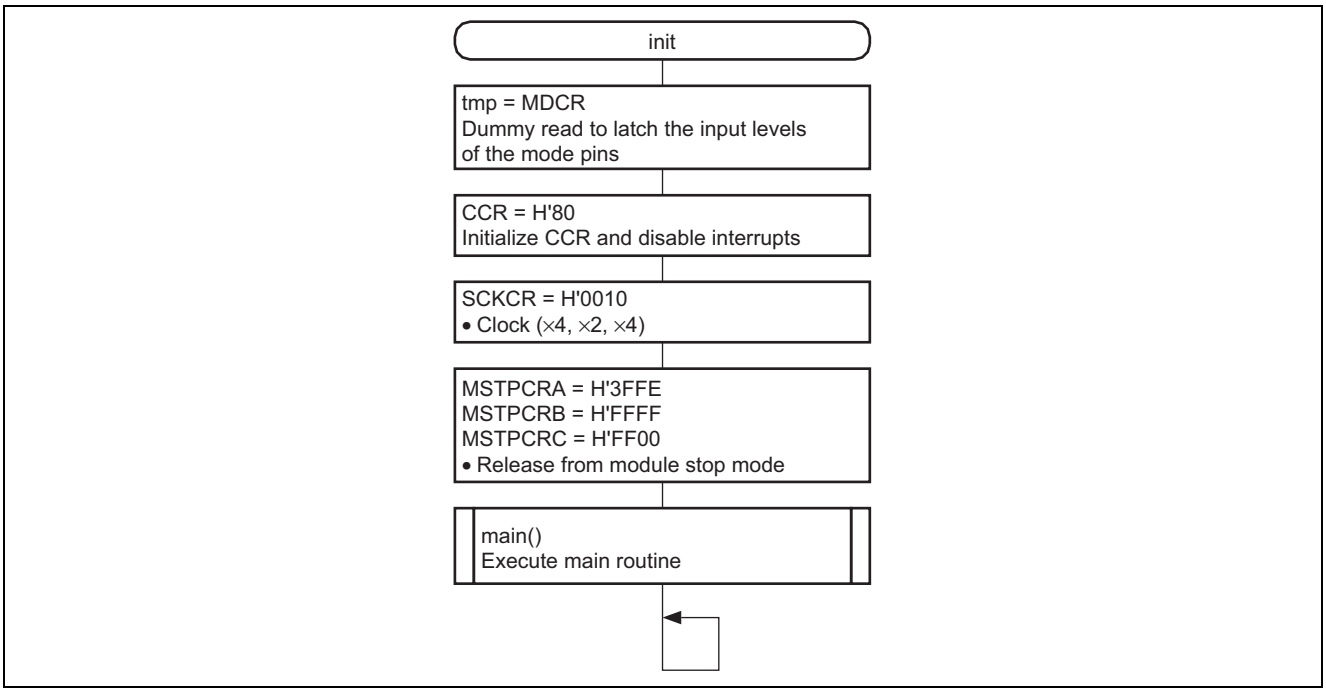
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface 1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input levels
of the mode pins
CCR = H'80
Initialize CCR and disable interrupts
SCKCR = H'0010
• Clock (×4, ×2, ×4)
MSTPCRA = H'3FFE
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release from module stop mode
main()
Execute main routine

5.6.2 main Function

1. Functional overview
   Synchronized clearing of TPU0 to TPU5 and setting of pulse output
2. Arguments
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 2 data direction register (P2DDR) Number of bits: 8 Address: H'FFFB81

Bit	Bit Name	Setting	R/W	Description
0	P20DDR	1	R/W	0: Sets P20 as an input pin 1: Sets P20 as an output pin

- Port 2 input buffer control register (P2ICR) Number of pins: 8 Address: H'FFFB91

Bit	Bit Name	Setting	R/W	Description
6	P26ICR	1	R/W	0: Disables input buffer for pin P26. Input signal is fixed to high level. 1: Enables input buffer for pin P26. Reflects the state of the pin on the peripheral module side.

- Timer control register_0 (TCR_0) Number of bits: 8 Address: H'FFFFC0

Bit	Bit Name	Setting	R/W	Description
7	CCLR2	0	R/W	Counter clear 2 to 0
6	CCLR1	1	R/W	Select the trigger for clearing of TCNT_4.
5	CCLR0	1	R/W	011: Clears other TCNT_n for which synchronous clearing/operation has been selected.
4	CKEG1	0	R/W	Clock edge 1 and 0
3	CKEG0	0	R/W	Select the input clock edge. 00: Counts falling edges
2	TPSC2	0	R/W	Timer prescaler 2 to 0
1	TPSC1	0	R/W	Select the TCNT counter clock
0	TPSC0	0	R/W	000: Counts cycles of the internal clock Pϕ/1

- Timer control register_1 (TCR_1) Number of bits: 8 Address: H'FFFFD0
- Timer control register_2 (TCR_2) Number of bits: 8 Address: H'FFFFE0
- Timer control register_3 (TCR_3) Number of bits: 8 Address: H'FFFFF0
- Timer control register_4 (TCR_4) Number of bits: 8 Address: H'FFFEE0
- Timer control register_5 (TCR_5) Number of bits: 8 Address: H'FFFEF0

Bit	Bit Name	Setting	R/W	Description
7	CCLR2	0	R/W	Counter clear 2 to 0
6	CCLR1	0	R/W	Select the trigger for clearing of counter TCNT_0.
5	CCLR0	1	R/W	001: TCNT_0 cleared on compare match/input capture in TGRA
4	CKEG1	0	R/W	Clock edge 1 and 0
3	CKEG0	0	R/W	Select the input clock edge.
				00: Counts falling edges
2	TPSC2	0	R/W	Timer prescaler 2 to 0
1	TPSC1	0	R/W	Select the TCNT counter clock
0	TPSC0	0	R/W	000: Counts cycles of the internal clock Pϕ/1

- Timer mode register_0 (TMDR_0) Number of bits: 8 Address: H'FFFFC1
- Timer mode register_1 (TMDR_1) Number of bits: 8 Address: H'FFFFD1
- Timer mode register_2 (TMDR_2) Number of bits: 8 Address: H'FFFFE1
- Timer mode register_3 (TMDR_3) Number of bits: 8 Address: H'FFFFF1
- Timer mode register_4 (TMDR_4) Number of bits: 8 Address: H'FFFEE1

Bit	Bit Name	Setting	R/W	Description
3	MD3	0	R/W	Mode 3 to 0
2	MD2	0	R/W	Set the timer operating mode
1	MD1	1	R/W	0010: PWM mode 1
0	MD0	0	R/W	

- Timer mode register_5 (TMDR_5) Number of bits: 8 Address: H'FFFEF1

Bit	Bit Name	Setting	R/W	Description
3	MD3	0	R/W	Mode 3 to 0
2	MD2	0	R/W	Set the timer operating mode
1	MD1	0	R/W	0000: Normal operation
0	MD0	0	R/W	

- Timer I/O control register H_0 (TIORH_0) Number of bits: 8 Address: H'FFFFC2
- Timer I/O control register_1 (TIOR_1) Number of bits: 8 Address: H'FFFFD2
- Timer I/O control register_2 (TIOR_2) Number of bits: 8 Address: H'FFFFE2
- Timer I/O control register H_3 (TIORH_3) Number of bits: 8 Address: H'FFFFF2
- Timer I/O control register _4 (TIOR_4) Number of bits: 8 Address: H'FFFEE2

Bit	Bit Name	Setting	R/W	Description
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	1	R/W	Specify the function of TGRB.
5	IOB1	0	R/W	0010: TGRB functions as an output compare register.
4	IOB0	1	R/W	In PWM mode 1, 0 is output from the TIOCA pin on a compare match with TGRB.
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	Specify the function of TGRA.
1	IOA1	1	R/W	0010: TGRA functions as an output compare register.
0	IOA0	0	R/W	In PWM mode 1, 1 is output from the TIOCA pin on a compare match with TGRA.

- Timer I/O control register L_0 (TIORL_0) Number of bits: 8 Address: H'FFFFC3
- Timer I/O control register L_3 (TIORL_3) Number of bits: 8 Address: H'FFFFF3

Bit	Bit Name	Setting	R/W	Description
7	IOD3	0	R/W	I/O Control D3 to D0
6	IOD2	1	R/W	Specify the function of TGRD.
5	IOD1	0	R/W	0010: TGRD functions as an output compare register.
4	IOD0	1	R/W	In PWM mode 1, 0 is output from the TIOCC pin on a compare match with TGRD.
3	IOC3	0	R/W	I/O Control C3 to C0
2	IOC2	0	R/W	Specify the function of TGRC.
1	IOC1	1	R/W	0010: TGRC functions as an output compare register.
0	IOC0	0	R/W	In PWM mode 1, 1 is output from the TIOCC pin on a compare match with TGRC.

- Timer I/O control register_5 (TIOR_5) Number of bits: 8 Address: H'FFFEF2

Bit	Bit Name	Setting	R/W	Description
7	IOB3	0	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	Specify the function of TGRB_5.
5	IOB1	0	R/W	0000: TGRB_5 functions as an output compare register.
4	IOB0	0	R/W	This setting disables output from the TIOCA5 pin.
3	IOA3	1	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	Specify the function of TGRA_5.
1	IOA1	0	R/W	1001: TGRA functions as an output compare register.
0	IOA0	1	R/W	Input capture is executed on falling edges of TIOCA5 pin.

- Timer general register A_0 (TGRA_0) Number of bits: 16 Address: H'FFFFC8
- Timer general register C_0 (TGRC_0) Number of bits: 16 Address: H'FFFFCC
- Timer general register A_1 (TGRA_1) Number of bits: 16 Address: H'FFFFD8
- Timer general register A_2 (TGRA_2) Number of bits: 16 Address: H'FFFFE8
- Timer general register A_3 (TGRA_3) Number of bits: 16 Address: H'FFFFF8
- Timer general register C_3 (TGRC_3) Number of bits: 16 Address: H'FFFFFC
- Timer general register A_4 (TGRA_4) Number of bits: 16 Address: H'FFFEE8

Function: These registers are used as output compare registers and set the delay times for the PWM waveforms.

Settings: TGRA_0=set_dly[0], TGRC_0=set_dly[1], TGRA_1=set_dly[2], TGRA_2=set_dly[3], TGRA_3=set_dly[4], TGRC_3=set_dly[5], TGRA_4=set_dly[6]

- Timer general register B_0 (TGRB_0) Number of bits: 16 Address: H'FFFFCA
- Timer general register D_0 (TGRD_0) Number of bits: 16 Address: H'FFFFCE
- Timer general register B_1 (TGRB_1) Number of bits: 16 Address: H'FFFFDA
- Timer general register B_2 (TGRB_2) Number of bits: 16 Address: H'FFFFEA
- Timer general register B_3 (TGRB_3) Number of bits: 16 Address: H'FFFFFA
- Timer general register D_3 (TGRD_3) Number of bits: 16 Address: H'FFFFFE
- Timer general register B_4 (TGRB_4) Number of bits: 16 Address: H'FFFEEA

Function: These registers are used as output compare registers and set the reset values for the PWM waveforms.

Settings: TGRB_0=set_wid[0], TGRD_0=set_ wid[1], TGRB_1=set_ wid[2], TGRB_2=set_wid[3], TGRB_3=set_wid[4], TGRD_3=set_wid[5], TGRB_4=set_wid[6]

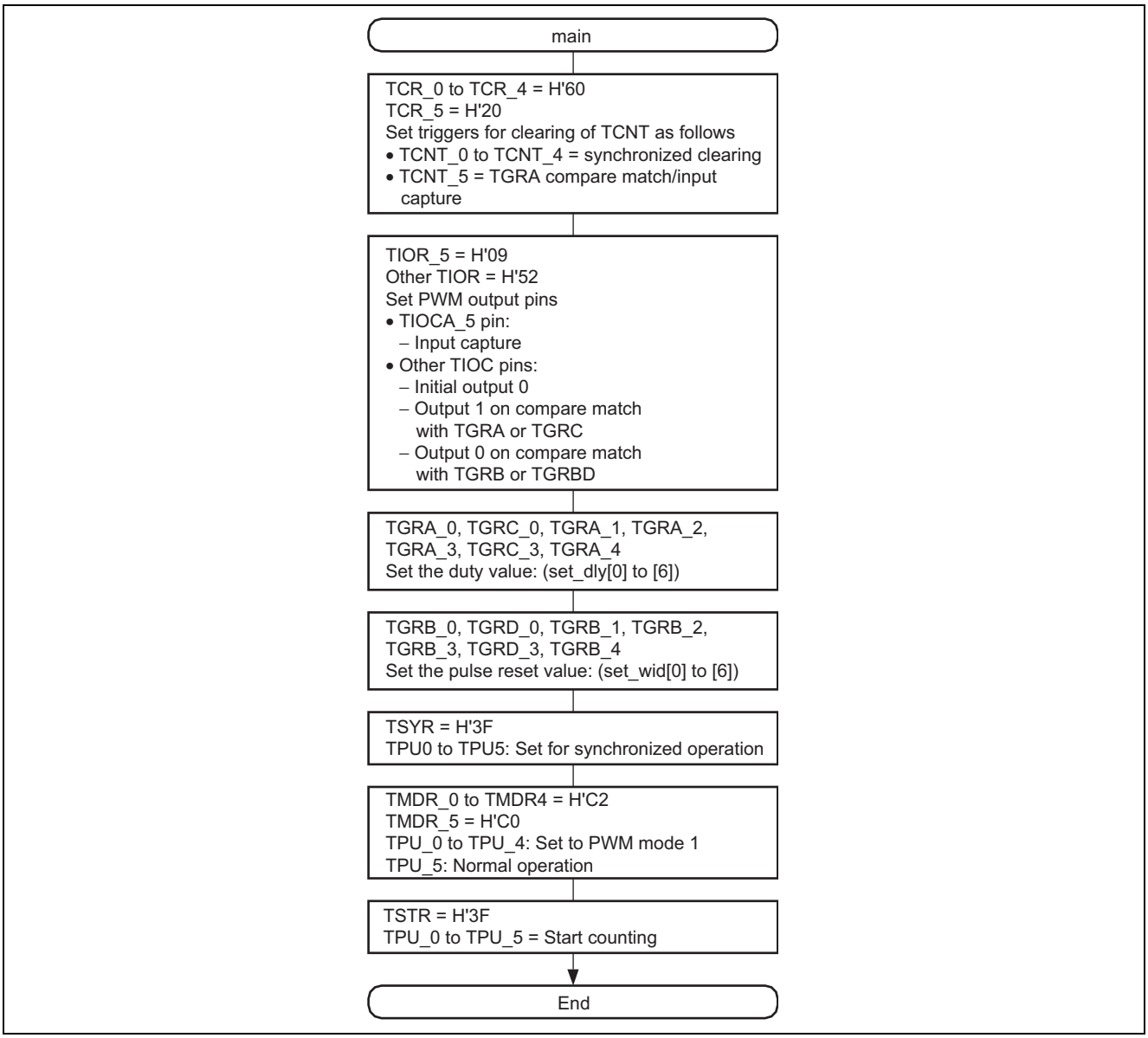
- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Description
5	CST5	1	R/W	Counter start 5 to 0
4	CST4	1	R/W	Selects operation or stoppage for TCNT
3	CST3	1	R/W	0: Stops counting by TCNT_5 to TCNT_0
2	CST2	1	R/W	1: Counting by TCNT_5 to TCNT_0
1	CST1	1	R/W	
0	CST0	1	R/W	

- Timer synchronous register (TSYR) Number of bits: 8 Address: H'FFFFBD

Bit	Bit Name	Setting	R/W	Description
5	SYNC5	1	R/W	Timer synchronization 5 to 0
4	SYNC4	1	R/W	Selects independent/synchronized operation for the TCNT counters.
3	SYNC3	1	R/W	0: TCNT_5 to TCNT_0 operate independently
2	SYNC2	1	R/W	1: TCNT_5 to TCNT_0 operates in synchronization
1	SYNC1	1	R/W	
0	SYNC0	1	R/W	

5. Flowchart


main
TCR_0 to TCR_4 = H'60
TCR_5 = H'20
Set triggers for clearing of TCNT as follows
• TCNT_0 to TCNT_4 = synchronized clearing
• TCNT_5 = TGRA compare match/input capture
TIOR_5 = H'09
Other TIOR = H'52
Set PWM output pins
• TIOCA_5 pin:
– Input capture
• Other TIOC pins:
– Initial output 0
– Output 1 on compare match with TGRA or TGRC
– Output 0 on compare match with TGRB or TGRBD
TGRA_0, TGRC_0, TGRA_1, TGRA_2, TGRA_3, TGRC_3, TGRA_4
Set the duty value: (set_dly[0] to [6])
TGRB_0, TGRD_0, TGRB_1, TGRB_2, TGRB_3, TGRD_3, TGRB_4
Set the pulse reset value: (set_wid[0] to [6])
TSYR = H'3F
TPU0 to TPU5: Set for synchronized operation
TMDR_0 to TMDR4 = H'C2
TMDR_5 = H'C0
TPU_0 to TPU_4: Set to PWM mode 1
TPU_5: Normal operation
TSTR = H'3F
TPU_0 to TPU_5 = Start counting
End

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http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	May.18.07	—	First edition issued

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