
Summary

This application note describes how to configure the communications evaluation unit for the use of the various peripheral modules of the EC-1 LSI chip for industrial Ethernet communications.

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1. Overview

1.1 Overview

This application note describes the usage of the communications evaluation board for the EC-1 (TS-EC-1-COM made by TESSERA TECHNOLOGY INC.).

This board includes the interfaces listed below for use in evaluating communications by the EC-1.

- EtherCAT[®]
- USB
- I²C
- CSI
- SPI
- RS-485
- CAN
- JTAG
- General-purpose ports
- Others (extension connectors)

1.2 Overall Block Diagram

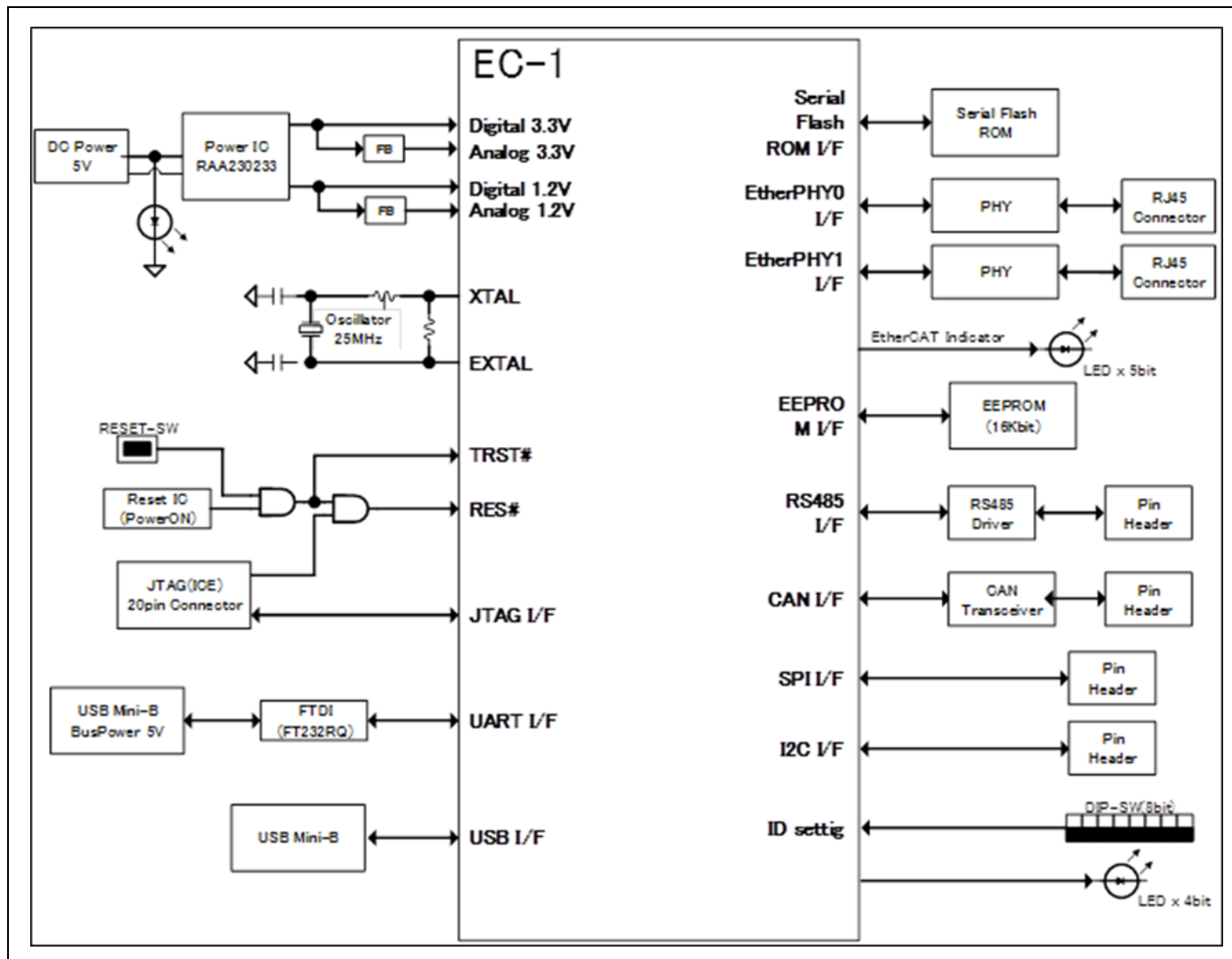


Figure 1.1 Overall Block Diagram

2. General Specifications

2.1 Electrical Specifications

This section gives the electrical and other specifications of this product in a set of tables.

Item		Specifications
Power supply	Rated voltage	DC 5 V
	Range of voltage tolerance	DC 4.75 V to 5.25 V
	Current drawn internally	100 mA or less
	Status LED (POWER)	Green

2.2 Environmental Specifications and Mass

Item		Specifications
Physical environment	Ambient temperature for operation	0 to 55°C
	Ambient temperature for storage	-25 to 70°C
	Ambient humidity for operation	30 to 90% RH (no condensation)
	Ambient humidity for storage	30 to 90% RH (no condensation)
	Atmosphere for operation	No corrosive gas
Mass	—	Approximately 180 g
Board dimensions	—	83 (W) × 74 (H) (not including protrusions)

2.3 Communications Specifications

Item	Specifications
Communications protocols	EtherCAT
Communications control IC	EC-1
EtherCAT PHY	TLK105 from TI
Communications method	IEEE 802.3u (100Base-TX)
Form of isolation	Pulse-transformer isolation
Status LEDs	RUN (green), ERR (red) L/A IN (green), L/A OUT (green) STAT (green/read)
External interfaces	RJ-45 × 2

3. Names and Functions of Parts

3.1 Clock

The EC-1 system clock (25 MHz) is supplied by this board.

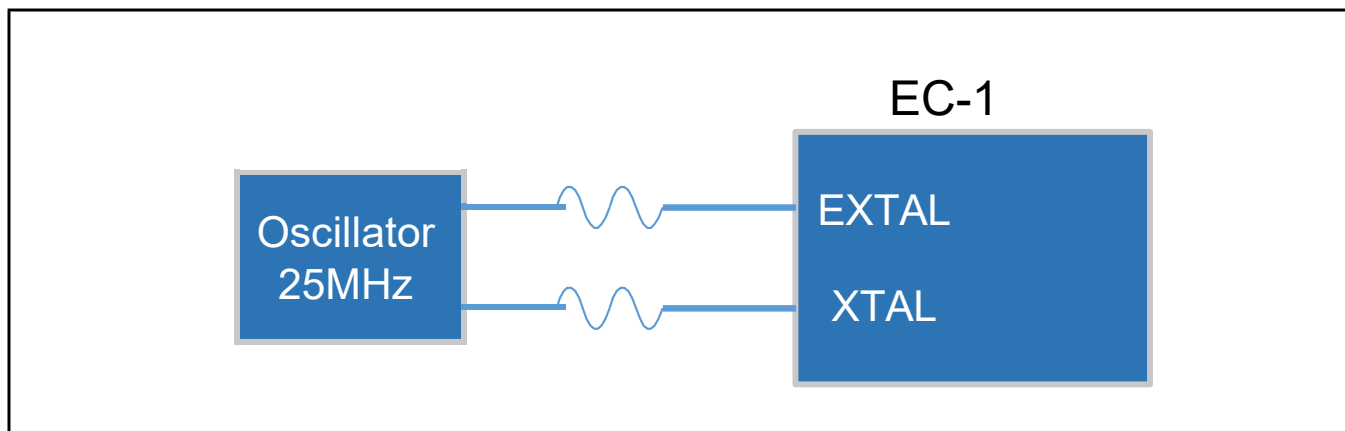


Figure 3.1 System clock supply

3.2 Communications Section

EtherCAT Communication connector (ECATIN, ECATOUT) IEEE802.3u

#8 pin

#1 pin

8	NC
7	NC
6	RXD-
5	NC
4	NC
3	RXD+
2	TXD-
1	TXD+

Conformity connector : RJ-45connector
 Conformity cable : Double shielded cable

Figure 3.2 EtherCAT Communications Connectors

3.3 Power Supply and Peripheral Pins

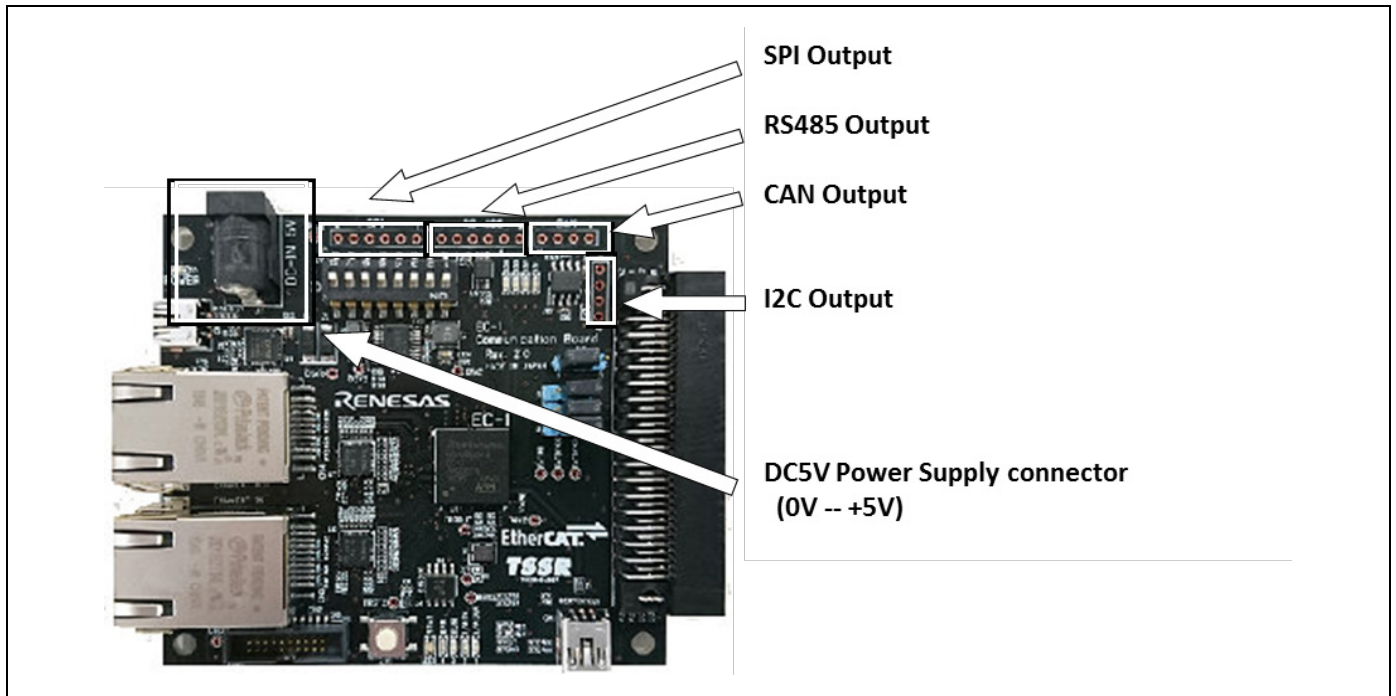


Figure 3.3 Power Supply and I/O Connectors

3.3.1 CAN I/F pins

These pins function as the pin headers for the CAN interface.

Table 3.1 CAN I/F (J4 FFC-4AMEP1)

Pin No.	I/O	Signal Name
1	—	+5 V
2	I/O	CANH
3	—	FG
4	I/O	CANL

3.3.2 RS 485 I/F pins

These pins function as the pin headers for the RS-485 interface.

Table 3.2 RS485 I/F (J1 FFC-6AMEP1)

Pin No.	I/O	Signal Name
1	—	+5 V
2	Output	A
3	Output	B
4	Input	Z
5	Input	Y
6	—	GND

3.3.3 SPI I/F pins

These pins function as the pin headers for the SPI.

Table 3.3 SPI I/F (J7 FFC-6AMEP1)

Pin No.	I/O	Signal Name
1	Clocks	RSPCK
2	I/O	MISO0
3	I/O	MOSI0
4	I/O	SSL00
5	I/O	SSL01
6	I/O	SSL02

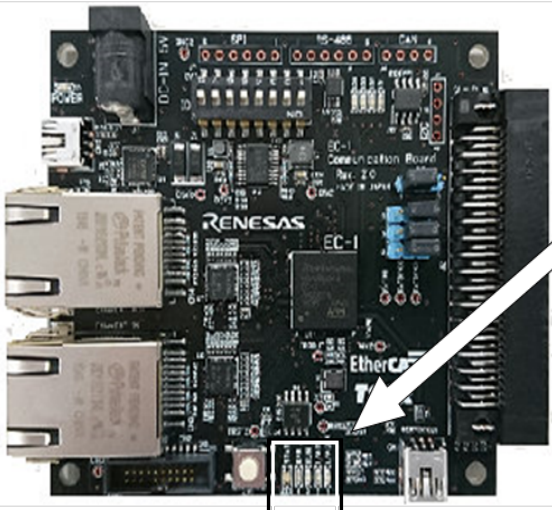
3.3.4 I2C I/F pins

These pins function as the pin headers for the I²C.

Table 3.4 I²C I/F (J9 FFC-4AMEP1)

Pin No.	I/O	Signal Name
1	—	+3.3 V
2	SCL1	SCL1
3	SDA1	SDA1
4	—	GND

3.4 Status LEDs



Communication Status LED

RUN
 Operation : Turn on
 Safe Operation : Single flash
 Pre Operation : Blinking
 Initialization : Turn off

L/A IN
 Link up operation : Flickering
 Physical layer link up : Turn on
 Physical layer non-link up : Turn off

L/A OUT
 Link up operation : Flickering
 Physical layer link up : Turn on
 Physical layer non-link up : Turn off

ERR
 WD Time Out : Double flash
 Sync or Communication data are abnormal : Single flash
 Communication setting is abnormal : Invalid configuration
 Normal operation : Turn off

STAT (RUN+ERR)
 Operation : Turn on
 Sync or Communication data are abnormal : Single flash
 Safe Operation : Single flash
 Pre Operation : Blinking
 Initialization : Turn off

Figure 3.3 Communications Status LEDs

The EtherCAT slave controller (ESC) controls lighting of the status LEDs.

Table 3.5 EtherCAT Status LEDs

Pin No.	I/O	Signal Name
CATLINKACT1	Output	LED1
CATLINKACT0	Output	LED2
CATLEDRUN	Output	LED3
CATLEDERR	Output	LED4
CATLEDSTER	Output	LED5

3.5 Power supply, General-Purpose LEDs

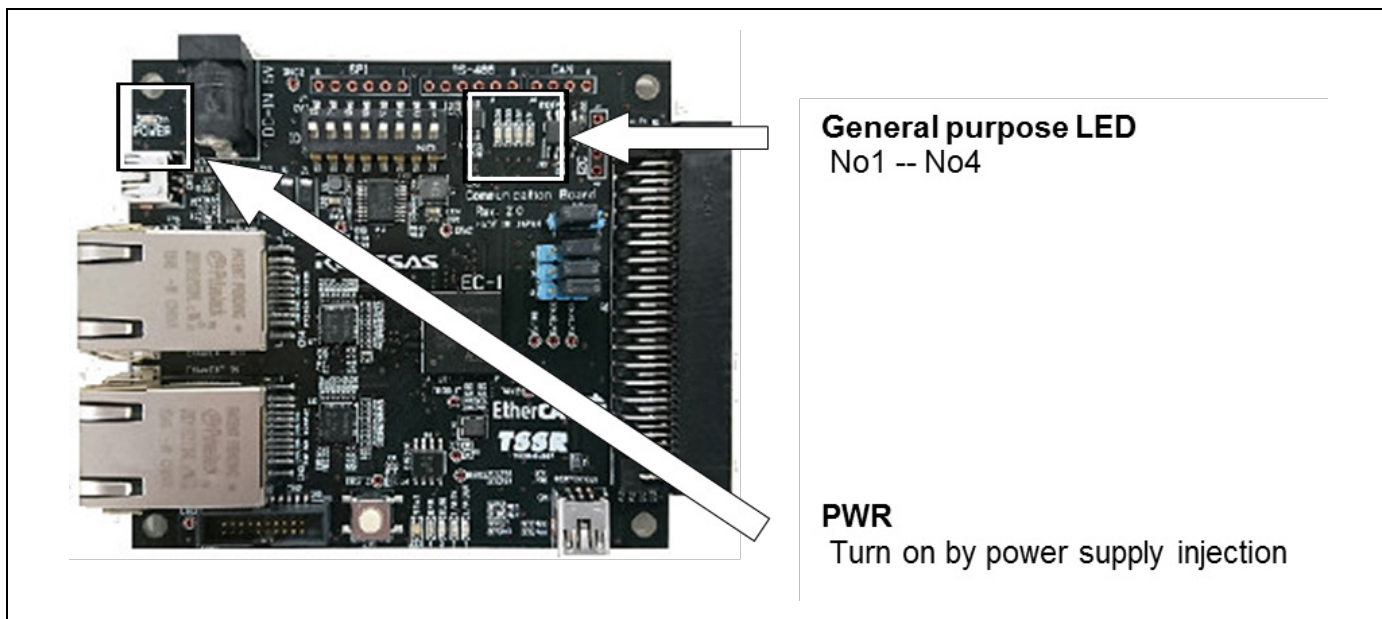


Figure 3.4 Power-Supply and General-Purpose LEDs

3.5.1 Power supply LEDs

The power for various devices is generated by the input of 5-V DC through a DC jack or via the USB. When 5.0 V is supplied, the POWER_LED lights up in green.

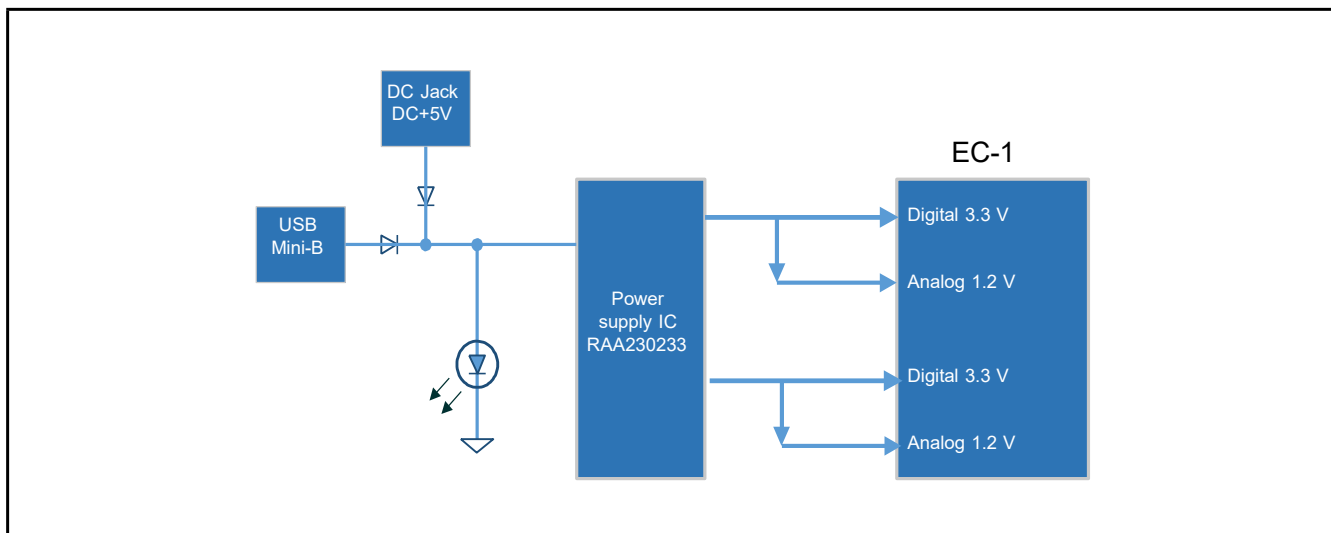


Figure 3.5 Power-Supply Connection

3.5.2 General-Purpose LEDs

Table 3.6 General-Purpose LEDs

Pin No.	I/O	Signal Name
PS3	Output	LD1
PS2	Output	LD2
PS1	Output	LD3
PS0	Output	LD4

3.6 DIP Switch Block

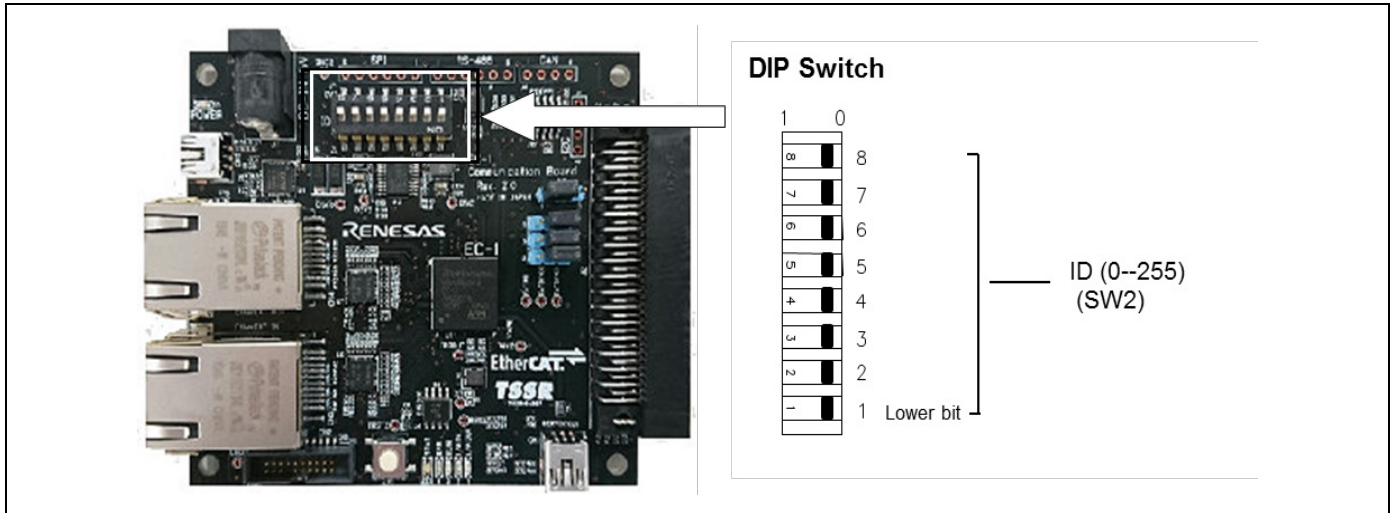


Figure 3.6 DIP Switch Block

The DIP switches of SW2 are used to set the node ID (0 to 255).

Table 3.7 DIP Switches (SW2)

Switch No.	Name of EC-1 Signal	Function
SW2-1	PE0	ID SW2-1
SW2-2	PE1	ID SW2-2
SW2-3	PE2	ID SW2-3
SW2-4	PE3	ID SW2-4
SW2-5	PE4	ID SW2-5
SW2-6	PE5	ID SW2-6
SW2-7	PE6	ID SW2-7
SW2-8	PE7	ID SW2-8

3.7 Debugging Connector and Push Switch

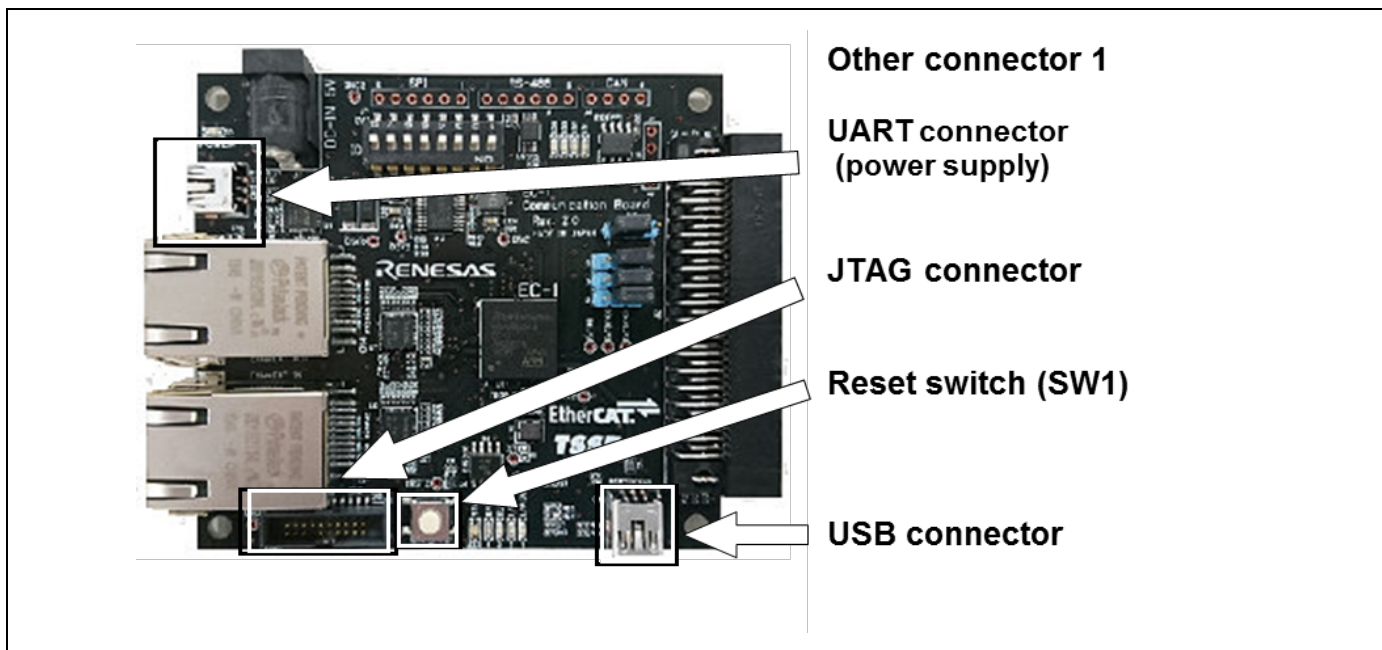


Figure 3.7 Push Switch and Other Connectors on the Board

3.7.1 Reset switch(SW1)

This push switch generates a reset of the EC-1 and its I/O pins.

3.7.2 JTAG connector (CN2)

This is a half-pitch connector having JTAG-20 pins for debugging. Connector: SHF-110-01-L-D-TH

Table 3.8 JTAG CN2

Pin No.	Signal Name	Pin No.	Signal Name
1	VRef	2	TMS
3	GND	4	TCK
5	GND	6	TDO
7	—	8	TDI
9	GND	10	RESET
11	GNDcap	12	GND
13	GNDcap	14	GND
15	GND	16	GND
17	GND	18	GND
19	GND	20	GND

3.7.3 UART connector (CN5)

This is a USB Mini-B type connector for the USB interface to be used as a UART.

Table 3.9 **UART CN5**

Pin No.	Signal Name
1	VBUS
2	-D
3	+D
4	ID
5	GND

3.7.4 USB connector (CN1)

This is a USB Mini-B type connector for the USB interface.

Table 3.10 **USB CN1**

Pin No.	Signal Name
1	VBUS
2	USB_DM
3	USB_DP
4	GND
5	GND

3.8 Jumper Blocks

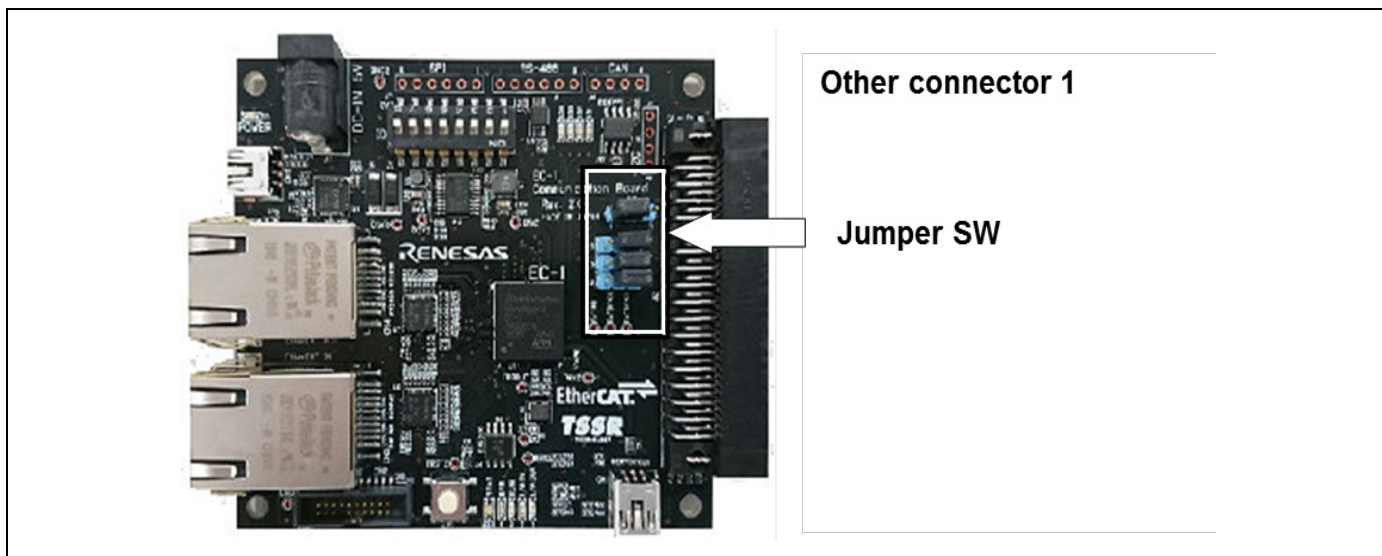


Figure 3.8 Jumper Blocks

The jumper blocks are used to switch the signal lines on the EC-1 communications board. Switching jumpers enables the output to the combination connector and the switching of peripheral functions.

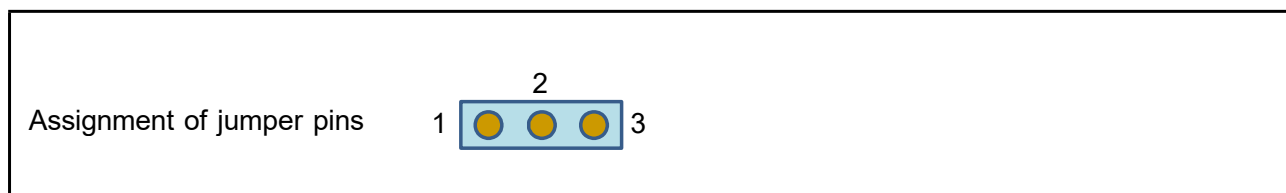


Figure 3.9 Jumper Pin Assignment

3.8.1 Switching of EtherCAT Interrupts and GPIO Outputs to the Combination Connector

Board silkscreen mark: J3

Connector: Jumper

Part type number: FFC-3AMEP1

Table 3.11 Jumper Pin J3

Jumper Connection	Function
1-2	CATSYNC0
2-3	P74

Default: Short-circuit 2-3

3.8.2 Switching of EtherCAT Interrupts and GPIO Outputs to the Combination Connector

Board silkscreen mark: J5

Connector: Jumper

Part type number: FFC-3AMEP1

Table 3.12 Jumper Pin J5

Jumper Connection	Function
1-2	CATSYNC1
2-3	P73

Default: Short-circuit 2-3

3.8.3 Switching of EtherCAT Interrupts and GPIO Outputs to the Combination Connector

Board silkscreen mark: J6

Connector: Jumper

Part type number: FFC-3AMEP1

Table 3.13 Jumper Pin J6

Jumper Connection	Function
1-2	CATIRQ
2-3	P72

Default: Short-circuit 2-3

3.8.4 Switching between SPI and I²C

Board silkscreen mark: J10

Connector: Jumper

Part type number: FFC-3AMEP1

Table 3.14 Jumper Pin J10

Jumper Connection	Function
1-2	I2C (SCL1)
2-3	USB (VBUSIN)

Default: Short-circuit 2-3

3.9 Combination Connector

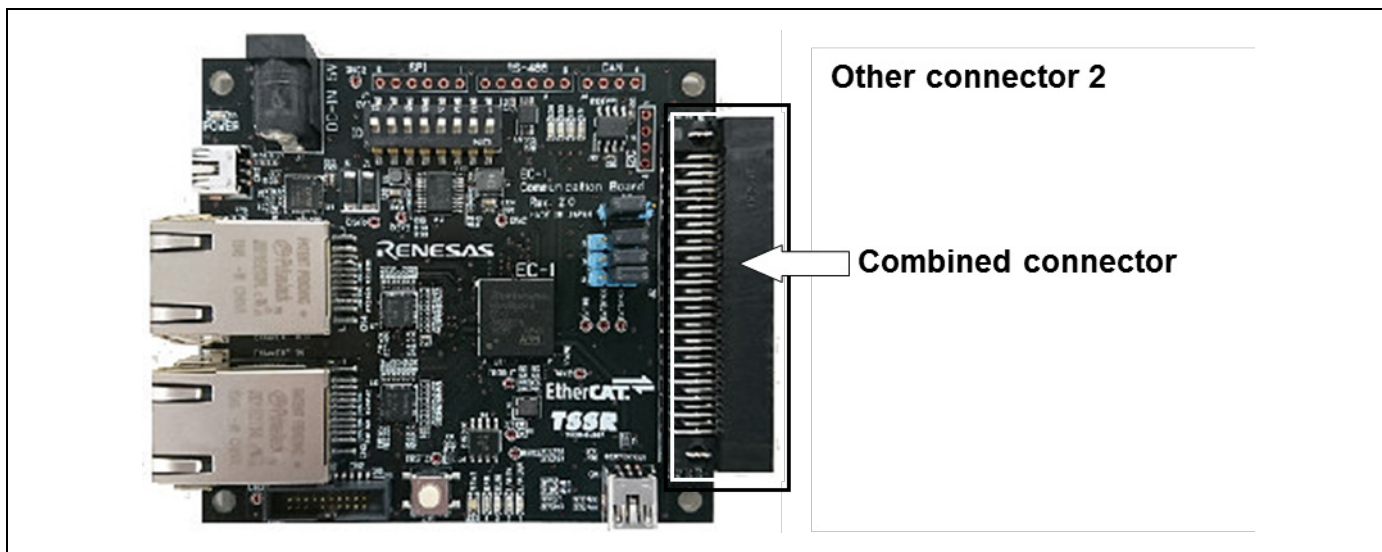


Figure 3.10 Combination Connector

The combination connector is used to connect an external device to the EC-1 communications board. This enables the connection of an external microcontroller to the I/O board.

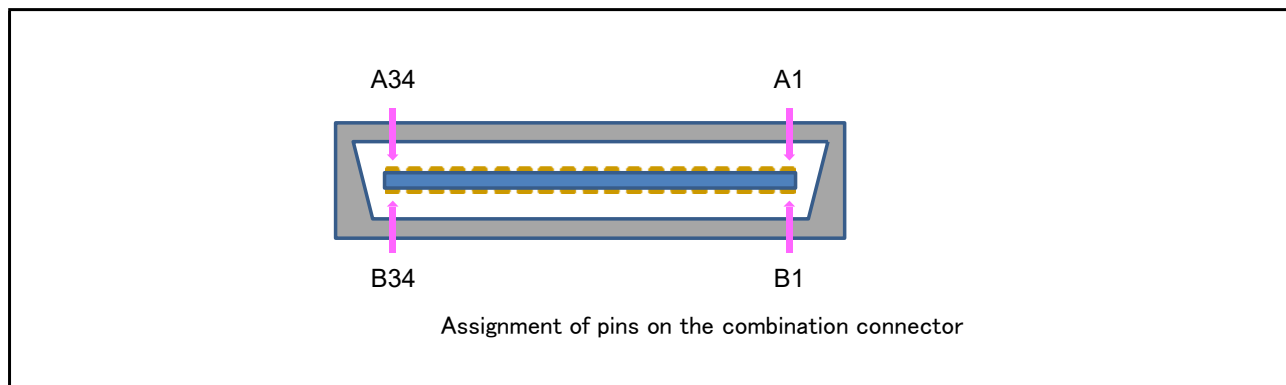


Figure 3.11 Combination Connector Assignment

Table 3.15 Assignment on the Combination Connector

Pin No.	EC-1 Assignment	Pin No.	EC-1 Assignment
A1	—	B1	—
A2	—	B2	—
A3	—	B3	—
A4	—	B4	—
A5	—	B5	—
A6	—	B6	—
A7	P97	B7	—
A8	P44	B8	—
A9 (IRQ2)	P77	B9	—
A10 (IRQ3)	P76	B10	—
A11 (IRQ4)	P75	B11	P77/RSPCK0
A12 (IRQ5)	P74/CATSYNC0	B12	P75/SSL00
A13 (IRQ6)	P72/CATSYNC1	B13	PA1/MOSI0
A14 (IRQ7)	P72/CATIRQ	B14	PA0/MISO0
A15 (D8)	P71	B15	—
A16 (D9)	P70	B16	—
A17 (D10)	PA7	B17	—
A18 (D11)	PA6	B18	—
A19 (D12)	PA5	B19	—
A20 (D13)	PA4	B20	Reset
A21 (D14)	PA3	B21	—
A22 (D15)	PA2	B22	—
A23 (TPSA0)	PA1	B23	—
A24 (A1)	PA0	B24	—
A25	—	B25	—
A26	—	B26	—
A27	SSL10	B27	V3.3
A28	RSPCK1	B28	—
A29	MOSI1	B29	—
A30	MISO1	B30	—
A31	—	B31	GND
A32	—	B32	GND
A33	—	B33	GND
A34	—	B34	GND

3.10 Test Pins

TEST Pad

This is a list of pins connected to the pads from the EC-1 on this board.

The pads are $\phi 0.8$ -mm through holes.

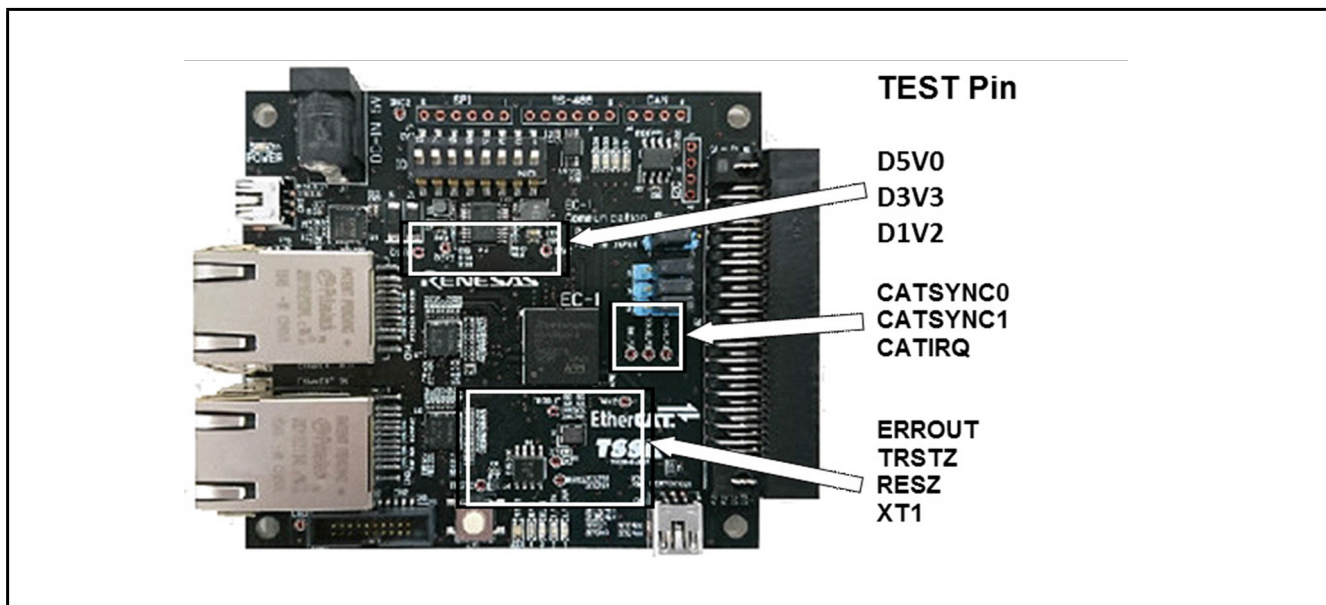


Figure 3.12 Test Pins

Table 3.16 List of Pins

Pin Name	Pad Name	Handling of Pins Connected to the Pads
PM3	CATSYNC0	—
PM2	CATSYNC1	—
PU7	CATIRQ	—
D5V	D5V0	—
D3.3V	D3V3	—
D1.2V	D1V2	—
ERROUT	ERROUT	—
TRST#	TRSTZ	—
RES#	RESZ	—
EXTAL	XT1	—
A1.2V	A1V2	—

4. Board Dimensions

This section describes the dimensions of the EC-1 communications board.

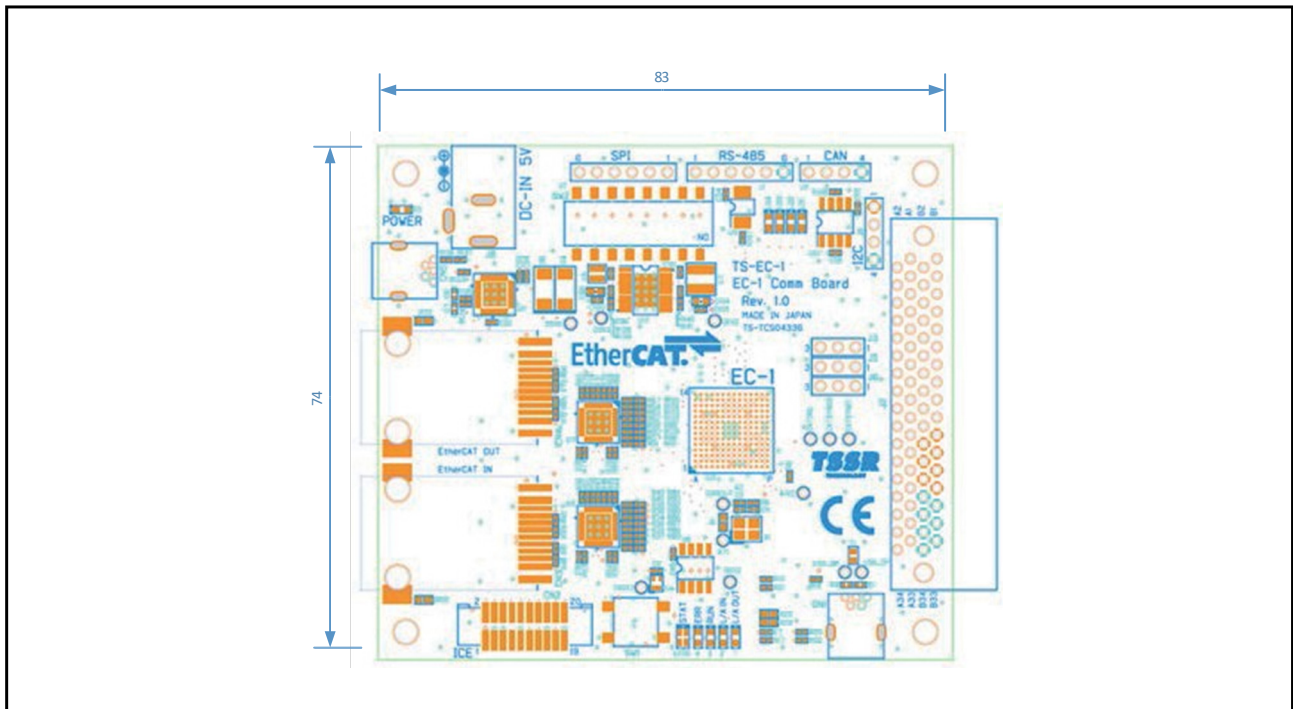


Figure 4.1 External Dimensions of the Board

5. Examples of Applications

The following are descriptions of examples of applications for use in evaluating the communications board.

5.1 External Access to the ESC via SPI

Access the ESC of the EC-1 is enabled externally from an external microcomputer.

This can be realized with reference to the following sample program and document.

Master: EC-1 Remote I/O Sample Program
 ESC H/W driver for access via the SPI
 Application Note (r01an3780ej0100)

Slave: EC-1 Communications Board Manual
 (this EC-1 Sample Program
 ESC H/W library for SPI access
 Application Note (r01an3780ej0100))

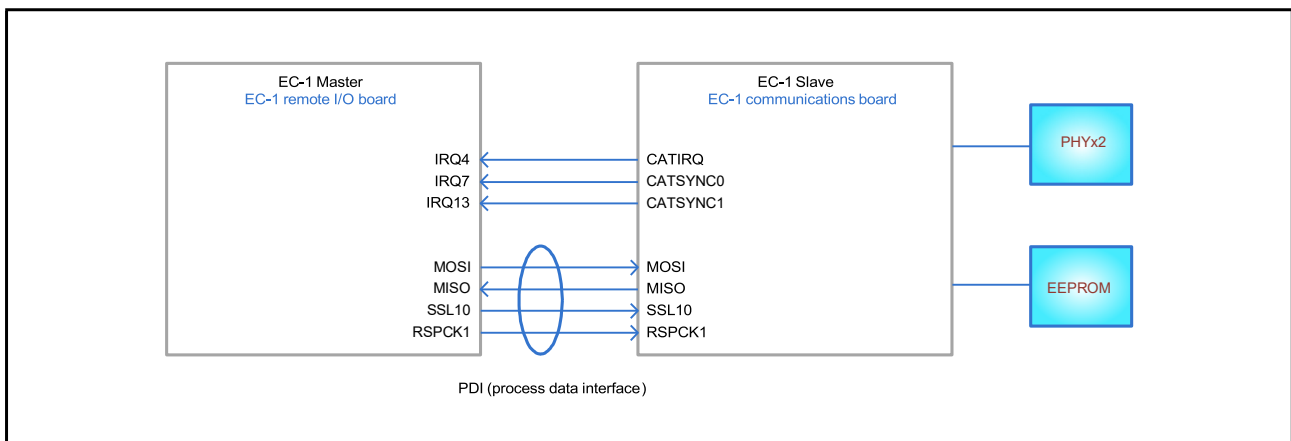


Figure 5.1 SPI Connections

6. Website and Support

Renesas Electronics website

<http://japan.renesas.com/>

Inquiries

<http://japan.renesas.com/contact/>

Revision History	Application Note: EC-1 Series Communications Board
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Rev.	Date	Description	
		Page	Summary
1.00	Mar. 22, 2017	-	First Edition issued
1.10	Sep. 17, 2018	-	Add trademark

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1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

— The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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