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SH7211 Group

DMAC Dual Address Mode

Introduction

This application note provides an example of DMA transfer by means of the dual address mode of the direct memory access controller (DMAC) incorporated in the SH7211.

Target Device

SH7211

Contents

1. Introduction

1.1 Specification

- DMA transfer from the on-chip RAM to external SDRAM is performed on DMAC channel 0 in dual address mode.
- Auto request mode is used to request the DMAC to transfer for five sets of 32-bit data (total 20 bytes).

1.2 Module Used

- Direct memory access controller (DMAC channel 0)

1.3 Applicable Conditions

- Microcontroller: SH7211
- Operating Frequency: Internal clock 160 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
- C Compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01,
  from Renesas Technology
- Compile Option: -cpu = sh2a -include = "$(WORKSPDIR)\inc"
  -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath
  -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo

1.4 Related Application Note

The sample program of this application note has been evaluated with the initial settings described in the SH7211 Initialization Application Note. Refer to that application note for details.

2. Description of the Sample Application

This sample program uses the direct memory access controller (DMAC) to perform DMA transfer from the on-chip RAM to external SDRAM in dual address mode.

2.1 Overview of Operations by the Module Used

In dual address mode, both the transfer source and destination are accessed (selected) by an address. The transfer source and destination can be located externally or internally. DMA transfer requires two bus cycles because data are read from the transfer source in a data read cycle and written to the transfer destination in a data write cycle. After the read cycle, the data for transfer are temporarily stored in the DMAC. For example in transfer between external memories, data are read to the DMAC from one region of external memory in a data read cycle, after which data are written to the other region of external memory in a data write cycle.

The flow of data in dual mode is illustrated in figure 1. A block diagram of the DMAC is shown in figure 2. The settings of the DMAC are listed in table 1.

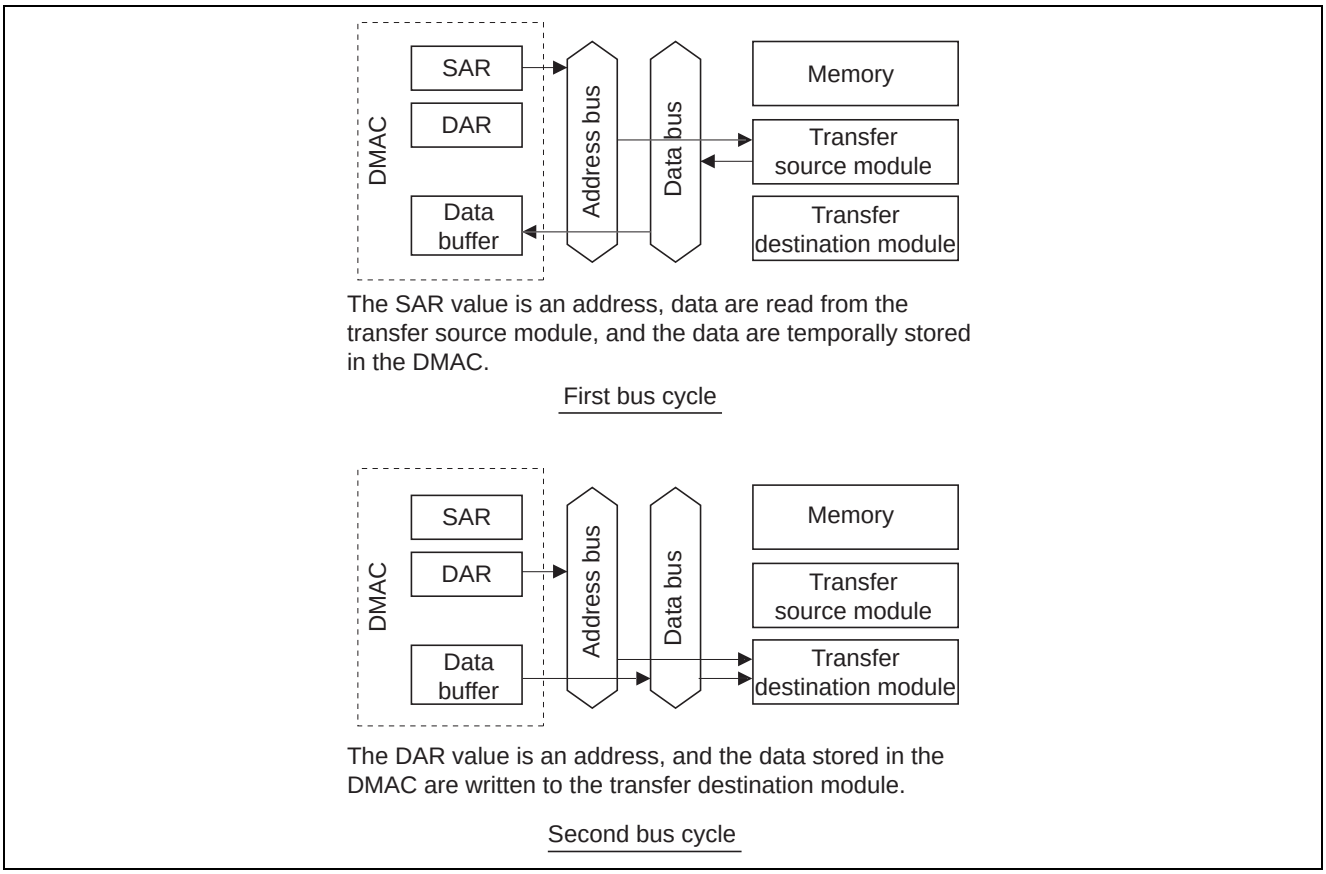
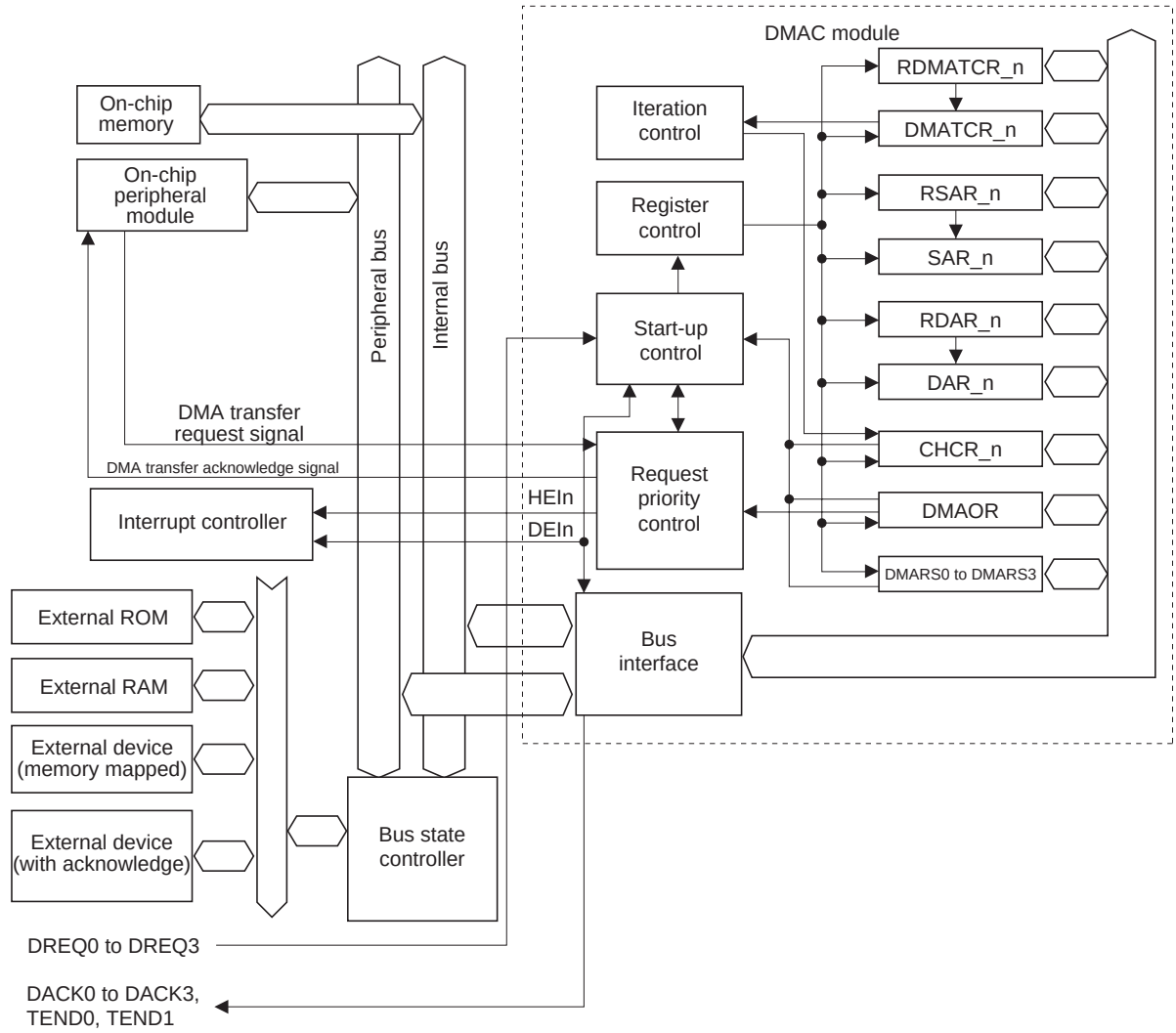


Figure 1 Flow of Data in Dual Address Mode

Table 1 Settings of DMAC

Item	Setting
Address mode	Dual address
Transfer request	Auto request (transfer requests are made by software)
Transfer count	5 transfers (20 bytes of data in total are transferred)
Bus mode	Burst mode
Transfer source address	On-chip RAM (automatic incrementation according to the data size after each transfer)
Transfer destination address	SDRAM (H'0C00 0000) in the CS3 space (automatic incrementation according to the data size after each transfer)
Transfer data size	Longword (32 bits)
Interrupt	Transfer end interrupt enabled

Note For details on the DMAC, refer to the section on the direct memory access controller (DMAC) in the SH7211 Group Hardware Manual.



[Legend]

RDMATCR:	DMA reload transfer count register	CHCR:	DMA channel control register
DMATCR:	DMA transfer count register	DMAOR:	DMA operation register
RSAR:	DMA reload source address register	DMARS0 to DMARS3:	DMA extension resource selectors 0 to 3
SAR:	DMA source address register	HEIn:	DMA transfer half-end interrupt request to the CPU
RDAR:	DMA reload destination address register	DEIn:	DMA transfer end interrupt request to the CPU
DAR:	DMA destination address register	n:	0, 1, 2, 3, 4, 5, 6, 7

Figure 2 Block Diagram of the DMAC

2.2 Procedure for Setting the Module to be Used

This section describes the procedure for specifying initial settings for operating the DMAC in dual address mode. Auto request mode is used for requesting transfer. A flowchart of the DMAC initialization is shown in figure 3. For details on registers, refer to the SH7211 Group Hardware Manual.

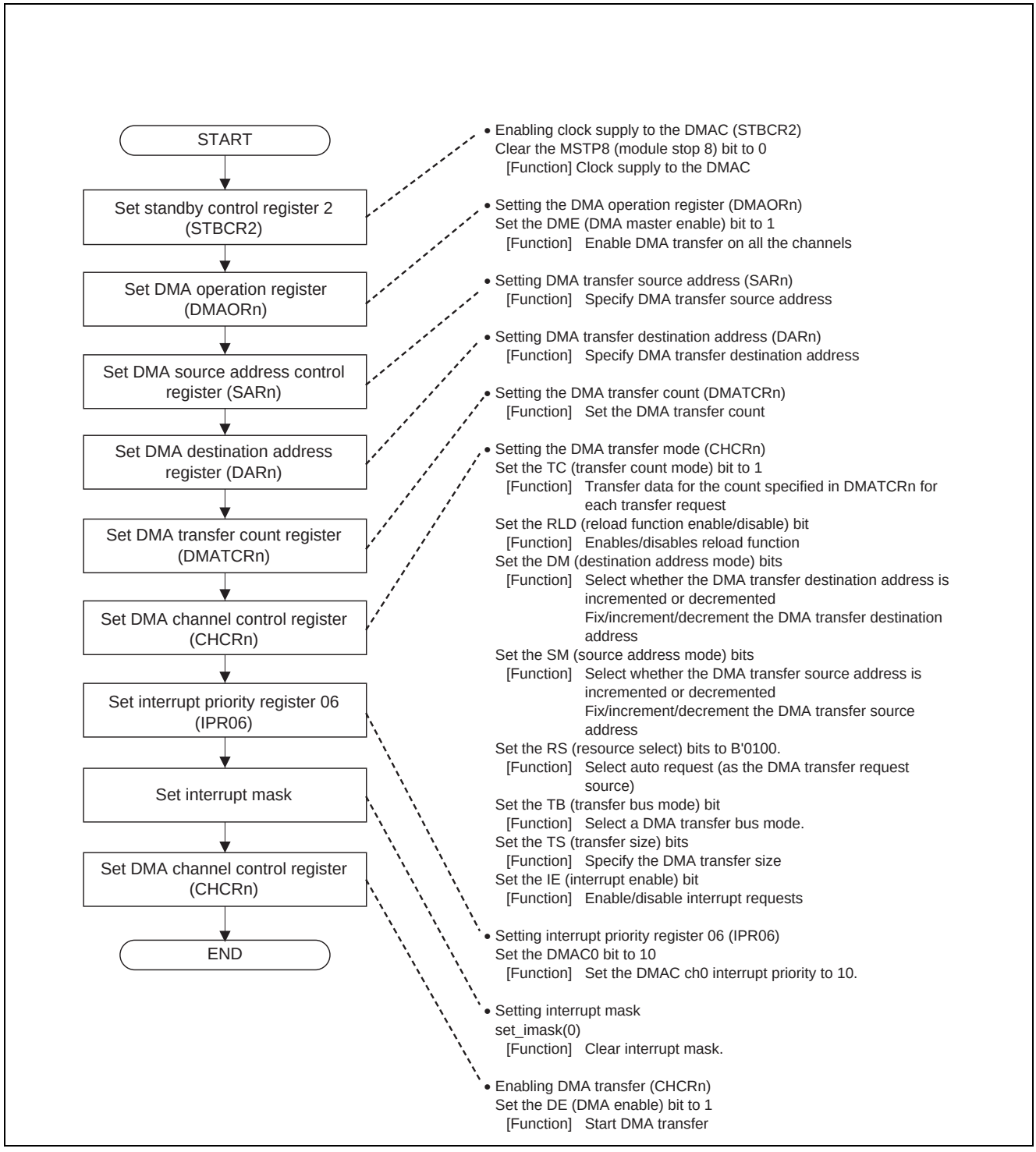


Figure 3 Flowchart of Initializing DMAC

2.3 Operation of the Sample Program

The operation of the sample program is described in figure 4 and table 2.

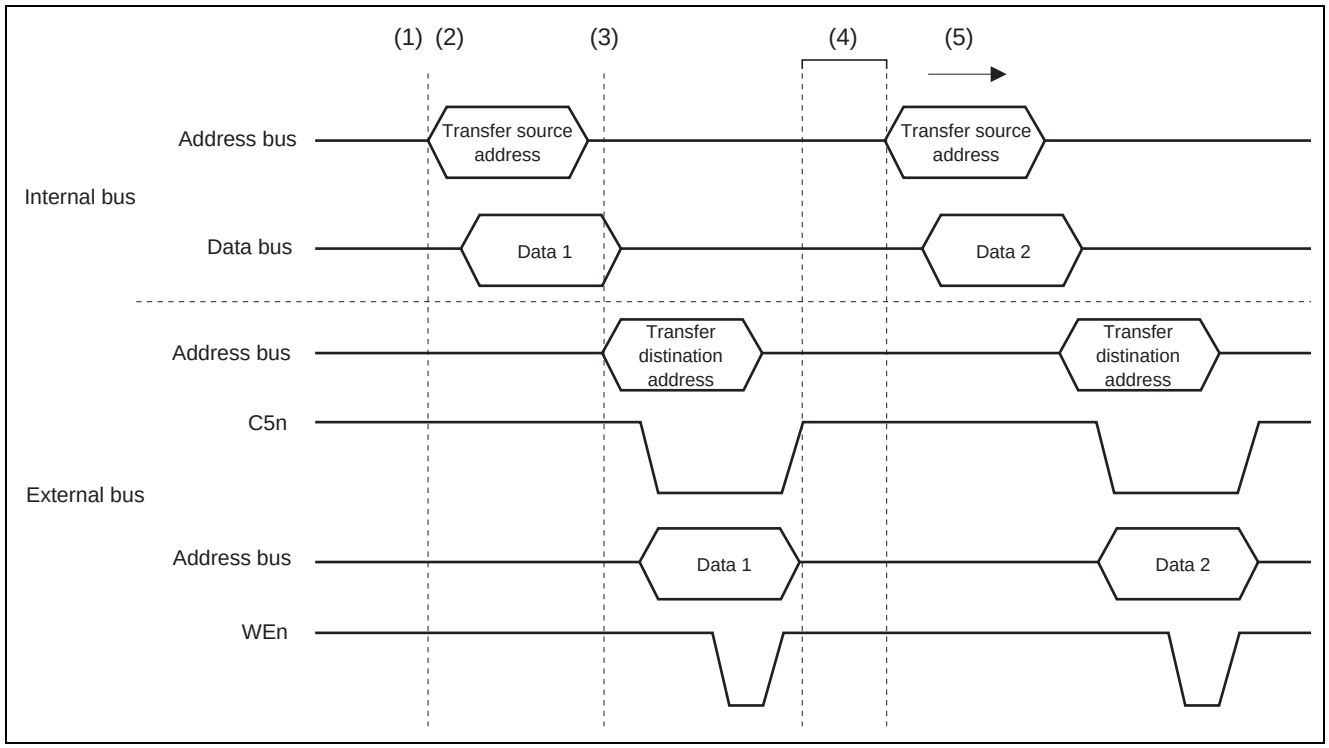


Figure 4 Operation in Dual Address Mode

Table 2 Processing

	Software Processing	Hardware Processing
(1)	Setting the DE bit in CHCR0 to 1 after all the other settings have been specified. (starts DMAC0 operation)	Output of the transfer source address to the internal address bus
(2)	—	Output of data from the on-chip RAM to the internal data bus
(3)	—	Output of CSn and WEn signals, address, and data to the external bus
(4)	—	Incrementing SAR0 and DAR0
(5)	—	Repeating until DMATCR0 becomes 0

2.4 Usage Notes on Sample Program

In this sample program, addresses where the source and destination areas for transfer start are specified as absolute addresses for clarity. Ensure that sections used by the user program do not overlap with the source and destination regions that start from the absolute addresses.

2.5 Processing Procedure of Sample Program

In the sample program, DMA transfer of 20-byte data from the on-chip RAM to external SDRAM is performed, after which transfer end interrupt processing is performed to disable DMA transfer.

The register settings for the sample program are listed in table 3. Also, a flowchart of the sample program is shown in figure 5.

Table 3 Register Settings for Sample Program

Register Name	Address	Setting Value	Description
Standby control register 2 (STBCR2)	H'FFFE 0018	H'00	MSTP8="0": DMAC operates
DMA channel control register 0 (CHCR0)	H'FFFE 100C	H'0000 5474	TC = "0": Transfer data once per DMA request RLD = "0": Disable reload function DM = "B'01": Increment the destination address SM = "B'01": Increment the source address RS = "B'0100": Auto request TB = "1": Burst mode TS = "B'10": Longword transfer IE = "1": Enable interrupt requests
		H'0000 5475	DE = "1": Enable DMA transfer
		H'0000 5470	IE = "0": Disable interrupt requests TE = “0” Clear the transfer end flag DE = "0": Disable DMA transfer
DMA source address register 0 (SAR0)	H'FFFE 1000	Address of transfer source data	Start address of the transfer source: Set to an address in the on-chip RAM area
DMA destination register_0 (DAR0)	H'FFFE 1004	H'0C00 0000	Start address of the transfer destination: Set to an address in the external memory area*
DMA transfer count register_0 (DMATCR0)	H'FFFE 1008	H'05	Transfer count: 5 transfers
DMA operation register (DMAOR)	H'FFFE 1200	H'0001	DME = "1": Enable DMA transfer on all channels
DMA extension resource selector_0 (DMARS0)	H'FFFE1300	H'0000	Not used for auto request

Note: * Addresses in external memory areas vary with the target board.

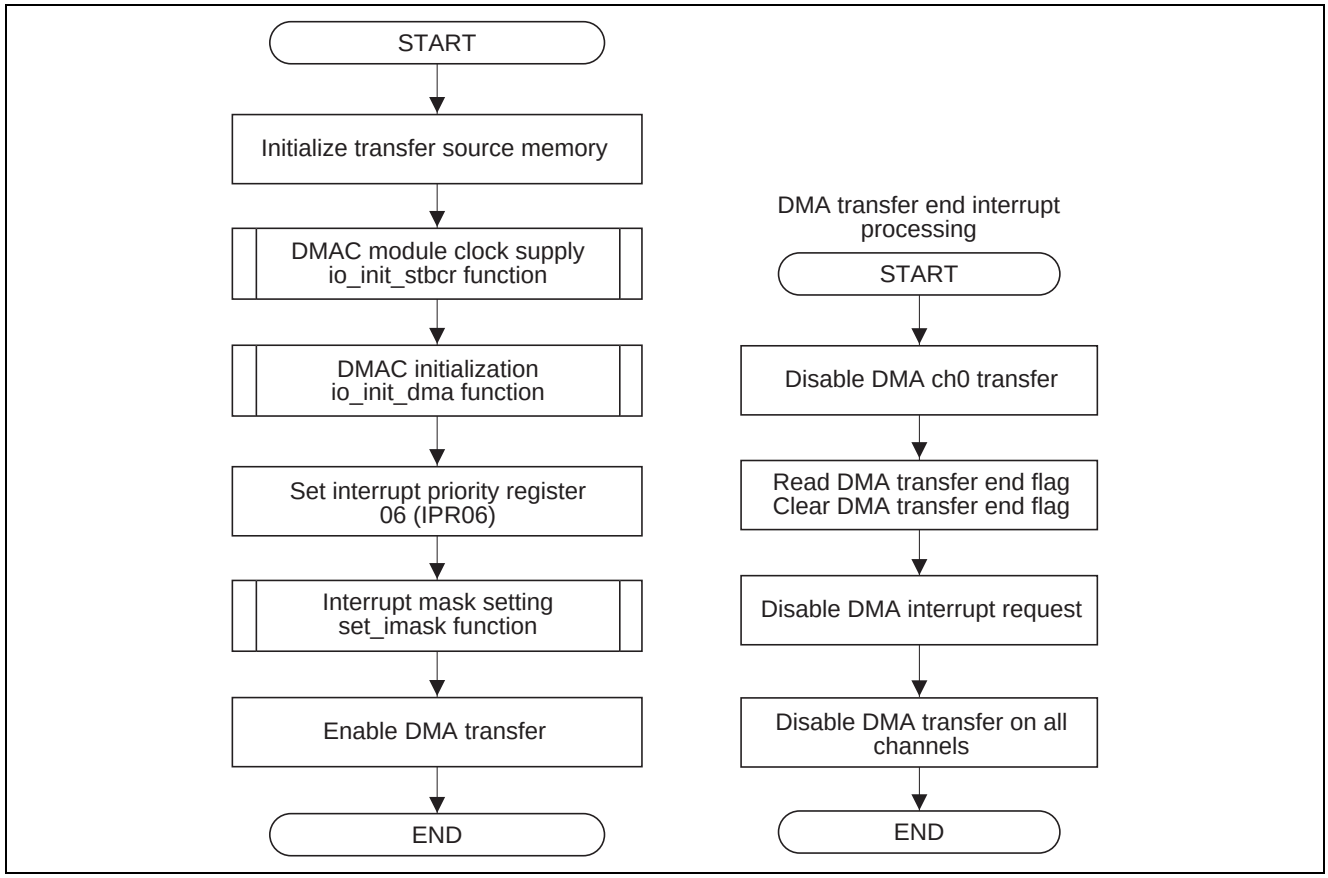


Figure 5 Flowchart of the Sample Program

3. Sample Program

1. Sample Program Listing: "main.c" (1)

```
1       /*""FILE COMMENT""*****************************************************************
2       *
3       *       System Name : SH7211 Sample Program
4       *       File Name   : main.c
5       *       Contents    : DMA dual address mode sample program
6       *       Version     : 1.00.00
7       *       Model       : M3A-HS11
8       *       CPU         : SH7211
9       *       Compiler    : SHC9.1.1.0
10      *       note        : DMA transfer from the on-chip RAM to externally connected
11      *                     SDRAM is performed using the DMAC. Auto request mode is used
12      *                     for requesting the DMAC to transfer 5 sets of 32-bit data
13      *                     (total 20 bytes).
14      *
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22      *
23      *       history   : 2008.01.11 ver.1.00.00
24      *""FILE COMMENT END""*************************************************************/
25      #include <machine.h>
26      #include "iodefine.h"               /* SH7211 iodefine  */
27
28
29      /* ==== prototype declaration ==== */
30      void main(void);
31      void io_init_stbcr(void);
32      void io_init_dma(unsigned long sar, unsigned long dar, unsigned long num);
33
34      /* ==== symbol definition ==== */
35      #define NUM 5
36      #define SDRAM_ADDR 0x0c000000       /* DMA source address(SDRAM) */
37
38      /* ==== RAM allocation variable declaration ==== */
39      unsigned long Data[NUM];
40
```

2. Sample Program Listing: "main.c" (2)

```
41      /*""FUNC COMMENT""*****************************************************
42       * Outline     : Sample program main
43       *-------------------------------------------------------------------
44       * Include     : #include "iodefine.h"
45       *             : #include <machine.h>
46       *-------------------------------------------------------------------
47       * Declaration : void main(void);
48       *-------------------------------------------------------------------
49       * Function    : Sample program main
50       *-------------------------------------------------------------------
51       * Argument    : void
52       *-------------------------------------------------------------------
53       * Return Value: void
54       *-------------------------------------------------------------------
55       * Notice      :
56       *""FUNC COMMENT END""************************************************/
57      void main(void)
58      {
59          /* ==== Transfer data setting ==== */
60          Data[0] = 0x11111111;
61          Data[1] = 0x22222222;
62          Data[2] = 0x33333333;
63          Data[3] = 0x44444444;
64          Data[4] = 0x55555555;
65
66          /* ==== Setting of power down mode ==== */
67          io_init_stbcr();
68
69          /* ==== Setting of DMAC ==== */
70          io_init_dma((unsigned long)&Data[0], SDRAM_ADDR, NUM);
71
72          /* ==== Setting of interrupt priority level ==== */
73          INTC.IPR06.BIT._DMAC0 = 10;
74
75          /* ==== Interrupt mask clear ==== */
76          set_imask(0);
77
78          /* ==== DMA transfer start ==== */
79          DMAC0.CHCR.BIT.DE = 1;
80
81          while(1){
82              /* loop */
83          }
84      }
85
```

3. Sample Program Listing: "main.c" (3)

```
/*""FUNC COMMENT""*************************************************************
 * Outline     : Release of module standby mode
 *-----------------------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *-----------------------------------------------------------------------------
 * Declaration : void io_init_stbcr(void);
 *-----------------------------------------------------------------------------
 * Function    : Release of module standby mode
 *-----------------------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------------------
 * Return Value: void
 *-----------------------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""*********************************************************/
void io_init_stbcr(void)
{
    /* ==== Setting of power down mode ==== */
    STB.CR2.BIT._DMAC = 0;            /* Release of the DMAC module standby mode */
}

/*""FUNC COMMENT""*************************************************************
 * Outline     : Setting of DMAC
 *-----------------------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *-----------------------------------------------------------------------------
 * Declaration : void io_init_dma(unsigned long sar, unsigned long dar,
 *             :                  unsigned long num);
 *-----------------------------------------------------------------------------
 * Function    : Setting of DMAC
 *-----------------------------------------------------------------------------
 * Argument    : unsigned long sar : transfer source address
 *             : unsigned long dar : transfer destination address
 *             : unsigned long num : transfer count
 *-----------------------------------------------------------------------------
 * Return Value: void
 *-----------------------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""*********************************************************/
void io_init_dma(unsigned long sar, unsigned long dar, unsigned long num)
{
    /* ==== Setting of DMAC ==== */
    /* ---- DMA operation register(DMAOR) ---- */
    DMAC.DMAOR.BIT.DME = 1;             /* DMA master enable */

    /* ---- DMA Source Address Register(SAR) ---- */
    DMAC0.SAR = (void *)sar;            /* DMA source address */

    /* ---- DMA Destination Address Register(DAR) ---- */
    DMAC0.DAR = (void *)dar;            /* DMA destination address */

    /* ---- DMA Transfer Count Register(DMATCR) ---- */
    DMAC0.DMATCR = num;                 /* DMA transfer count */

```

4. Sample Program Listing: "main.c" (4)

```
140         /* ---- DMA Channel Control Register(CHCR) ---- */
141         DMAC0.CHCR.LONG = 0x00005474;
142                 /* 15-14 = b'01  - Destination address is incremented       */
143                 /* 13-12 = b'01  - Source address is incremented            */
144                 /* 11-8  = b'0100- Auto request                             */
145                 /* 7-6   = b'01  - DREQ is detected at falling edge         */
146                 /* 5     = b'1   - Burst mode                               */
147                 /* 4-3   = b'10  - Longword unit(four bytes)                */
148                 /* 2     = b'1   - Interrupt request is enabled             */
149                 /* 1     = b'0   - Transfer End Flag                        */
150                 /* 0     = b'0   - DMA transfer is disabled                 */
151     }
152
153     /*""FUNC COMMENT""*****************************************************
154      * Outline     : DMA transfer end interrupt
155      *---------------------------------------------------------------------
156      * Include     : #include "iodefine.h"
157      *---------------------------------------------------------------------
158      * Declaration : void io_int_dma(void);
159      *---------------------------------------------------------------------
160      * Function    : 1. Disabling DMA transfer
161      *             : 2. Clearing the transfer end flag
162      *             : 3. Disabling interrupt requests
163      *             : 4. Disabling DMA transfer on all the channels
164      *             : 5. Dummy read
165      *---------------------------------------------------------------------
166      * Argument    : void
167      *---------------------------------------------------------------------
168      * Return Value: void
169      *---------------------------------------------------------------------
170      * Notice      :
171      *""FUNC COMMENT END""*************************************************/
172     void io_int_dma(void)
173     {
174     volatile unsigned long dummy;
175
176         DMAC0.CHCR.BIT.DE = 0x00; /* DE bit clear */
177
178         DMAC0.CHCR.BIT.TE = 0x00; /* TE bit clear */
179
180         DMAC0.CHCR.BIT.IE = 0x00; /* IE bit clear */
181
182         DMAC.DMAOR.BIT.DME = 0x00;/* DMA master disable */
183
184     dummy = DMAC0.CHCR.BIT.TE;
185     }
186     /* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7211 Group Hardware Manual
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