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April 1st, 2010
Renesas Electronics Corporation

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H8/300L Super Low Power Series

Division of 8-Digit BCD Numbers (DIVD)

Introduction

The software DIVD divides an 8-digit binary-coded decimal (BCD) number by another 8-digit BCD number and places the result (an 8-digit BCD number) in general-purpose registers.

Target Device

H8/38024

Contents

1. Arguments

Description		Memory area	Data length (bytes)
Input	Dividend	R0, R1	4
	Divisor	R2, R3	4
Output	Result of division (quotient)	R0, R1	4
	Result of division (remainder)	R4, R5	4
	Occurrence of error	Z flag (CCR)	—

2. Changes to Internal Registers and Flags

R0	R1	R2	R3	R4	R5	R6	R7
○	○	—	—	○	○	×	—

I	U	H	U	N	Z	V	C
—	—	×	—	×	○	×	×

Legend
—: No change
×: Undefined
○: Result

3. Specifications

Program memory (bytes)
84
Data memory (bytes)
0
Stack (bytes)
0
Clock cycle count
1162
Reentrant
Possible
Relocation
Possible
Interrupt
Possible

4. Notes

The clock cycle count (1162) in the specifications is for division of 99999999 by 9999.

5. Description

5.1 Details of functions

1. The following arguments are used with the software DIVD:
   R0: Sets the upper 4 digits of an 8-digit BCD dividend (32 bits long). After execution of the software DIVD, the upper 4 digits of the result of division (quotient) are placed in this register.
   R1: Sets the lower 4 bits of the 8-digit BCD dividend (32 bits long). After execution of the software DIVD, the lower 4 digits of the result of division (quotient) are placed in this register.
   R2: Sets the upper 4 digits of an 8-digit BCD divisor as an input argument.
   R3: Sets the lower 4 digits of the 8-digit BCD divisor as an input argument.
   R4: The upper 4 digits of an 8-digit BCD remainder are placed in this register as an output argument.
   R5: The lower 4 digits of the 8-digit BCD remainder are placed in this register as an output argument.
   Z flag (CCR): Indicates the occurrence of an error (division by 0) with the software DIVD as an output argument.
   Z flag = 1: The divisor was 0, indicating an error.
   Z flag = 0: The divisor was not 0.
2. The following figure illustrates the execution of the software DIVD. When the input arguments are set as shown in (1), the result of division is placed in the registers as shown in (2).

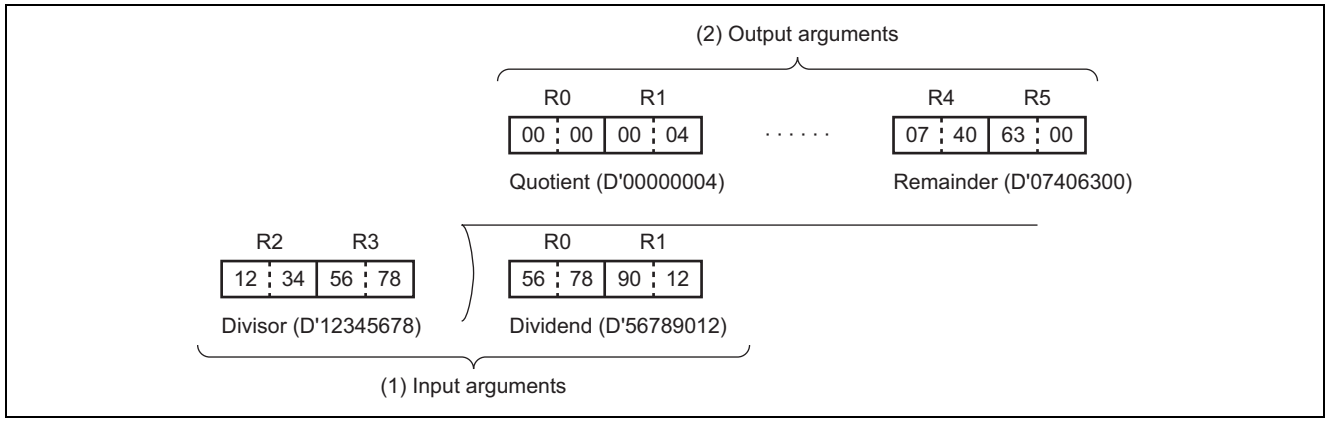


Figure 1 Example of Software DIVD Execution

3. Table 1 lists the result of division with 0 placed in input arguments.

Table 1 Result of Division with 0 Placed in Input Arguments

Input arguments		Output arguments		
Dividend (R0, R1)	**Divisor (R2, R3)**	**Quotient (R0, R1)**	**Remainder (R4, R5)**	**Error (Z)**
H'**** ****	H'0000 0000	H'**** ****	H'0000 0000	1
H'0000 0000	H'**** ****	H'0000 0000	H'0000 0000	0
H'0000 0000	H'0000 0000	H'0000 0000	H'0000 0000	1

Note: H'**** **** is a hexadecimal number.

5.2 Notes on usage

1. When the upper bits are not used (see figure 2), set them to 0; otherwise, a correct result cannot be obtained because division is done on the numbers including indeterminate data placed in the upper bits.

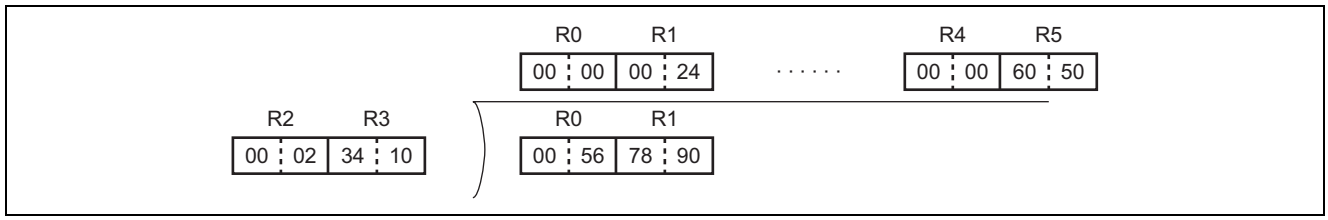


Figure 2 Example of Division with Upper Bits Unused

2. After execution of the software DIVD, the dividend will be lost because the quotient is placed in R0 and R1. When the dividend is still needed after software DIVD execution, save it in memory.

5.3 Data memory

The software DIVD uses no data memory.

5.4 Example of usage

Set a dividend and a divisor in the registers and call the software DIVD as a subroutine.

```
WORK1    . RES. W      2     ----------  Reserve a data memory area in which the user program places
                                         an 8-digit BCD dividend.

WORK2    . RES. W      2     ----------  Reserve a data memory area in which the user program places
                                         an 8-digit BCD divisor.

WORK3    . RES. W      2     ----------  Reserve a data memory area in which the user program places
                                         an 8-digit BCD quotient.

WORK4    . RES. W      2     ----------  Reserve a data memory area in which the user program places
                                         an 8-digit BCD remainder.
           .
           .
           .
         MOV. W        @WORK1, R0      -------  Place the 8-digit BCD dividend set by the user program
         MOV. W        @WORK1+2, R1             in the input argument (R0 and R1).

         MOV. W        @WORK2, R2      -------  Place the 8-digit BCD divisor set by the user program
         MOV. W        @WORK2+2 R3              in the input argument (R2 and R3).

       +-------------------------------+
       | JSR           @DIVD           | -------  Call the software DIVD as a subroutine.
       +-------------------------------+

         BEQ           ERROR           -------  Branch to the error (division by 0) processing routine
                                                when an error (division by 0) has occurred as a result of division.

         MOV. W R0,    @WORK3
         MOV. W R1,    @WORK3+2        -------  Place the result set in the output argument
         MOV. W R4,    @WORK4                   in the data memory of the user program.
         MOV. W R5,    @WORK4+2
           .
           .
           .
ERROR    +-------------------------------+
         | Dividion-by-0                 |
         | processing routine            |
         +-------------------------------+
```

5.5 Operation

1. Division of decimal numbers can be done by performing a series of subtractions.
   Figure 3 shows an example of division (64733088 ÷ 5).

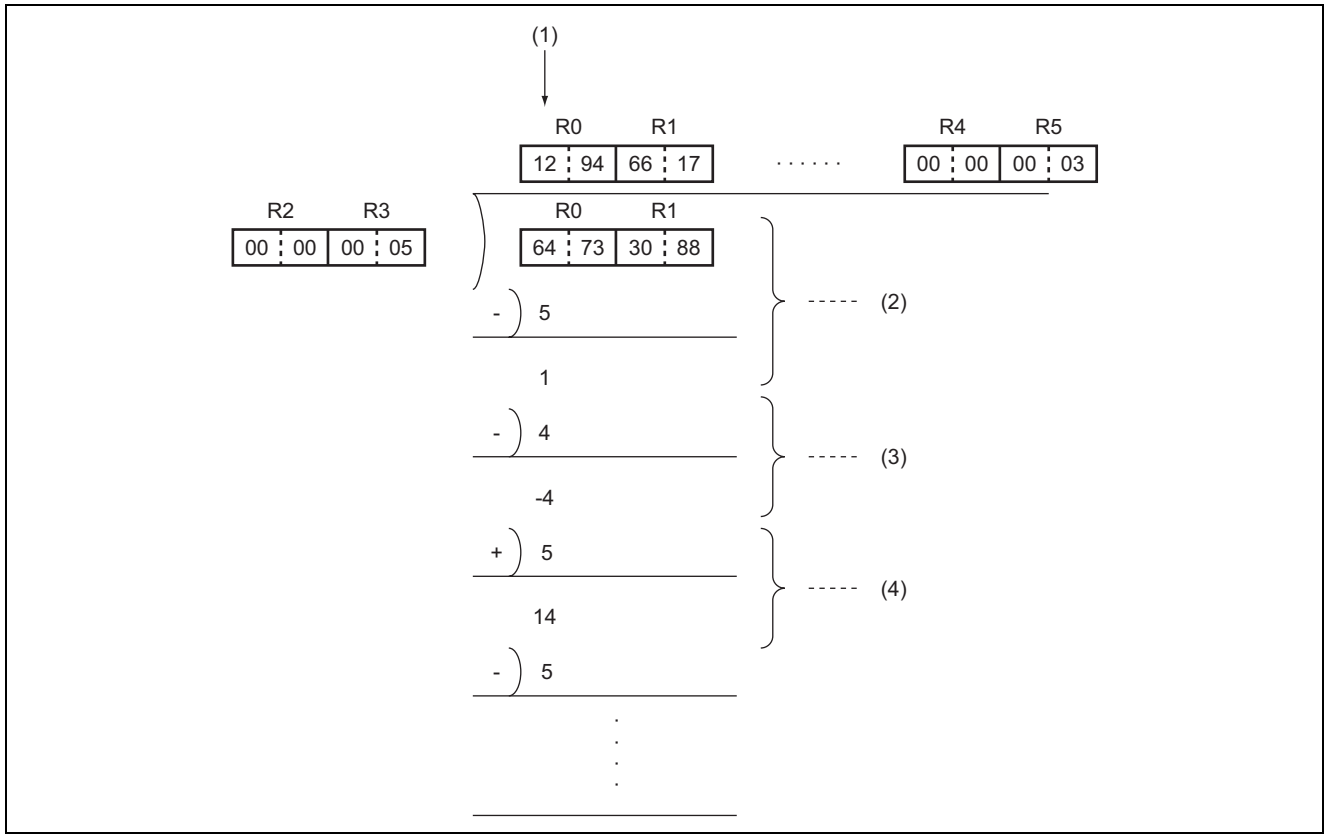
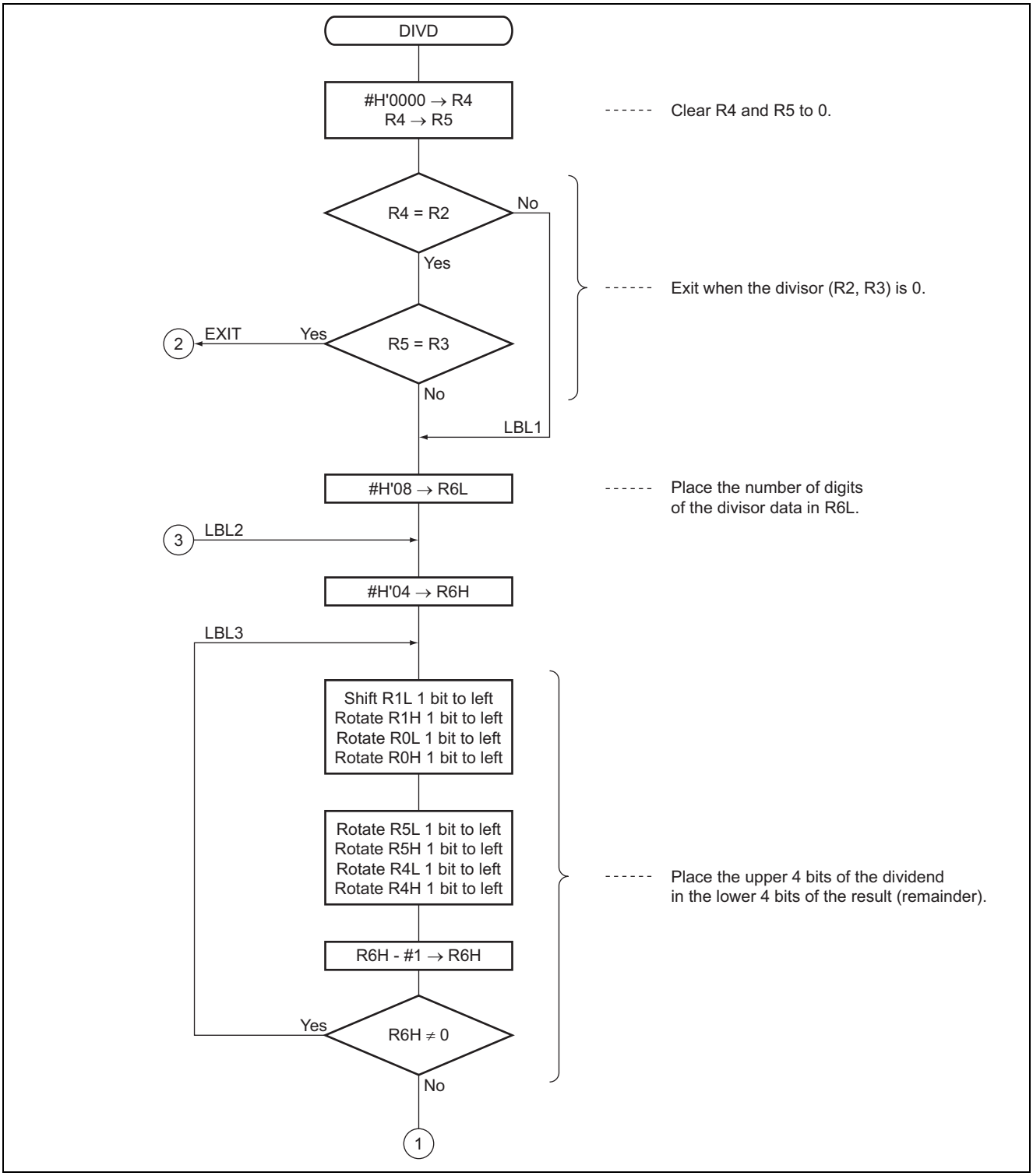
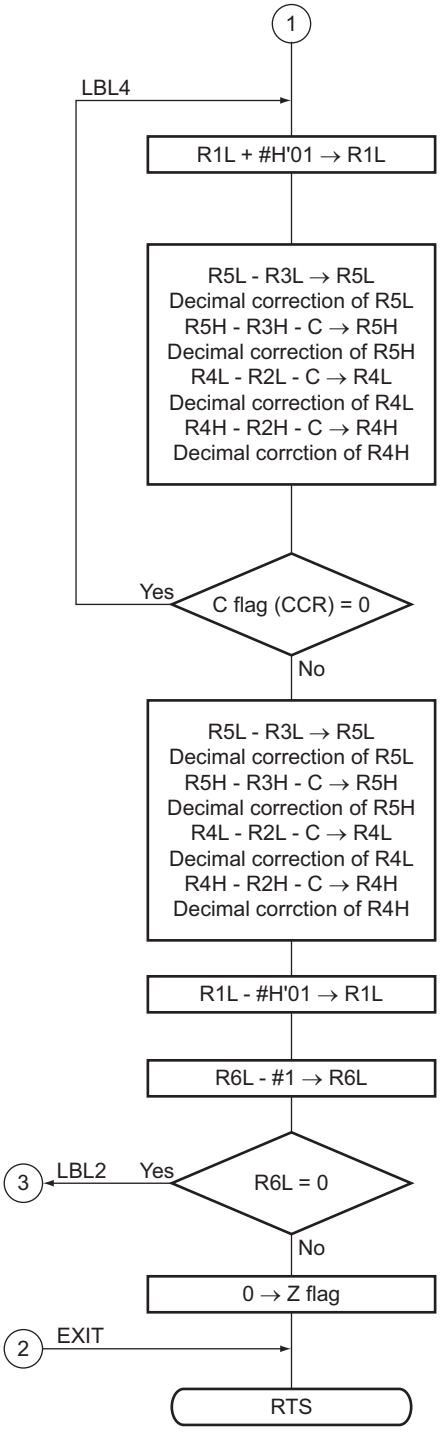


Figure 3 Example of Division (64733088 ÷ 5)

2. The program runs in the following steps:
   a. The dividend is shifted 4 bits (1 digit of the BCD) to left to place the upper 4 bits of the dividend in the lower 4 bits of the result of division (remainder).
   b. The divisor is subtracted from the dividend. Subtractions are repeated until the result becomes negative. The number of subtractions thus done is placed in the lower 4 bits (the least significant digit) of the dividend ((2)→(3)→(1) in figure 3). When the result has become negative, the divisor is added to the result (remainder) to return to the value before subtractions ((4) in figure 3).
   c. Steps a to b are repeated as many times as 8 digits.

6. Flowchart


DIVD
#H'0000 → R4
R4 → R5
Clear R4 and R5 to 0.
R4 = R2
No
Yes
Exit when the divisor (R2, R3) is 0.
2
EXIT
Yes
R5 = R3
No
LBL1
#H'08 → R6L
Place the number of digits
of the divisor data in R6L.
3
LBL2
#H'04 → R6H
LBL3
Shift R1L 1 bit to left
Rotate R1H 1 bit to left
Rotate R0L 1 bit to left
Rotate R0H 1 bit to left
Rotate R5L 1 bit to left
Rotate R5H 1 bit to left
Rotate R4L 1 bit to left
Rotate R4H 1 bit to left
Place the upper 4 bits of the dividend
in the lower 4 bits of the result (remainder).
R6H - #1 → R6H
Yes
R6H ≠ 0
No
1



------ Add H'01 to R1L

------ Perform decimal subtraction of the divisor (R2, R3) from the remainder (R4, R5).

------ Branch when the result of decimal subtraction is positive. When it is negative, perform decimal addition of the divisor (R2, R3) to the remainder (R4, R5) and subtracts H'01 from R1L.

------ Decrement R6L (number of digits).

------ Branch when R6L is not #H'00.

------ Place 0 in the Z flag.

7. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:02:05 PAGE 1
PROGRAM NAME =
 1                              ;*************************************************************
 2                              ;*
 3                              ;*      00 - NAME   :MULTIPLE-PRECISION DECIMAL DIVISION (DIVD)
 4                              ;*
 5                              ;*************************************************************
 6                              ;*
 7                              ;*      ENTRY       :R2,R3 (DIVISOR)
 8                              ;*                   R0,R1 (DIVIDEND)
 9                              ;*
10                              ;*      RETURNS     :R0,R1 (QUOTIENT)
11                              ;*                   R4,R5 (RESIDUAL)
12                              ;*                   Z flag OF CCR (Z=1;FALSE , Z=0;TRUE)
13                              ;*
14                              ;*************************************************************
15                              ;
16  DIVD_cod C    0000                    .SECTION                  DIVD_code,CODE,ALIGN=2
17                                        .EXPORT  DIVD
18                              ;
19  DIVD_cod C          00000000  DIVD    .EQU $                    ;Entry point
20  DIVD_cod C    0000  79040000          MOV.W    #H'0000,R4       ;Clear R4
21  DIVD_cod C    0004  0D45              MOV.W    R4,R5            ;Clear R5
22  DIVD_cod C    0006  1D42              CMP.W    R4,R2
23  DIVD_cod C    0008  4604              BNE      LBL1             ;Branch if Z=0
24  DIVD_cod C    000A  1D53              CMP.W    R5,R3
25  DIVD_cod C    000C  4744              BEQ      EXIT             ;Branch if Z=1 then exit
26  DIVD_cod C    000E            LBL1
27  DIVD_cod C    000E  FE08              MOV.B    #H'08,R6L        ;Set bit counter1
28  DIVD_cod C    0010            LBL2
29  DIVD_cod C    0010  F604              MOV.B    #H'04,R6H        ;Set bit counter2
30  DIVD_cod C    0012            LBL3
31  DIVD_cod C    0012  1009              SHLL.B   R1L              ;Shift dividend
32  DIVD_cod C    0014  1201              ROTXL.B  R1H
33  DIVD_cod C    0016  1208              ROTXL.B  R0L
34  DIVD_cod C    0018  1200              ROTXL.B  R0H
35  DIVD_cod C    001A  120D              ROTXL.B  R5L
36  DIVD_cod C    001C  1205              ROTXL.B  R5H
37  DIVD_cod C    001E  120C              ROTXL.B  R4L
38  DIVD_cod C    0020  1204              ROTXL.B  R4H
39  DIVD_cod C    0022  1A06              DEC.B    R6H              ;Decrement bit counter2
40  DIVD_cod C    0024  46EC              BNE      LBL3             ;Branch if Z=0
41  DIVD_cod C    0026            LBL4
42  DIVD_cod C    0026  0A09              INC.B    R1L              ;Increment R1L
43  DIVD_cod C    0028  18BD              SUB.B    R3L,R5L          ;R5L - R3L -> R5L
44  DIVD_cod C    002A  1F0D              DAS.B    R5L              ;Decimal adjust R5L
45  DIVD_cod C    002C  1E35              SUBX.B   R3H,R5H          ;R5H - R3H - C -> R3H
46  DIVD_cod C    002E  1F05              DAS.B    R5H              ;Decimal adjust R5H
47  DIVD_cod C    0030  1EAC              SUBX.B   R2L,R4L          ;R4L - R2L - C -> R4L
48  DIVD_cod C    0032  1F0C              DAS.B    R4L              ;Decimal adjust R4L
49  DIVD_cod C    0034  1E24              SUBX.B   R2H,R4H          ;R4H - R2H - C -> R4H
50  DIVD_cod C    0036  1F04              DAS.B    R4H              ;Decimal adjust R4H
```

```
51  DIVD_cod C    0038  44EC            BCC     LBL4              ;Branch if C = 0
52                                  ;
53  DIVD_cod C    003A  08BD            ADD.B   R3L,R5L           ;R3L + R5L -> R5L
54  DIVD_cod C    003C  0F0D            DAA.B   R5L               ;Decimal adjust R5L
55  DIVD_cod C    003E  0E35            ADDX.B  R3H,R5H           ;R3H + R5H + C -> R5H
56  DIVD_cod C    0040  0F05            DAA.B   R5H               ;Decimal adjust R5H
57  DIVD_cod C    0042  0EAC            ADDX.B  R2L,R4L           ;R2L + R4L + C -> R4L
58  DIVD_cod C    0044  0F0C            DAA.B   R4L               ;Decimal adjust R4L
59  DIVD_cod C    0046  0E24            ADDX.B  R2H,R4H           ;R2H + R4H + C -> R4H
60  DIVD_cod C    0048  0F04            DAA.B   R4H               ;Decimal adjust R4H
61  DIVD_cod C    004A  1A09            DEC.B   R1L               ;Decrement R1L
62  DIVD_cod C    004C  1A0E            DEC.B   R6L               ;Decrement bit counter1
63  DIVD_cod C    004E  46C0            BNE     LBL2
64  DIVD_cod C    0050  06FB            ANDC.B  #B'11111011,CCR   ;Clear Z flag of CCR
65  DIVD_cod C    0052          EXIT
66  DIVD_cod C    0052  5470            RTS
67                                  ;
68                                    .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.18.03	—	First edition issued
2.00	Nov.30.06	All pages	Content correction

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