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April 1st, 2010
Renesas Electronics Corporation

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H8SX Series

Direct Memory Operation

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

Contents

1. Overview

The H8SX series has an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series. Furthermore, in addition its instruction set has been enhanced to improve CPU performance. The enhancement of the instruction set has greatly improved the coding efficiency relative to the conventional series. This improvement in the coding efficiency has realized advantages such as a reduction of the amount of ROM required to store programs and the shortening of each instruction fetch cycle. This application note describes "direct memory operation", which is an enhanced instruction set item.

2. Configuration

"Direct memory operation" is a function that allows you to directly specify operands in memory with absolute addresses as the addressing mode for both the source and destination in arithmetic and logical operation instructions. For example, with the conventional H8S series, the addition of two data items in memory is performed by means of the following procedure: Transferring (loading) two data items in memory into individual registers, adding the contents of the registers, and then transferring (storing) the result of the addition into memory (with multiple instructions). With the H8SX series, this operation can be performed with one instruction. An example is shown in Figure 1.

In the following description, a sample that adds data items (byte, word, and longword) that are in memory is used to compare the H8SX series with the H8S series. The sample program is written in C. The results of comparing them in the following items are shown: The code generated by a compiler (assembler code), the instruction code length, and other items in the generated code.

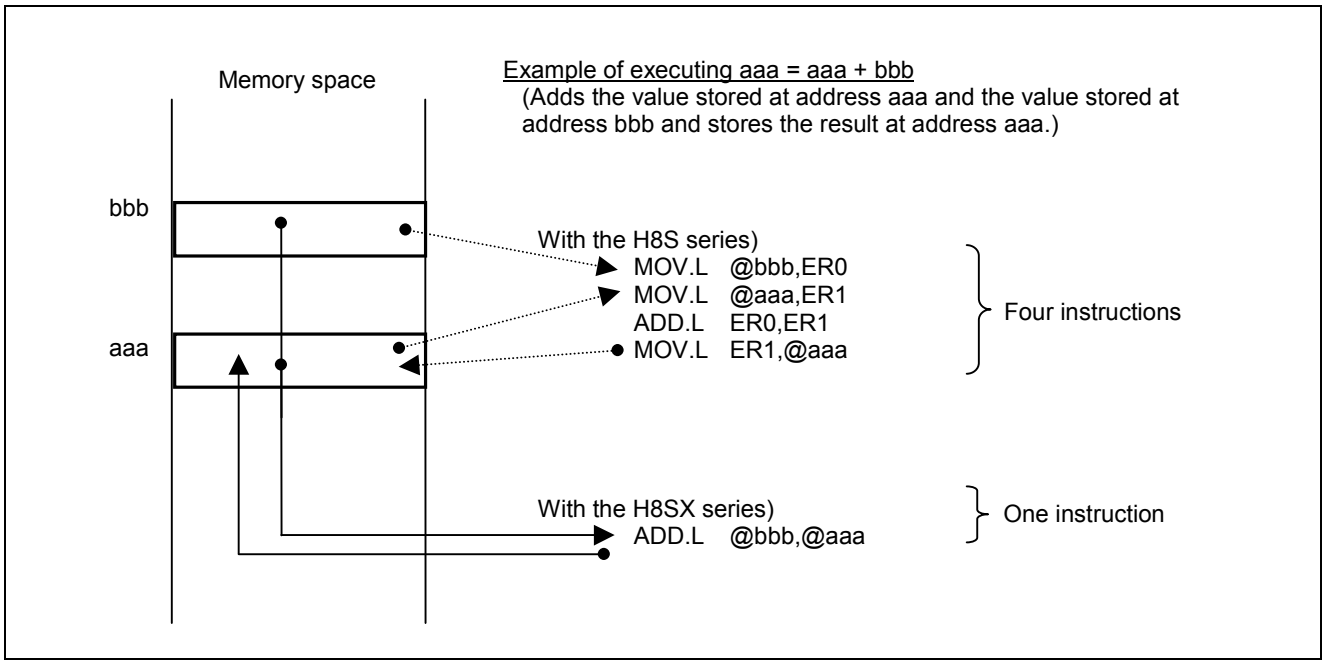
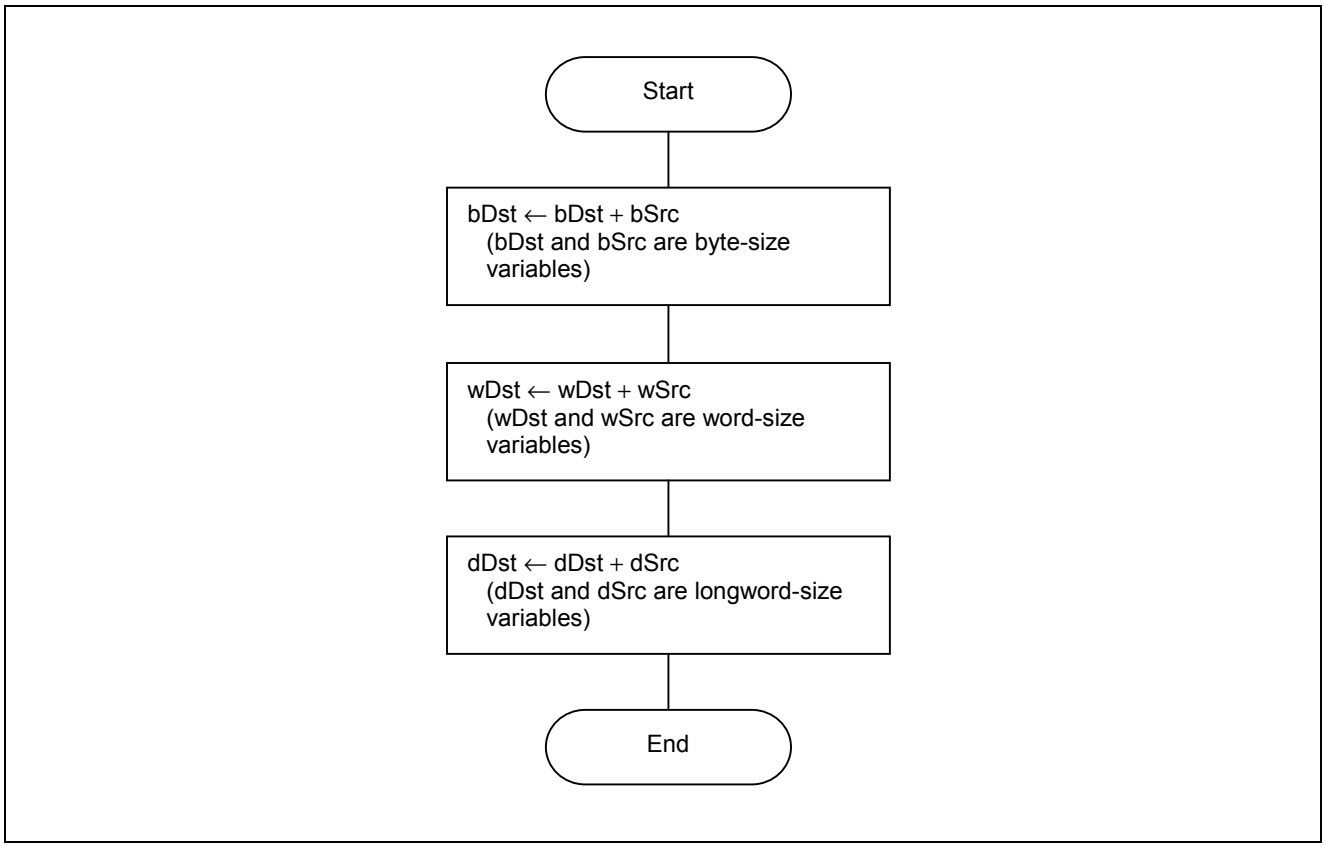


Figure 1 Example of Adding Data in Memory

3. Sample Program

3.1 Flowchart

The sample program shown below is very simple, but allows you to understand the description of "direct memory operation", an enhanced instruction set item. As a comparison with the H8S series, the results of compilation are shown. Use these results only for information because the instruction code length generated in the compilation of an application-level program depends on the source program and compile conditions. A flowchart is shown below for the sample program that adds data items (byte, word and longword) in memory.



3.2 Program Listing

A source program that is written in C is shown below.

```
/************************************************************/
/* include file                                             */
/************************************************************/
#include <machine.h>

/************************************************************/
/* function prototype                                       */
/************************************************************/
void mem_add( void );

/************************************************************/
/* static variable                                          */
/************************************************************/
static unsigned char  bSrc, bDst;
static unsigned short wSrc, wDst;
static unsigned long  dSrc, dDst;

/************************************************************/
/* function definition                                      */
/************************************************************/
void  mem_add( void )
{
   bDst += bSrc;
   wDst += wSrc;
   dDst += dSrc;

}
```

3.3 Comparison of the H8S Series with the H8SX Series

The result of compilation (assembly code) with the H8S series is shown below.

```
SCT OFFSET LABEL     INSTRUCTION OPERAND    COMMENT

P                                           ; section
  00000000 _mem_add:                        ; function: mem_add
  00000000     PUSH.L      ER2

  00000004     MOV.B       @__$bSrc:32,R0L
  0000000A     MOV.L       #__$bDst,ER1
  00000010     MOV.B       @ER1,R0H
  00000012     ADD.B       R0L,R0H
  00000014     MOV.B       R0H,@ER1

  00000016     MOV.W       @__$wSrc:32,R0
  0000001C     MOV.L       #__$wDst,ER1
  00000022     MOV.W       @ER1,E0
  00000024     ADD.W       R0,E0
  00000026     MOV.W       E0,@ER1

  00000028     MOV.L       @__$dSrc:32,ER0
  00000030     MOV.L       #__$dDst,ER1
  00000036     MOV.L       @ER1,ER2
  0000003A     ADD.L       ER0,ER2
  0000003C     MOV.L       ER2,@ER1
  00000040     POP.L       ER2

  00000044     RTS
B                                           ; section
  00000000 __$wSrc                          ; static: wSrc
  00000000     .RES.W      1
  00000002 __$wDst                          ; static: wDst
  00000002     .RES.W      1
  00000004 __$dSrc                          ; static: dSrc
  00000004     .RES.L      1
  00000008 __$dDst                          ; static: dDst
  00000008     .RES.L      1
  0000000C __$bSrc                          ; static: bSrc
  0000000C     .RES.B      1
  0000000D __$bDst                          ; static: bDst
  0000000D     .RES.B      1
```

The result of compilation (assembly code) with the H8SX series is shown below.

```
SCT OFFSET LABEL     INSTRUCTION OPERAND    COMMENT

P                                           ; section
  00000000 _mem_add:                        ; function: mem_add
  00000000     ADD.B       @__$bSrc:32,@__$bDst:32

  0000000C     ADD.W       @__$wSrc:32,@__$wDst:32

  00000018     ADD.L       @__$dSrc:32,@__$dDst:32
```

```
   00000026     RTS

B                                          ; section
   00000000 __$wSrc                        ; static: wSrc
   00000000     .RES.W      1
   00000002 __$wDst                        ; static: wDst
   00000002     .RES.W      1
   00000004 __$dSrc                        ; static: dSrc
   00000004     .RES.L      1
   00000008 __$dDst                        ; static: dDst
   00000008     .RES.L      1
   0000000C __$bSrc                        ; static: bSrc
   0000000C     .RES.B      1
   0000000D __$bDst                        ; static: bDst
   0000000D     .RES.B      1
```

Table 1 lists the operations performed with the H8S series, while Table 2 lists those performed with the H8SX series.

Table 1 Results of Compilation (H8S Series)

H8S series			Instruction length		Execution time	
			In bytes	Total	In states	Total
Byte data addition	MOV.B	@__$bSrc:32,R0L	6	60	4	42
	MOV.L	#__$bDst,ER1	6		3	
	MOV.B	@ER1,R0H	2		2	
	ADD.B	R0L,R0H	2		1	
	MOV.B	R0H,@ER1	2		2	
Word data addition	MOV.W	@__$wSrc:32,R0	6		4	
	MOV.L	#__$wDst,ER1	6		3	
	MOV.W	@ER1,E0	2		2	
	ADD.W	R0,E0	2		1	
	MOV.W	E0,@ER1	2		2	
Longword data addition	MOV.L	@__$dSrc:32,ER0	8		6	
	MOV.L	#__$dDst,ER1	6		3	
	MOV.L	@ER1,ER2	4		4	
	ADD.L	ER0,ER2	2		1	
	MOV.L	ER2,@ER1	4		4	

Table 2 Results of Compilation (H8SX Series)

H8SX series			Instruction length		Execution time	
			In bytes	Total	In states	Total
Byte data addition	ADD.B	@__$bSrc:32,@__$bDst:32	12	38	5	21
Word data addition	ADD.W	__$wSrc:32,@__$wDst:32	12		6	
Longword data addition	ADD.L	@__$dSrc:32,@__$dDst:32	14		10	

The enhancement of the CPU performance and code efficiency as a result of direct memory operation can be seen by comparing the data listed in Tables 1 and 2.

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sept.19.03	—	First edition issued

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