RX671 Group, RX63N/RX631 Group

Differences Between the RX671 Group and the RX63N Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX671 Group and RX63N Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 145-pin package version of the RX671 Group and the 176-/177-pin package version of the RX63N Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX671 Group and RX63N Group

Contents

1. Comparison of Built-In Functions of RX671 Group and RX63N Group

A comparison of the built-in functions of the RX671 Group and RX63N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX671 Group and RX63N Group.

Table 1.1 Comparison of Built-In Functions of RX671 Group and RX63N Group

Function	RX63N	RX671
CPU	●	●
Operating mode	●/■	●/■
Address space	▲	▲
Resets	○	○
Option-setting memory (OFSM)	●/▲	●/▲
Voltage detection circuit (LVDA)	●	●
Clock generation circuit	●/▲/■	●/▲/■
Frequency measurement circuit (MCK)	○	×
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption function	●	●
Battery backup function (VBATTB)	●	●
Register write protection function	●/■	●/■
Exception handling	●	●
Interrupt controller (ICUb): RX63N, (ICUE): RX671	●	●
Buses	●/▲	●/▲
Memory-protection unit (MPU)	▲	▲
DMA controller (DMACA): RX63N, (DMACAb): RX671	●	●
EXDMA controller (EXDMACa)	▲	▲
Data transfer controller (DTCa): RX63N, (DTCb): RX671	●	●
Event link controller (ELC)	×	○
I/O ports	●/■	●/■
Multi-function pin controller (MPC)	●/▲/■	●/▲/■
Multi-function timer pulse unit 2 (MTU2a): RX63N Multi-function timer pulse unit 3 (MTU3a): RX671	●	●
Port output enable 2 (POE2a): RX63N Port output enable 3 (POE3a): RX671	●	●
16-bit timer pulse unit (TPUa)	●	●
Programmable pulse generator (PPG)	●	●
8-bit timer (TMR): RX63N, (TMRb): RX671	●	●
Compare match timer (CMT)	●	●
Compare match timer W (CMTW)	×	○
Realtime clock (RTCa): RX63N, (RTCd): RX671	●	●
Watchdog timer (WDTA)	●	●
Independent watchdog timer (IWDTa)	●	●
Ethernet controller (ETHERC)	○	×
DMA controller for the ethernet controller (EDMAC)	○	×
USB 2.0 Host/Function module (USBa): RX63N USB 2.0 FS Host/Function module (USBb): RX671	●	●
Serial communications interface (SCIc, SCId): RX63N, (SCIk, SCIm, SCIh): RX671	●	●
Serial communications interface (RSCI)	×	○
I²C bus interface (RIIC): RX63N, (RIICa): RX671	●/■	●/■
High-speed I²C bus interface (RIICHS)	×	○

Function	RX63N	RX671
CAN module (CAN)		■
Serial peripheral interface (RSPI): RX63N, (RSPId): RX671		●
Serial peripheral interface (RSPIA)	×	○
Quad SPI memory interface (QSPIX)	×	○
IEBus™ controller (IEB)	○	×
CRC calculator (CRC): RX63N, (CRCA): RX671		●
SD host interface (SDHI)	×	○
Serial sound interface (SSIE)	×	○
Remote control signal receiver (REMCa)	×	○
Capacitive touch sensing unit (CTSUa)	×	○
Boundary scan		▲
Trusted Secure IP (TSIP)	×	○
Parallel data capture unit (PDC)	○	×
12-bit A/D converter (S12ADa): RX63N, (S12ADFa): RX671		●
10-bit A/D converter (ADb)	○	×
D/A converter (DAa)	○	×
Temperature sensor (TEMPS)		▲
Data operation circuit (DOCA)	×	○
RAM		●
Standby RAM	×	○
Flash memory		●/▲
Packages		▲/■

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX63N	RX671
CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Floating-point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
FPU	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Item	RX63N	RX671
Double-precision floating point coprocessor	—	• Double-precision floating-point register set — Double-precision floating-point data registers: 64-bit × 16 — Double-precision floating-point control registers: 32-bit × 4 • Double-precision floating-point processing instructions: 21 • Function for notifying the interrupt controller of double-precision floating-point exceptions
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

Table 2.2 Comparison of CPU Registers

Register	Bit	RX63N	RX671
EXTB	—	—	Exception table register
ACC (RX63N) ACC0, ACC1 (RX671)	—	Accumulator	Accumulator 0, accumulator 1
DR0 to DR15	—	—	Double-precision floating-point data registers
DPSW	—	—	Double-precision floating-point status word
DCMR	—	—	Double-precision floating-point comparison result register
DECNT	—	—	Double-precision floating-point exception handling control register
DEPC	—	—	Double-precision floating-point exception program counter

2.2 Operating Modes

Table 2.3 is a comparative overview of the operating modes, and Table 2.4 is a comparison of operating mode registers.

Table 2.3 Comparative Overview of Operating Modes

Item	RX63N	RX671
Operating modes selected by mode-setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
	USB boot mode	Boot mode (USB interface)
	User boot mode	—
	—	Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode	Single-chip mode
	User boot mode	—
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode
Selection of endian	Single-chip mode: MDES (endian select register S) User boot mode: MDEB (endian select register B)	MDE register

Table 2.4 Comparison of Operating Mode Registers

Register	Bit	RX63N	RX671
MDSR	—	Mode status register	—
SYSCR1	SBYRAME	—	Standby RAM enable bit

2.3 Address Space

Figure 2.1 is a comparative memory map of single-chip mode, Figure 2.2 is a comparative memory map of on-chip ROM enabled extended mode, and Figure 2.3 is a comparative memory map of on-chip ROM disabled extended mode.

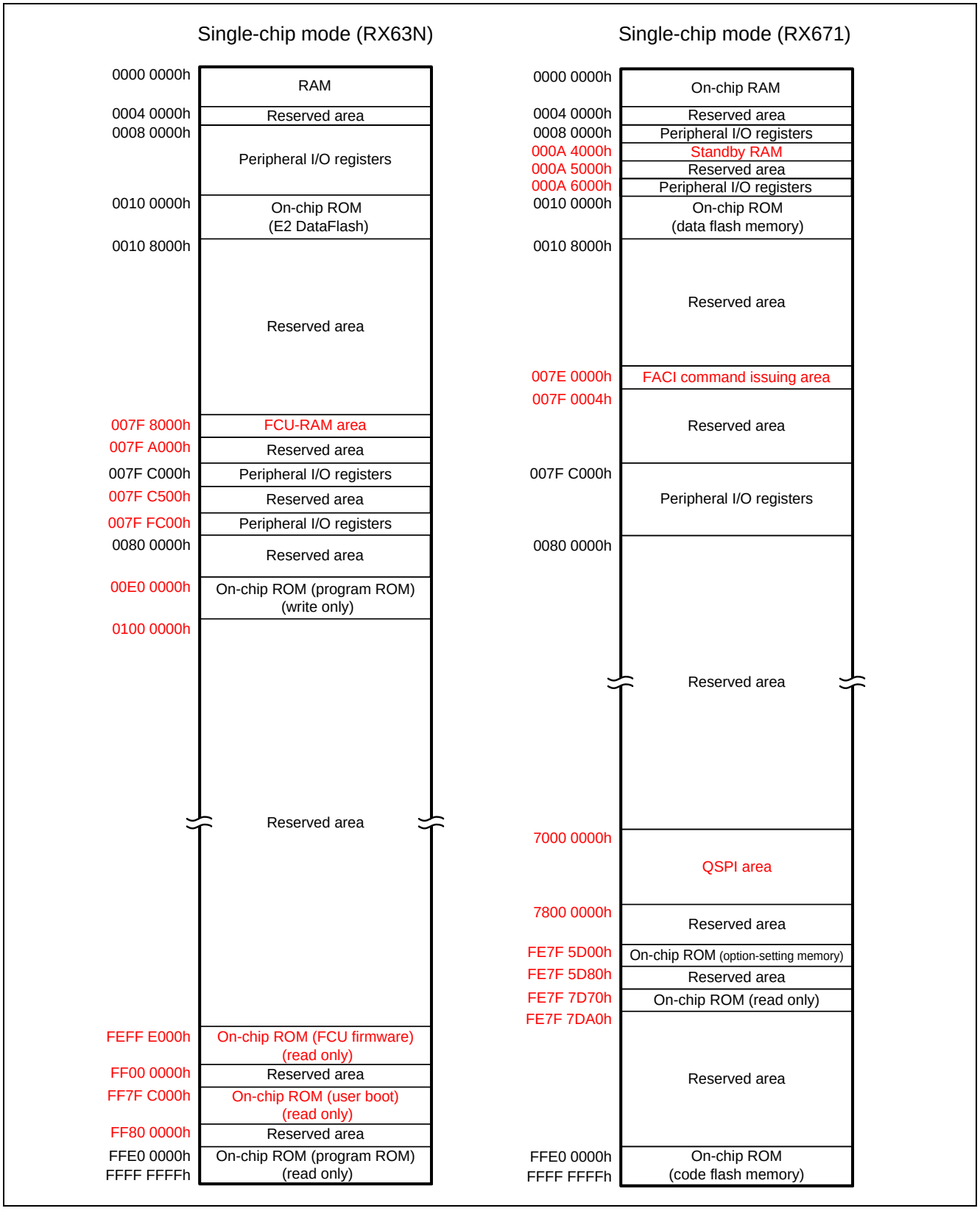

Figure 2.1 Comparative Memory Map of Single-Chip Mode

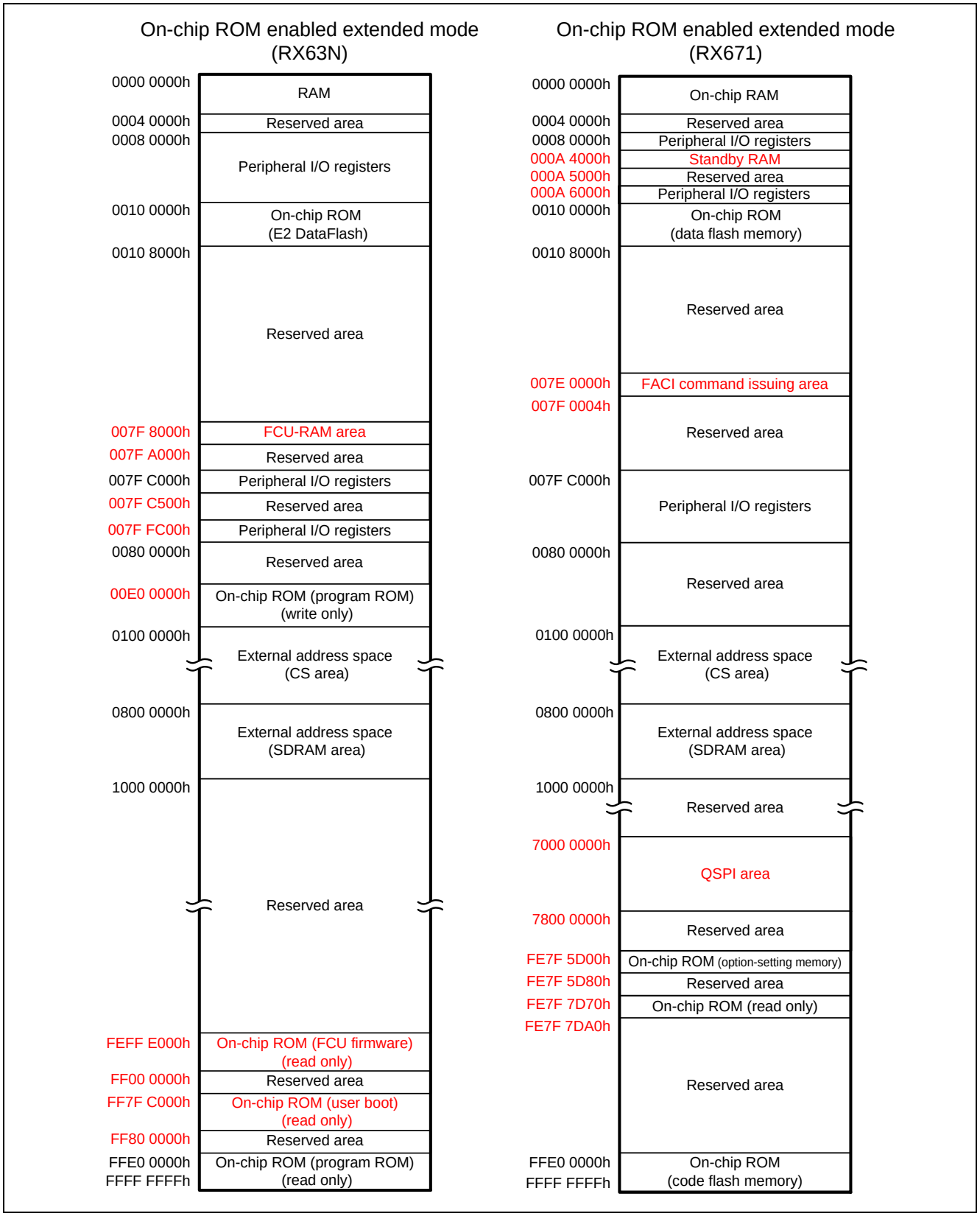

Figure 2.2 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

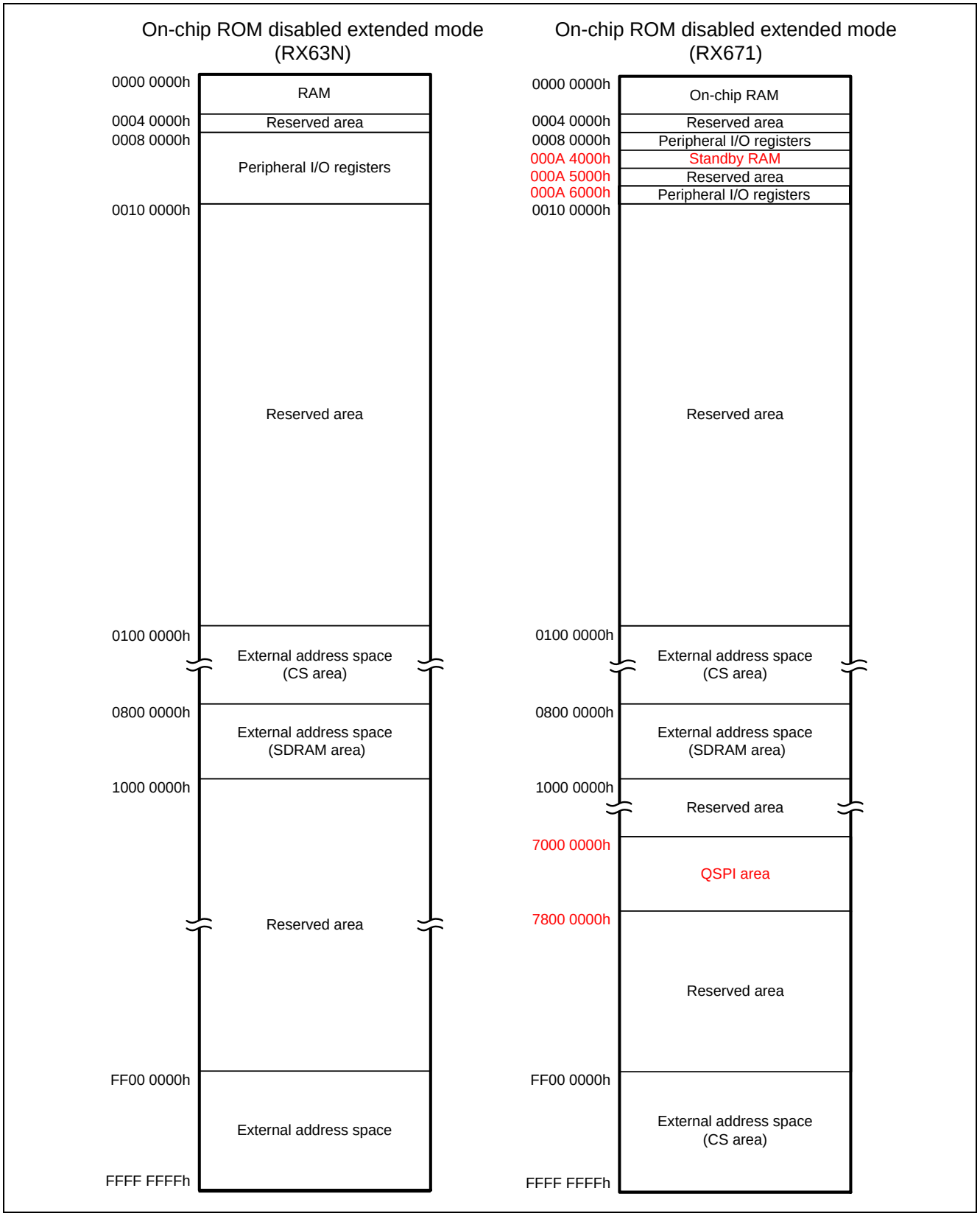

Figure 2.3 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

2.4 Option-Setting Memory

Figure 2.4 is a comparison of option-setting memory areas, and Table 2.5 is a comparison of option-setting memory registers.

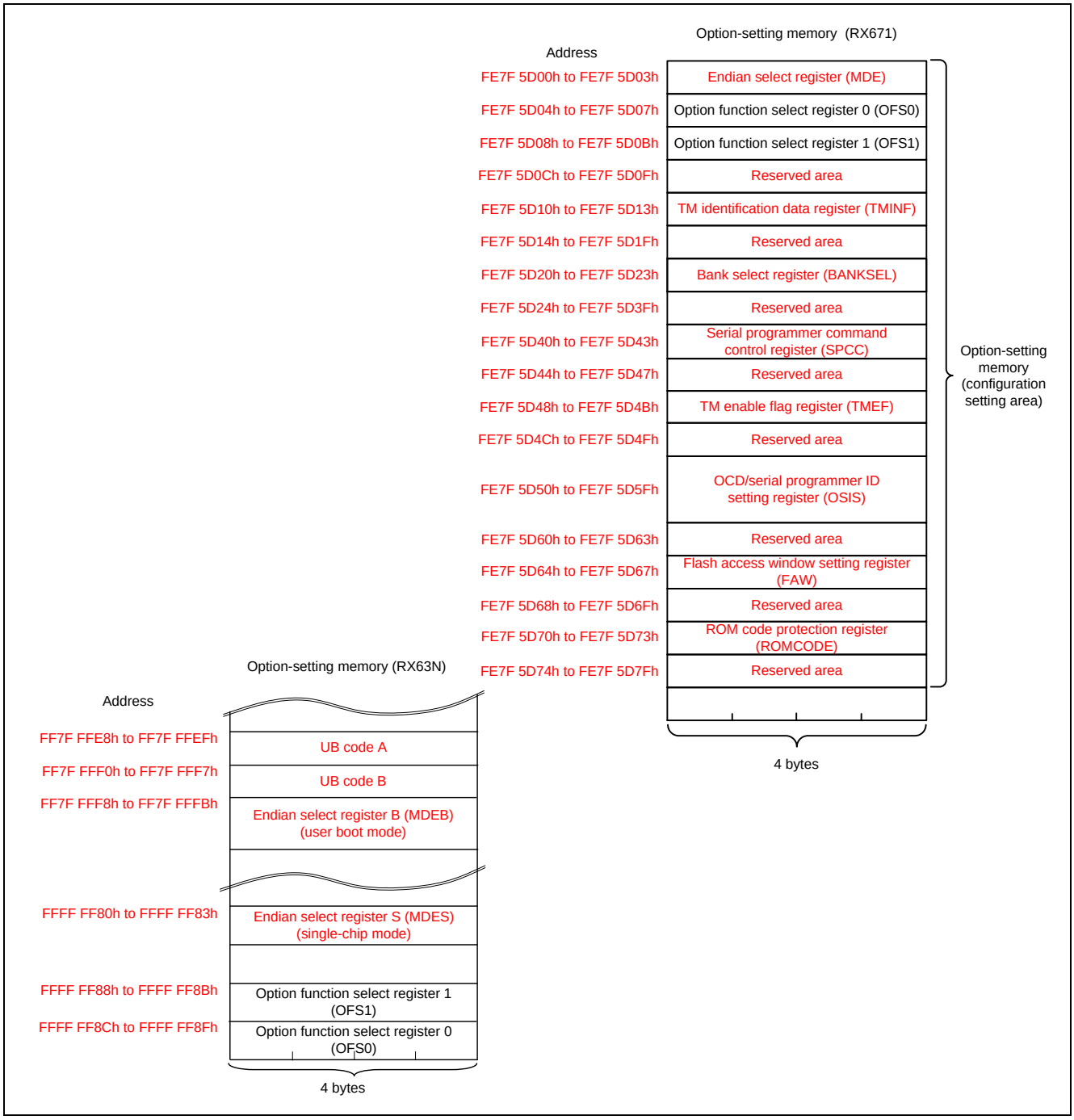

Figure 2.4 Comparison of Option-Setting Memory Areas

Table 2.5 Comparative Overview of Option-Setting Memory Registers

Register	Bit	RX63N	RX671 (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial program ID setting register
OFS0	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled. 1: Reset is enabled.	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request is enabled. 1: Reset is enabled.
	WDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled. 1: Reset is enabled.	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request is enabled. 1: Reset is enabled.
OFS1	VDSEL[1:0]	—	Voltage detection 0 level select bits
MDEB	—	Endian select register B	—
MDES	—	Endian select register S	—
MDE	—	—	Endian select register
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
BANKSEL	—	—	Bank select register
FAW	—	—	Flash access window setting register
ROMCODE	—	—	ROM code protection register

2.5 Voltage Detection Circuit

Table 2.6 is a comparative overview of the voltage detection circuits, and Table 2.7 is a comparison of voltage detection circuit registers.

Table 2.6 Comparative Overview of Voltage Detection Circuits

Item		RX63N (LVDA)			RX671 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
	Detection voltage	One level fixed	Specify voltage using LVDLVLR.LVD1LVL[3:0] bits	Specify voltage using LVDLVLR.LVD2LVL[3:0] bits	Selectable from three levels using OFS1.VDSEL[1:0] bits.	Selectable from three levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from three levels using LVDLVLR.LVD2LVL[3:0] bits.
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.
	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable interrupt	Non-maskable interrupt		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
			Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.

Item		RX63N (LVDA)			RX671 (LVDA)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
Digital filter	Enable/ disable switching	—	Available	Available	—	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	—	—	—	Available: Vdet pass-through detection event output	Available: Vdet pass-through detection event output

Table 2.7 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX63N (LVDA)	RX671 (LVDA)
LVD1CR1	LVD1IRQSEL	—	Voltage monitoring 1 interrupt type select bit
LVD2CR1	LVD2IRQSEL	—	Voltage monitoring 2 interrupt type select bit
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 1 0 1 0: 2.95 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 1 0 0 1: 2.99 V (Vdet1_1) 1 0 1 0: 2.92 V (Vdet1_2) 1 0 1 1: 2.85 V (Vdet1_3) Settings other than the above are prohibited.
	LVD2LVL[3:0]	Voltage detection 2 level select bits (standard voltage during drop in voltage) b7 b4 1 0 1 0: 2.95 V Settings other than the above are prohibited.	Voltage detection 2 level select bits (standard voltage during drop in voltage) b7 b4 1 0 0 1: 2.99 V (Vdet2_1) 1 0 1 0: 2.92 V (Vdet2_2) 1 0 1 1: 2.85 V (Vdet2_3) Settings other than the above are prohibited.
LVD1CR0	LVD1FSAMP[1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency
LVD2CR0	LVD2FSAMP[1:0]	Sampling clock select bits b5 b4 0 0: 1/1 LOCO frequency 0 1: 1/2 LOCO frequency 1 0: 1/4 LOCO frequency 1 1: 1/8 LOCO frequency	Sampling clock select bits b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency

2.6 Clock Generation Circuit

Table 2.8 is a comparative overview of the clock generation circuits, and Table 2.9 is a comparison of clock generation circuit registers.

Table 2.8 Comparative Overview of Clock Generation Circuits

Item	RX63N	RX671
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, and DEU. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the IEBUS clock (IECLK) supplied to the IEBUS. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC-dedicated main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, QSPIX, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, RSPIA, SCIm, RSCI, MTU, and RIICHS. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module (for analog conversion) clocks (PCLKC: unit 0, PCLKD: unit 1) to be supplied to the S12ADC. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the RTC sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC main clock (RTCMCLK) supplied to the RTC. • Generates the REMC sub clock (REMSCLK) supplied to the REMC. • Generates the VBATT clock (VBATCLK) supplied to the VBATT. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.

Item	RX63N	RX671
Operating frequencies	• ICLK: 100 MHz (max.) • PCLKA: 100 MHz (max.) • PCLKB: 50 MHz (max.) • FCLK: — 4 MHz to 50 MHz (when programming or erasing the ROM or E2 DataFlash) — 50 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 100 MHz (max.) • BCLK pin output: 50 MHz (max.) • SDCLK pin output: 50 MHz (max.) • UCLK: 48 MHz (max.) • CANMCLK: 20 MHz (max.) • IECLK: 50 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 4 MHz to 16 MHz • IWDTCLK: 125 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (when programming or erasing the code flash memory or data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • CLKOUT pin output: 40 MHz (max.) • CACCLK: Same frequency as each oscillator • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 1 kHz to 16 MHz • REMSCLK: 32.768 kHz • VBATCLK: 32.768 kHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 4 MHz to 16 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT

Item	RX63N	RX671
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 16 MHz • Frequency multiplication ratio: Selectable within range from 8, 10, 12, 16, 20, 24, 25, and 50 • VCO oscillation frequency: 104 MHz to 200 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable within range from 10 to 30 • PLL frequency synthesizer output clock frequency: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 50 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function • Support for user trimming
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
External clock input (TCK) for JTAG	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock
Control of output on SDCLK pin	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable
Event link function (output)	—	Main clock oscillator oscillation stop detection
Event link function (input)	—	Switching of clock source to low-speed on-chip oscillator

Table 2.9 Comparison of Clock Generation Circuit Registers

Register	Bit	RX63N	RX671
SCKCR	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
ROMWT	—	—	ROM wait cycle setting register
SCKCR2	IEBCK[3:0]	IEBUS clock (IECLK) select bits	—
	UCK[3:0]	USB clock (UCLK) select bits b7 b4 0 0 1 0: ×1/3 0 0 1 1: ×1/4 Settings other than the above are prohibited when USB is in use. When USB is not in use, these bits are read as 0001b. The write value should be 0001b.	USB clock (UCLK) select bits b7 b4 0 0 0 1: ×1/2 0 0 1 0: ×1/3 0 0 1 1: ×1/4 0 1 0 0: ×1/5 Settings other than the above are prohibited when USB is in use. When USB is not in use, these bits are read as 0001b. The write value should be 0001b.

Register	Bit	RX63N	RX671
PLLCR	—	PLL control register	PLL control register
		Initial values after a reset are different.	
	PLIDIV[1:0]	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited.	PLL input frequency division ratio select bits b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/3 1 1: Setting prohibited.
	PLLSRCSEL	—	PLL clock source select bit
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×8 0 0 1 0 0 1: ×10 0 0 1 0 1 1: ×12 0 0 1 1 1 1: ×16 0 1 0 0 1 1: ×20 0 1 0 1 1 1: ×24 0 1 1 0 0 0: ×25 1 1 0 0 0 1: ×50 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 ... 0 1 1 0 0 0: ×12.5 ... 1 1 0 0 0 1: ×25.0 ... 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register
MOSCWTCR*1	MSTS[4:0] (RX63N) MSTS[7:0] (RX671)	Main clock oscillator wait time select bits (b4 to b0)	Main clock oscillator wait time select bits (b7 to b0)
SOSCWTCR*1	SSTS[4:0] (RX63N) SSTS[7:0] (RX671)	Sub-clock oscillator wait time select bits (b4 to b0)	Sub-clock oscillator wait time select bits (b7 to b0)
MOFCR	MODRV2 [1:0]	—	Main clock oscillator drive capability 2 switch bits
	MOSEL	—	Main clock oscillator switch bit
CKOCR	—	—	CLKOUT output control register
SOSCCR2	—	—	Sub-clock oscillator control register 2

Register	Bit	RX63N	RX671
BKSCCR	—	—	Backup area sub-clock control register
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0 to 2)

Note: 1. In the User's Manual: Hardware of the RX63N Group, MOSCWTCR and SOSCWTCR are described in the Low Power Consumption section.

2.7 Low Power Consumption

Table 2.10 is a comparative overview of low power consumption, Table 2.11 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.12 is a comparison of low power consumption registers.

Table 2.10 Comparative Overview of Low Power Consumption

Item	RX63N	RX671
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA and PCLKB), external bus clock (BCLK), and Flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and Flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	SDCLK output or high-level output can be selected.	SDCLK output or high-level output can be selected.
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in the power consumption when the same conditions (frequency and voltage) are specified in low-speed operating mode 1 and low-speed operating mode 2.

Table 2.11 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX63N	RX671
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM1 (0001 0000h to 0003 FFFh): RX63N RAM: RX671	Operation possible (retained)	Operation possible (retained)
	RAM0 (0000 0000h to 0000 FFFFh)	Operation possible (retained)	—
	Standby RAM	—	Operation possible (retained)
	Flash memory	Operation	Operation
	USB 2.0 Host/Function module (USB)	Operation possible	Operation possible
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM1 (0001 0000h to 0003 FFFh): RX63N RAM: RX671	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh)	Stopped (retained)	—
	Standby RAM	—	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX63N	RX671
All-module clock stop mode	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USB)	Stopped	Stopped
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible*1	Operation possible*1
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM1 (0001 0000h to 0003 FFFh): RX63N RAM: RX671	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh)	Stopped (retained)	—
	Standby RAM	—	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USB)	Stopped	Stopped
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX63N	RX671
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)
	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM1 (0001 0000h to 0003 FFFFh): RX63N RAM: RX671	Stopped (undefined)	Stopped (undefined)
	RAM0 (0000 0000h to 0000 FFFFh)	Stopped (retained/undefined)	—
	Standby RAM	—	Stopped (retained/undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USB)	Stopped (retained/undefined)	Stopped (retained/undefined)
	Watchdog timer (WDT)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Port output enable (POE)	Stopped (undefined)	Stopped (undefined)
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Other peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

Notes: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

1. If POE interrupts are enabled and a POE interrupt source occurs while the chip is in all-module clock stop mode, return from all-module clock stop mode does not occur but the state of the interrupt source flag is retained. If a different source initiates return from all-module clock stop mode in this state, the POE interrupt is generated after the return.

Table 2.12 Comparison of Low Power Consumption Function Registers

Register	Bit	RX63N	RX671
MSTPCRA	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA9	Multi-function timer pulse unit 2 module stop bit	Multi-function timer pulse unit 3 module stop bit
	MSTPA12	16-bit timer pulse unit 1 (unit 1) module stop bit	—
	MSTPA16	—	12-bit A/D converter (unit 1) module stop bit
	MSTPA19	12-bit D/A converter module stop bit	—
	MSTPA23	10-bit A/D converter module stop bit	—
MSTPCRB	MSTPB2	CAN module 2 module stop bit	—
	MSTPB4	Serial communication interface SCId module stop bit	Serial communication interface SCIh module stop bit
	MSTPB6	—	Data operation circuit module stop bit
	MSTPB9	—	Event link controller module stop bit
	MSTPB15	Ethernet controller DMAC (channel 0) module stop bit	—
	MSTPB22	Parallel data capture unit module stop bit	—
MSTPCRC	MSTPC1	RAM1 module stop bit	—
	MSTPC7	—	Standby RAM module stop bit
	MSTPC16	I^2C bus interface 3 module stop bit	—
	MSTPC18	IEBUS module stop bit	—
	MSTPC19	Frequency measurement circuit module stop bit Target module: MCK	CAC module stop bit Target module: CAC
MSTPCRD	—	Module stop control register D	Module stop control register D
		Initial values after a reset are different.	
	MSTPD1	—	Quad SPI memory interface module-stop setting bit
	MSTPD2	—	Serial communication interface 11 module-stop setting bit
	MSTPD3	—	Serial communication interface 10 module-stop setting bit
	MSTPD5	—	High-speed I^2C bus interface module stop bit
	MSTPD7	—	Remote control signal receiver module stop bit
	MSTPD12	—	Capacitive touch sensing unit module stop bit
	MSTPD15	—	Serial sound interface module-stop setting bit
	MSTPD19	—	SD host interface module-stop setting bit
	MSTPD26	—	Serial peripheral interface module-stop setting bit

Register	Bit	RX63N	RX671
MSTPCRD	MSTPD27	—	Trusted Secure IP module-stop setting bit
	MSTPD31	Data encryption unit (DEU) module stop bit	—
MOSCWTCR*1	MSTS[4:0] (RX63N) MSTS[7:0] (RX671)	Main clock oscillator wait time select bits (b4 to b0)	Main clock oscillator wait time select bits (b7 to b0)
SOSCWTCR*1	SSTS[4:0] (RX63N) SSTS[7:0] (RX671)	Sub-clock oscillator wait time select bits (b4 to b0)	Sub-clock oscillator wait time select bits (b7 to b0)
PLLWTCR	—	PLL wait control register	—
DPSIER3	DRMCIE	—	REMC interrupt deep standby cancel signal enable bit
	DTADIE	—	VBATT tamper detection deep standby cancel signal enable bit
DPSIFR3	DRMCIF	—	Deep standby cancel by REMC interrupt flag
	DTADIF	—	VBATT tamper detection deep standby cancel flag
DPSBKRy	—	Deep standby backup register y (y = 0 to 31)	—

Note: 1. In the User's Manual: Hardware of the RX671 Group, MOSCWTCR and SOSCWTCR are described in the Clock Generation Circuit section.

2.8 Battery Backup Function

Table 2.13 is a comparative overview of the battery backup functions, and Table 2.14 is a comparison of battery backup function registers.

Table 2.13 Comparative Overview of Battery Backup Functions

Item	RX63N	RX671 (VBATTB)
Backup target	• Sub-clock oscillator • Realtime clock (RTC)	All modules in the backup area • Backup register • Sub-clock oscillator • Power-down detection circuit • Tamper detection circuit • Realtime clock (RTC)
Backup register	—	128 bytes Can be erased immediately when tamper detection occurs.
Backup area power-down detection	—	Generates a backup area reset signal when the power supply voltage to the backup area drops.
Tamper event detection	—	Detects unauthorized access to the system, and provides notification by setting a flag or generating an interrupt. • A timestamp can be obtained when tamper detection occurs. • Tamper input pins: 3 (TAMPI0 to TAMPI2) • Built-in noise filter (sampling rate: 32.768 kHz, three-match detection) • Can be used as a source for triggering return from deep software standby mode.

Table 2.14 Comparison of Battery Backup Function Registers

Register	Bit	RX63N	RX671 (VBATTB)
BKPSR	—	—	Backup area power supply status register
TAMPSR	—	—	Tamper status register
TAMPCR	—	—	Tamper control register
TCECR	—	—	Time capture event control register
TAMPICR1	—	—	Tamper/RTCIC input control register 1
TAMPICR2	—	—	Tamper/RTCIC input control register 2
TAMPIMR	—	—	Tamper/RTCIC input monitor register
BKRn	—	—	Backup register n (n = 0 to 127)

2.9 Register Write Protection Function

Table 2.15 is a comparative overview of the register write protection functions.

Table 2.15 Comparative Overview of Register Write Protection Functions

Item	RX63N	RX671
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR	Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, CKOCR, FLLCR1, FLLCR2, HOCOTRR0, HOCOTRR1, HOCOTRR2, CTSUTRMR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR • Registers related to battery backup: BKSCCR, BKPSR, SOSCCR2, TAMPSR, TAMPCR, TCECR, TAMPICR1, TAMPICR2, TAMPIMR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.10 Exception Handling

Table 2.16 is a comparative overview of exception handling, Table 2.17 is a comparative listing of vector tables, and Table 2.18 is a comparative listing of return from exception handling routine instructions.

Table 2.16 Comparative Overview of Exception Handling

Item	RX63N	RX671
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Address exception • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.17 Comparative Listing of Vector Tables

Item		RX63N	RX671
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception (RX63N)/ single-precision floating-point exception (RX671)		Fixed vector table	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.18 Comparative Listing of Return from Exception Handling Routine Instructions

Item		RX63N	RX671
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Address exception		—	RTE
Floating-point exception (RX63N)/ single-precision floating-point exception (RX671)		RTE	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Prohibited	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.11 Interrupt Controller

Table 2.19 is a comparative overview of the interrupt controllers, and Table 2.20 is a comparison of interrupt controller registers.

Table 2.19 Comparative Overview of Interrupt Controllers

Item		RX63N (ICUb)	RX671 (ICUE)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source. • Interrupt grouping: Multiple interrupts can be assigned to a single interrupt vector. — Number of groups for edge detection interrupts: 7 (groups 0 to 6) — Number of groups for level detection interrupts: 1 (group 12) • Unit selection function: Either of two interrupt request sources can be selected as the interrupt request source. Number of units: 6	• Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX63N (ICUb)	RX671 (ICUE)
Interrupts	External pin interrupts	• Interrupts from pins IRQ0 to IRQ15 • Number of sources: 16 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • Digital filter function: supported	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt can be generated by writing to a register. • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority	Setting of priority level by writing to a register	Setting of priority level in interrupt source priority register (IPR)
	Fast interrupt function	It is possible to speed up interrupt processing by the CPU. This setting can be used for one interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	—	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: supported	• Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt at detection of oscillation stop	Interrupt at detection of main clock oscillation stop
	WDT underflow/ refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.

Item		RX63N (ICUb)	RX671 (ICUE)
Non-maskable interrupts	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in the RAM.
	Double-precision floating-point exceptions	—	Exceptions from double-precision floating-point coprocessor
Return from low power consumption state	Sleep mode	Exit sleep mode by a non-maskable interrupt or any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Return is initiated by non-maskable interrupts, interrupts IRQ0 to IRQ15, TMR interrupts, USB resume interrupts, and RTC alarm/period interrupts.	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB0 resume, RTC alarm, RTC period, IWDT, VBATT tamper detection, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Return is initiated by non-maskable interrupts, interrupts IRQ0 to IRQ15, USB resume interrupts, and RTC alarm/period interrupts.	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	—	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

Table 2.20 Comparison of Interrupt Controller Registers

Register	Bit	RX63N (ICUb)	RX671 (ICUE)
IRn*1	—	Interrupt request register n (n = 016 to 253)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 253)	Interrupt source priority register n (n = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC activation enable register n (n = 027 to 251)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	DMAC activation request select register m (m = 0 to 3)	DMAC trigger select register m (m = 0 to 7)
NMISR	EXNMIST	—	Extended non-maskable interrupt status flag
NMIER	EXNMIEN	—	Extended non-maskable interrupt enable bit
EXNMISR	—	—	Extended non-maskable interrupt status register
EXNMIER	—	—	Extended non-maskable interrupt enable register
EXNMICLR	—	—	Extended non-maskable interrupt status clear register
GRPm	—	Group m interrupt source register (m = 0 to 6, 12)	—
GENm	—	Group m interrupt enable register (m = 0 to 6, 12)	—
GCRm	—	Group m interrupt clear register (m = 0 to 6)	—
SEL	—	Unit selecting register	—
GRPIE0	—	—	Group IE0 interrupt request register
GRPBE0	—	—	Group BE0 interrupt request register
GRPBL0 GRPBL1	—	—	Group BL0/BL1 interrupt request register
GRPAL0 GRPAL1	—	—	Group AL0/AL1 interrupt request register
GENIE0	—	—	Group IE0 interrupt request enable register
GENBE0	—	—	Group BE0 interrupt enable register
GENBL0 GENBL1	—	—	Group BL0/BL1 interrupt enable register
GENAL0 GENAL1	—	—	Group AL0/AL1 interrupt enable register
GCRIE0	—	—	Group IE0 interrupt clear register
GCRBE0	—	—	Group BE0 interrupt clear register
PIBRk	—	—	Software configurable interrupt B request register k (k = 0h to Ch)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh)
SLIBXRn	—	—	Software configurable interrupt B source select register Xn (n = 128 to 143)
SLIBRn	—	—	Software configurable interrupt B source select register n (n = 144 to 207)

Register	Bit	RX63N (ICUb)	RX671 (ICUE)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SELEXDR	—	—	EXDMAC activation interrupt select register
SLIPRCR	—	—	Software configurable interrupt source select register Write protection register

Note: 1. On the RX63N Group n = 254, 255 correspond to a reserved area.

2.12 Buses

Table 2.21 is a comparative overview of the buses, Table 2.22 is a comparative overview of the external buses, and Table 2.23 is a comparison of bus registers.

Table 2.21 Comparative Overview of Buses

Item		RX63N	RX671
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC, DMAC, and EDMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, DEU, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)

Item		RX63N	RX671
Internal peripheral buses	Internal peripheral bus 3	• Connected to peripheral modules (USB and PDC) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USB, DOC, CTSU, REMC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC and ETHERC) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral modules (MTU, SCIm, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (RSCI, RSPIA, and RIICHS) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to ROM (in P/E) and E2 DataFlash. • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)
Internal expansion bus	QSPI area	—	• Connected to external SPI devices • Operates in synchronization with the system clock (ICLK)

Table 2.22 Comparative Overview of External Buses

Item	RX63N	RX671
External address space	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • The bus width can be selected independently for each area. — Separate bus: An 8, 16, or 32-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be selected independently for each area.	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • The bus width can be selected independently for each area. — Separate bus: An 8 or 16-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be selected independently for each area.
CS area controller	• Recovery cycles can be inserted. — Up to 15 cycles for read recovery — Up to 15 cycles for write recovery • Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access). • Wait control — Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#) — Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1# to WR3#) — Ability to specify data output start and end timing • Write access mode: Single write strobe mode or byte strobe mode • Separate bus or address/data multiplexed bus can be specified for each area.	• Recovery cycles can be inserted. — Up to 15 cycles for read recovery — Up to 15 cycles for write recovery • Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access). • Wait control — Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#) — Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1#) — Ability to specify data output start and end timing • Write access mode: Single write strobe mode or byte strobe mode • Separate bus or address/data multiplexed bus can be specified for each area.
SDRAM area controller	• Multiplexed output of row address/ column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh • CAS latency can be specified from one to three cycles.	• Multiplexed output of row address/ column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh • CAS latency can be specified from one to three cycles.
Write buffer function	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.
Frequencies	• The CS area controller (CSC) operates in synchronization with BCLK. • The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.	• The CS area controller (CSC) operates in synchronization with BCLK. • The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.

Table 2.23 Comparison of Bus Registers

Register	Bit	RX63N	RX671
CSnCR (n = 0 to 7)	BSIZE[1:0]	External bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited	External bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: Setting prohibited 1 0: 8-bit bus space selected 1 1: Setting prohibited
SDCCR	BSIZE[1:0]	SDRAM bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited	SDRAM bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: Setting prohibited 1 0: 8-bit bus space selected 1 1: Setting prohibited
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: EDMAC 1 1 1: EXDMAC	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: EXDMAC
BUSPRI	BPXB[1:0]	—	Internal expansion bus priority control bits

2.13 Memory Protection Unit

Table 2.24 is a comparison of memory protection unit registers.

Table 2.24 Comparison of Memory Protection Unit Registers

Register	Bit	RX63N (MPU)	RX671 (MPU)
MPESTS	IA (RX63N) IMPER (RX671)	Instruction memory protection error generated bit	Instruction memory protection error generated bit
	DA (RX63N) DMPER (RX671)	Data memory protection error generated bit	Data memory protection error generated bit

2.14 DMA Controller

Table 2.25 is a comparative overview of the DMA controllers, and Table 2.26 is a comparison of DMA controller registers.

Table 2.25 Comparative Overview of DMA Controllers

Item		RX63N (DMACA)	RX671 (DMACAb)
Number of channels		4 (DMACm (m = 0 to 3))	8 (DMACm (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	4 GB (00000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		1 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 1,024 blocks)	64 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA request sources		Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)
Transfer data	Single data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data units: 1 to 1,024 data units	Number of data units: 1 to 1,024 data units
Transfer modes	Normal transfer mode	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units
	Block transfer mode	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX63N (DMACA)	RX671 (DMACAb)
Interrupt requests	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	• Generated when the specified number of transfers is completed in normal transfer mode • Generated when the specified repeat count of transfers is completed in repeat transfer mode • Generated when the specified block count of transfers is completed in block transfer mode
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link activation		—	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		Module stop state can be set.	Module stop state can be set.

Table 2.26 Comparison of DMA Controller Registers

Register	Bit	RX63N (DMACA)	RX671 (DMACAb)
DMSAR	—	DMA source address register Specifies the start address of the transfer source. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA source address register Specifies the start address of the transfer source. 00000000h to FFFFFFFFh (4 GB)
DMDAR	—	DMA destination address register Specifies the start address of the transfer destination. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA destination address register Specifies the start address of the transfer destination. 00000000h to FFFFFFFFh (4 GB)
DMCRB	—	DMA block transfer count register (b9 to b0) 001h to 3FFh (1 to 1,023 operations) 000h (1,024 operations)	DMA block transfer count register (b15 to b0) 0001h to FFFFh (1 to 65,535 operations) 0000h (65,536 operations)
DMIST	—	—	DMAC74 interrupt status monitor register

2.15 EXDMA Controller

Table 2.27 is a comparative overview of the EXDMA controllers, and Table 2.28 is a comparison of EXDMA controller registers.

Table 2.27 Comparative Overview of EXDMA Controllers

Item		RX63N (EXDMACa)	RX671 (EXDMACa)
Number of channels		2 (EXDMAC0 and EXDMAC1)	2 (EXDMAC0 and EXDMAC1)
Transfer space		512 MB (external areas from 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)	512 MB (external areas from 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)
Maximum transfer volume		1 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 1,024 blocks)	1 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 1,024 blocks)
DMA request sources		Activation source selectable from the following three sources for each channel: • Software trigger • External DMA transfer request input • DMA transfer request from peripheral module (compare match A of MTU1 or TPU7)	Activation source selectable from the following three sources for each channel: • Software trigger • External DMA transfer request input • DMA transfer request from peripheral module (TPU1.TRGA or MTU1.TRGA) (Channel 0: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR144 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR208; Channel 1: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR145 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR209)
Channel priority		Channel 0 > channel 1 (channel 0: highest)	Channel 0 > channel 1 (channel 0: highest)
Transfer data	Single data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data units: 1 to 1,024 data units	Number of data units: 1 to 1,024 data units
	Cluster size	Number of data units: 1 to 8 data units	Number of data units: 1 to 8 data units
Transfer modes	Normal transfer mode	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.

Item		RX63N (EXDMACa)	RX671 (EXDMACa)
Transfer modes	Repeat transfer mode	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units
	Block transfer mode	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units
	Cluster transfer	• Transfer of one data cluster per DMA transfer request • Maximum settable cluster size: 8 data units (32 bytes)	• Transfer of one data cluster per DMA transfer request • Maximum settable cluster size: 8 data units (32 bytes)
Address modes	Single address mode	• Transfers data by accessing the transfer source or destination peripheral device with the EDACKn (n = 0 or 1) signal and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.	• Transfers data by accessing the transfer source or destination peripheral device with the EDACKn (n = 0 or 1) signal and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.
	Dual address mode	• Transfers data by specifying the addresses of the transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.	• Transfers data by specifying the addresses of the transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX63N (EXDMACa)	RX671 (EXDMACa)
Interrupt requests	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	• Generated when the specified number of transfers is completed in normal transfer mode • Generated when the specified repeat count of transfers is completed in repeat transfer mode • Generated when the specified block count of transfers is completed in block transfer mode • Generated on completion of the specified cluster count of transfers in cluster transfer mode
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Low power consumption function		Module stop state can be set.	Module stop state can be set.

Table 2.28 Comparison of EXDMA Controller Registers

Register	Bit	RX63N (EXDMAa)	RX671 (EXDMAa)
EDMTMD	DCTG[1:0]	Transfer request source select bits b1 b0 0 0: Software 0 1: Setting prohibited. 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer requests from peripheral modules (compare match A of MTU1 or TPU7)	Transfer request source select bits b1 b0 0 0: Software 0 1: Setting prohibited. 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer requests from peripheral modules (TPU1.TRGA or MTU1.TRGA)

2.16 Data Transfer Controller

Table 2.29 is a comparative overview of data transfer controllers, and Table 2.30 is a comparison of data transfer controller registers.

Table 2.29 Comparative Overview of Data Transfer Controllers

Item	RX63N (DTCa)	RX671 (DTCb)
Transfer channels	Data can be transferred on a channel corresponding to the interrupt source (transferred by DTC activation request from the ICU)	The number of channels is equal to the total number of interrupt sources that can activate the DTC.
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum repeat size is 256 data units. • Block transfer mode — A single activation leads to the transfer of a single block. — The maximum block size is 256 data units.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer	• Multiple data transfers can be initiated by a single transfer request (chain transfer). • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.	• Multiple types of data transfers can be initiated by a single transfer request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Sequence transfer	—	A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).

Item	RX63N (DTCa)	RX671 (DTCb)
Transfer space	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Length of a single data unit: 8, 16, or 32 bits • Number of data units in a single block: 1 to 256 data units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Event link function	—	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Transfer information read skip can be executed.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When “fixed” is selected for transfer source address or transfer destination address, write-back skip is executed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Allows disabling the write-back of transfer information.
Displacement addition	—	The displacement value can be added to the transfer source address (for each transfer information)
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state

Table 2.30 Comparison of Data Transfer Controller Registers

Register	Bit	RX63N (DTCa)	RX671 (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCVBR	—	DTC vector base register (b31 to b0) Writes to the upper 4 bits are ignored, and the address of the register is extended by the value specified in b27. In addition, the lower 12 bits are reserved, and their value is fixed at 0. The write value of these bits should be 0. The ranges 0000 0000h to 07FF F000h and F800 0000h to FFFF F000h can be set in 4 KB units.	DTC vector base register (b31 to b0) Writes to the upper 4 bits are ignored, and the address of the register is extended by the value specified in b27. In addition, the lower 10 bits are reserved, and their value is fixed at 0. The write value of these bits should be 0. The ranges 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h can be set in 1 KB units.
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.17 I/O Ports

Table 2.31 to Table 2.34 are comparative overviews of I/O ports, Table 2.35 is comparison of I/O port functions, and Table 2.36 is a comparison of I/O port registers.

Table 2.31 Comparative Overview of I/O Ports on 145- and 144-Pin Packages

Port Symbol	RX63N (145-, 144-Pin)	RX671 (145-, 144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77*1
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5
PORTH	—	PH1, PH2
PORTJ	PJ3, PJ5	PJ3, PJ5

Note: 1. The 145-pin TFLGA (0.65 mm pitch) product does not have pins P71 and P72.

Table 2.32 Comparative Overview of I/O Ports on 100-Pin Packages

Port Symbol	RX63N (100-Pin)	RX671 (100-Pin)
PORT0	P05, P07	P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	—	PH1, PH2
PORTJ	PJ3	PJ3

Table 2.33 Comparative Overview of I/O Ports on 64-Pin Packages

Port Symbol	RX631 (64-Pin)*1		RX671 (64-Pin)
	LQFP	TFLGA	
PORT0	P05	P05	P05*2
PORT1	P14 to P17	P14 to P17	P12, P13, P16, P17
PORT2	P26, P27	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37	P30, P31, P34 to P37
PORT4	P40 to P44, P46	P40 to P44, P46	P40 to P43
PORT5	P54, P55	—	P53
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6	PA1, PA2, PA4, PA6, PA7
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7	PB5 to PB7
PORTC	PC2 to PC7	PC2 to PC6	PC0, PC1, PC4 to PC7
PORTD	—	—	PD2 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE2, PE6, PE7
PORTH	—	—	PH1, PH2

Notes: 1. The RX63N Group is not available in a 64-pin package.
2. Not present on the 64-pin TFBGA product.

Table 2.34 Comparative Overview of I/O Ports on 48-Pin Packages

Port Symbol	RX63N (48-Pin)	RX671 (48-Pin)
PORT1	P14 to P17	P12, P13, P16, P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P34 to P37
PORT4	P40 to P42, P46	P40 to P43
PORTA	PA1, PA3, PA4, PA6	PA1, PA2, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB5 to PB7
PORTC	PC4 to PC7	PC4 to PC7
PORTD	—	PD2 to PD5
PORTE	PE1 to PE4	PE6, PE7

Table 2.35 Comparison of I/O Port Functions

Item	Port Symbol	RX63N		RX671
		64-, 48-Pin	177-, 176-, 145-, 144-, 100-Pin	
Input pull-up function	PORT0	P05	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P14 to P17	P10 to P17	P12 to P17
	PORT2	P26, P27	P20 to P27	P20 to P27
	PORT3	P30 to P31, P36, P37	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P44, P46	P40 to P47	P40 to P47
	PORT5	P54, P55	P50 to P57	P50 to P56
	PORT6	—	P60 to P67	P60 to P67
	PORT7	—	P70 to P77	P70 to P77
	PORT8	—	P80 to P87	P80 to P83, P86, P87
	PORT9	—	P90 to P97	P90 to P93
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0 to PA7	PA0 to PA7
	PORTB	PB0, PB1, PB3, PB5 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	PC2 to PC7	PC0 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE5	PE0 to PE7	PE0 to PE7
	PORTF	—	PF0 to PF5	PF5
	PORTG	—	PG0 to PG7	—
	PORTH	—	—	PH1, PH2
	PORTJ	—	PJ3, PJ5	PJ3, PJ5
Open-drain output function	PORT0	P05	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P14 to P17	P10 to P17	P12 to P17
	PORT2	P26, P27	P20 to P27	P20 to P27
	PORT3	P30 to P31, P36, P37	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P44, P46	P40 to P47	P40 to P47
	PORT5	P54, P55	P50 to P57	P50 to P56
	PORT6	—	P60 to P67	P60 to P67
	PORT7	—	P70 to P77	P70 to P77
	PORT8	—	P80 to P87	P80 to P83, P86, P87
	PORT9	—	P90 to P97	P90 to P93
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0 to PA7	PA0 to PA7
	PORTB	PB0, PB1, PB3, PB5 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	PC2 to PC7	PC0 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE5	PE0 to PE7	PE0 to PE7
	PORTF	—	PF0 to PF5	PF5
	PORTG	—	PG0 to PG7	—
	PORTH	—	—	PH1, PH2
	PORTJ	—	PJ3, PJ5	PJ3, PJ5

Item	Port Symbol	RX63N		RX671
		64-, 48-Pin	177-, 176-, 145-, 144-, 100-Pin	
Drive capacity switching function	PORT0	P05	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P14 to P17	P10 to P17	P12 to P17
	PORT2	P26, P27	P20 to P27	P20 to P27
	PORT3	P30 to P31, P36, P37	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P44, P46	P40 to P47	P40 to P47
	PORT5	P54, P55	P50 to P57	P50 to P56
	PORT6	—	P60 to P67	P60 to P67
	PORT7	—	P70 to P77	P70 to P77
	PORT8	—	P80 to P87	P80 to P83, P86, P87
	PORT9	—	P90 to P97	P90 to P93
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0 to PA7	PA0 to PA7
	PORTB	PB0, PB1, PB3, PB5 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	PC2 to PC7	PC0 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE5	PE0 to PE7	PE0 to PE7
	PORTF	—	PF0 to PF5	PF5
	PORTG	—	PG0 to PG7	—
	PORTH	—	—	PH1, PH2
	PORTJ	—	PJ3, PJ5	PJ3, PJ5
5 V tolerant	PORT0	—	P07	P07
	PORT1	P14 to P17	P12 to P17	P12 to P17
	PORT2	—	P20, P21	P20, P21
	PORT3	P30 to P31	P30 to P33	P30 to P33
	PORT6	—	P67	P67
	PORT7	—	—	P73
	PORTC	PC2 to PC3	PC0 to PC3	PC0 to PC3
	PORTJ	—	—	PJ3

Table 2.36 Comparison of I/O Port Registers

Register	Bit	RX63N	RX671
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, J)
ODR0	B0	Pm0 output type select bit (m = 0 to 9, A to G, J)	Pm0 output type select bit (m = 0 to 9, A to E, H, J)
	B2	Pm1 output type select bit (m = 0 to 9, A to G, J)	Pm1 output type select bit (m = 0 to 9, A to E, H, J)
	B3	—	PE1 output type select bit Bits for pins other than port PE1 pins are reserved.
	B4	Pm2 output type select bit (m = 0 to 9, A to G, J)	Pm2 output type select bit (m = 0 to 9, A to E, H, J)
	B6	Pm3 output type select bit (m = 0 to 9, A to G, J)	Pm3 output type select bit (m = 0 to 9, A to E, H, J)
ODR1	B0	Pm4 output type select bit (m = 0 to 9, A to G, J)	Pm4 output type select bit (m = 0 to 8, A to F, J)
	B2	Pm5 output type select bit (m = 0 to 9, A to G, J)	Pm5 output type select bit (m = 0 to 8, A to F, J)
	B4	Pm6 output type select bit (m = 0 to 9, A to G, J)	Pm6 output type select bit (m = 0 to 8, A to F, J)
	B6	Pm7 output type select bit (m = 0 to 9, A to G, J)	Pm7 output type select bit (m = 0 to 8, A to F, J)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, G)	Pm0 to Pm7 drive capacity control bits (m = 0 to 2, 5, 7 to 9, A to E, H)
DSCR2	—	—	Drive capacity control register 2
PSRA	—	Port switching register A RX631 products in 64-pin packages incorporate the PSRA register.	—
PSRB	—	Port switching register B RX631 products in 48-pin packages incorporate the PSRB register.	—

2.18 Multi-Function Pin Controller

Table 2.37 is a comparison of the assignments of multiplexed pins, and Table 2.38 to Table 2.55 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **blue text** designates pins that exist on the RX671 Group only and **orange text** pins that exist on the RX63N Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.37 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/144-Pin	100-Pin	64-Pin	48-Pin	145-/144-Pin	100-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○	○	○
EXDMA controller	EDREQ0 (input)	P22	○	○	×	×	○	○	×	×
		P55	○	○	×	×	○	○	×	×
		P80	○	×	×	×	○	×	×	×
	EDACK0 (output)	P23	○	○	×	×	○	○	×	×
		P54	○	○	×	×	○	○	×	×
		P81	○	×	×	×	○	×	×	×
	EDREQ1 (input)	P24	○	○	×	×	○	○	×	×
		P82	○	×	×	×	○	×	×	×
		P33	×	×	×	×	○	○	×	×
	EDACK1 (output)	P25	○	○	×	×	○	○	×	×
		P56	○	×	×	×	○	×	×	×
		P83	○	×	×	×	○	×	×	×
		PJ3	×	×	×	×	○	○	×	×
Interrupt	IRQ0-DS (input)	P30	○	○	○	○	○	○	○	○
	IRQ0 (input)	PD0	○	○	×	×	○	○	×	×
		P50	×	×	×	×	○	○	×	×
		P60	×	×	×	×	○	×	×	×
		P70	×	×	×	×	○	×	×	×
		P90	×	×	×	×	○	×	×	×
		PA0	×	×	×	×	○	○	×	×
		PH1	×	×	×	×	○	○	○	×
	IRQ1-DS (input)	P31	○	○	○	○	○	○	○	○
	IRQ1 (input)	PD1	○	○	×	×	○	○	×	×
		P51	×	×	×	×	○	○	×	×
		P61	×	×	×	×	○	×	×	×
		P71	×	×	×	×	○ *5	×	×	×
		PH2	×	×	×	×	○	○	○	×
	IRQ2-DS (input)	P32	○	○	×	×	○	○	×	×
	IRQ2 (input)	P12	○	○	×	×	○	○	○	○
		PD2	○	○	×	×	○	○	○	○
		P52	×	×	×	×	○	○	×	×
		P62	×	×	×	×	○	×	×	×
		P82	×	×	×	×	○	×	×	×
		PB2	×	×	×	×	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Interrupt	IRQ3-DS (input)	P33	○	○	×	×	○	○	×	×
	IRQ3 (input)	P13	○	○	×	×	○	○	○	○
		PD3	○	○	×	×	○	○	○	○
		P23	×	×	×	×	○	○	×	×
		P53	×	×	×	×	○	○	○	○
		P63	×	×	×	×	○	×	×	×
		P83	×	×	×	×	○	×	×	×
		PB3	×	×	×	×	○	○	×	×
	IRQ4-DS (input)	PB1	○	○	○	○	○	○	×	×
	IRQ4 (input)	P14	○	○	○	○	○	○	×	×
		P34	○	○	×	×	○	○	○	○
		PD4	○	○	×	×	○	○	○	○
		PF5	○	×	×	×	○	×	×	×
		P54	×	×	×	×	○	○	×	×
		P64	×	×	×	×	○	×	×	×
		PB4	×	×	×	×	○	○	×	×
	IRQ5-DS (input)	PA4	○	○	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	○	○	○	○	×	×
		PD5	○	○	×	×	○	○	○	○
		PE5	○	○	○	×	○	○	×	×
		P25	×	×	×	×	○	○	×	×
		PA5	×	×	×	×	○	○	×	×
		PC5	×	×	×	×	○	○	○	○
	IRQ6-DS (input)	PA3	○	○	○	○	○	○	×	×
	IRQ6 (input)	P16	○	○	○	○	○	○	○	○
		PD6	○	○	×	×	○	○	○	×
		PE6	○	○	×	×	○	○	○	○
		P26	×	×	×	×	○	○	○	○
		P56	×	×	×	×	○	×	×	×
		PB6	×	×	×	×	○	○	○	○
	IRQ7-DS (input)	PE2	○	○	○	○	○	○	○	×
	IRQ7 (input)	P17	○	○	○	○	○	○	○	○
		PD7	○	○	×	×	○	○	○	×
		PE7	○	○	×	×	○	○	○	○
		P27	×	×	×	×	○	○	○	○
		P77	×	×	×	×	○	×	×	×
		PA7	×	×	×	×	○	○	○	×
	IRQ8-DS (input)	P40	○	○	○	○	○	○	○	○
	IRQ8 (input)	P00	○	×	×	×	○	×	×	×
		P20	○	○	×	×	○	○	×	×
		P73	×	×	×	×	○	×	×	×
		P80	×	×	×	×	○	×	×	×
		PE0	×	×	×	×	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Interrupt	IRQ9-DS (input)	P41	○	○	○	○	○	○	○	○
	IRQ9 (input)	P01	○	×	×	×	○	×	×	×
		P21	○	○	×	×	○	○	×	×
		P81	×	×	×	×	○	×	×	×
		P91	×	×	×	×	○	×	×	×
		PE1	×	×	×	×	○	○	○	×
	IRQ10-DS (input)	P42	○	○	○	○	○	○	○	○
	IRQ10 (input)	P02	○	×	×	×	○	×	×	×
		P55	○	○	○ *2	×	○	○	×	×
		P72	×	×	×	×	○ *5	×	×	×
		P92	×	×	×	×	○	×	×	×
		PA2	×	×	×	×	○	○	○	○
		PC2	×	×	×	×	○	○	×	×
	IRQ11-DS (input)	P43	○	○	○	×	○	○	○	○
	IRQ11 (input)	P03	○	×	×	×	○	×	×	×
		PA1	○	○	○	○	○	○	○	○
		P93	×	×	×	×	○	×	×	×
		PC3	×	×	×	×	○	○	×	×
		PE3	×	×	×	×	○	○	×	×
		PJ3	×	×	×	×	○	○	×	×
	IRQ12-DS (input)	P44	○	○	○	×	○	○	×	×
	IRQ12 (input)	PB0	○	○	○	○	○	○	×	×
		PC1	○	○	×	×	○	○	○	×
		P24	×	×	×	×	○	○	×	×
		P74	×	×	×	×	○	×	×	×
		PC4	×	×	×	×	○	○	○	○
		PE4	×	×	×	×	○	○	×	×
	IRQ13-DS (input)	P45	○	○	×	×	○	○	×	×
	IRQ13 (input)	P05	○	○	○	×	○	○	○ *6	×
		PC6	○	○	○	○	○	○	○	○
		P65	×	×	×	×	○	×	×	×
		P75	×	×	×	×	○	×	×	×
		PB5	×	×	×	×	○	○	○	○
		PJ5	×	×	×	×	○	×	×	×
	IRQ14-DS (input)	P46	○	○	○	○	○	○	×	×
	IRQ14 (input)	PC0	○	○	×	×	○	○	○	×
		PC7	○	○	○ *2	○	○	○	○	○
		P66	×	×	×	×	○	×	×	×
		P76	×	×	×	×	○	×	×	×
		P86	×	×	×	×	○	×	×	×
		PA6	×	×	×	×	○	○	○	○
	IRQ15-DS (input)	P47	○	○	×	×	○	○	×	×
	IRQ15 (input)	P07	○	○	×	×	○	○	×	×
		P67	○	×	×	×	○	×	×	×
		P22	×	×	×	×	○	○	×	×
		P87	×	×	×	×	○	×	×	×
		PB7	×	×	×	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Multi-function timer units 2 and 3	MTIOC0A (input/output)	P34	○	○	×	×	○	○	○	○
		PB3	○	○	○	○	○	○	×	×
	MTIOC0B (input/output)	P13	○	○	×	×	○	○	○	○
		P15	○	○	○	○	○	○	×	×
		PA1	○	○	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	×	×
	MTIOC0D (input/output)	P33	○	○	×	×	○	○	×	×
		PA3	○	○	○	○	○	○	×	×
	MTIOC1A (input/output)	P20	○	○	×	×	○	○	×	×
		PE4	○	○	○	○	○	○	×	×
	MTIOC1B (input/output)	P21	○	○	×	×	○	○	×	×
		PB5	○	○	○	○	○	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○	○	○
		PB5	○	○	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○	○	○
		PE5	○	○	○	×	○	○	×	×
	MTIOC3A (input/output)	P14	○	○	○	○	○	○	×	×
		P17	○	○	○	○	○	○	○	○
		PC1	○	○	×	×	○	○	○	×
		PC7	○	○	○	○	○	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○	○	○	○	○
		P22	○	○	×	×	○	○	×	×
		P80	○	×	×	×	○	×	×	×
		PB7	○	○	○	×	○	○	○	○
		PC5	○	○	○*2	○	○	○	○	○
		PE1	×	×	×	×	○	○	○	×
	MTIOC3C (input/output)	P16	○	○	○	○	○	○	○	○
		P56	○	×	×	×	○	×	×	×
		PC0	○	○	×	×	○	○	○	×
		PC6	○	○	○	○	○	○	○	○
		PJ3	○	○	×	×	○	○	×	×
	MTIOC3D (input/output)	P16	○	○	○	○	○	○	○	○
		P23	○	○	×	×	○	○	×	×
		P81	○	×	×	×	○	×	×	×
		PB6	○	○	○	×	○	○	○	○
		PC4	○	○	○	○	○	○	○	○
		PE0	×	×	×	×	○	○	○	×
	MTIOC4A (input/output)	P24	○	○	×	×	○	○	×	×
		P82	○	×	×	×	○	×	×	×
		PA0	○	○	○	×	○	○	×	×
		PB3	○	○	○	○	○	○	×	×
		PE2	○	○	○	○	○	○	○	×
		P21	×	×	×	×	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Multi-function timer units 2 and 3	MTIOC4B (input/output)	P30	○	○	○	○	○	○	○	○
		P54	○	○	○ *2	×	○	○	×	×
		PC2	○	○	○	×	○	○	×	×
		PD1	○	○	×	×	○	○	×	×
		PE3	○	○	○	○	○	○	×	×
		P17	×	×	×	×	○	○	○	○
	MTIOC4C (input/output)	P25	○	○	×	×	○	○	×	×
		P83	○	×	×	×	○	×	×	×
		PB1	○	○	○	○	○	○	×	×
		PE1	○	○	○	○	○	○	○	×
		PE5	○	○	○	×	○	○	×	×
		P87	×	×	×	×	○	×	×	×
	MTIOC4D (input/output)	P31	○	○	○	○	○	○	○	○
		P55	○	○	○ *2	×	○	○	×	×
		PC3	○	○	○	×	○	○	×	×
		PD2	○	○	×	×	○	○	○	○
		PE4	○	○	○	○	○	○	×	×
		P86	×	×	×	×	○	×	×	×
	MTIC5U (input)	P12	×	×	×	×	○	○	○	○
		PA4	○	○	○	○	○	○	○	○
		PD7	○	○	×	×	○	○	○	×
	MTIC5V (input)	PA6	○	○	○	○	○	○	○	○
		PD6	○	○	×	×	○	○	○	×
	MTIC5W (input)	PB0	○	○	○	○	○	○	×	×
		PD5	○	○	×	×	○	○	○	○
	MTIOC6A (input/output)	PE7					○	○	○	○
	MTIOC6B (input/output)	PA5					○	○	×	×
	MTIOC6C (input/output)	PE6					○	○	○	○
	MTIOC6D (input/output)	PA0					○	○	×	×
	MTIOC7A (input/output)	PA2					○	○	○	○
	MTIOC7B (input/output)	PA1					○	○	○	○
	MTIOC7C (input/output)	P67					○	×	×	×
	MTIOC7D (input/output)	P66					○	×	×	×
	MTIOC8A (input/output)	PD6					○	○	○	×
	MTIOC8B (input/output)	PD4					○	○	○	○
	MTIOC8C (input/output)	PD5					○	○	○	○
	MTIOC8D (input/output)	PD3					○	○	○	○
	MTCLKA (input)	P14	○	○	○	○	○	○	×	×
		P24	○	○	×	×	○	○	×	×
		PA4	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○	○	○	×	×
		P25	○	○	×	×	○	○	×	×
		PA6	○	○	○	○	○	○	○	○
		PC7	○	○	○ *2	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Multi-function timer units 2 and 3	MTCLKC (input)	P22	○	○	×	×	○	○	×	×
		PA1	○	○	○	○	○	○	○	○
		PC4	○	○	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	×	×	○	○	×	×
		PA3	○	○	○	○	○	○	×	×
		PC5	○	○	○	○	○	○	○	○
Port output enable 2 and 3	POE0# (input)	PC4	○	○	○	○	○	○	○	○
		PD7	○	○	×	×	○	○	○	×
		P32	×	×	×	×	○	○	×	×
		P93	×	×	×	×	○	×	×	×
		PD1	×	×	×	×	○	○	×	×
	POE1# (input)	PB5	○	○	○	○				
		PD6	○	○	×	×				
	POE2# (input)	P34	○	○	×	×				
		PA6	○	○	○	○				
		PD5	○	○	×	×				
	POE3# (input)	P33	○	○	×	×				
		PB3	○	○	○	○				
		PD4	○	○	×	×				
	POE4# (input)	P33					○	○	×	×
		P92					○	×	×	×
		PB5					○	○	○	○
		PD0					○	○	×	×
		PD6					○	○	○	×
	POE8# (input)	P17	○	○	○	○	○	○	○	○
		P30	○	○	○	○	○	○	○	○
		PD3	○	○	×	×	○	○	○	○
		PE3	○	○	○	○	○	○	×	×
		PJ5	×	×	×	×	○	×	×	×
	POE10# (input)	P32					○	○	×	×
		P34					○	○	○	○
		PA6					○	○	○	○
		PD5					○	○	○	○
	POE11# (input)	P33					○	○	×	×
		PB3					○	○	×	×
		PD4					○	○	○	○
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	×	×	×	○	×	×	×
		PA0	○	○	○	×	○	○	×	×
	TIOCB0 (input/output)	P17	○	○	○	○	○	○	○	○
		PA1	○	○	○	○	○	○	○	○
	TIOCC0 (input/output)	P32	○	○	×	×	○	○	×	×
	TIOCD0 (input/output)	P33	○	○	×	×	○	○	×	×
		PA3	○	○	○	○	○	○	×	×
	TIOCA1 (input/output)	P56	○	×	×	×	○	×	×	×
		PA4	○	○	○	○	○	○	○	○
	TIOCB1 (input/output)	P16	○	○	○	○	○	○	○	○
		PA5	○	○	×	×	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
16-bit timer pulse unit	TIOCA2 (input/output)	P87	○	×	×	×	○	×	×	×
		PA6	○	○	○	○	○	○	○	○
	TIOCB2 (input/output)	P15	○	○	○	○	○	○	×	×
		PA7	○	○	×	×	○	○	○	×
	TIOCA3 (input/output)	P21	○	○	×	×	○	○	×	×
		PB0	○	○	○	○	○	○	×	×
	TIOCB3 (input/output)	P20	○	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	×	×
	TIOCC3 (input/output)	P22	○	○	×	×	○	○	×	×
		PB2	○	○	×	×	○	○	×	×
	TIOCD3 (input/output)	P23	○	○	×	×	○	○	×	×
		PB3	○	○	○	○	○	○	×	×
	TIOCA4 (input/output)	P25	○	○	×	×	○	○	×	×
		PB4	○	○	×	×	○	○	×	×
	TIOCB4 (input/output)	P24	○	○	×	×	○	○	×	×
		PB5	○	○	○	○	○	○	○	○
	TIOCA5 (input/output)	P13	○	○	×	×	○	○	○	○
		PB6	○	○	○	×	○	○	○	○
	TIOCB5 (input/output)	P14	○	○	○	○	○	○	×	×
		PB7	○	○	○	×	○	○	○	○
	TCLKA (input)	P14	○	○	○	○	○	○	×	×
		PC2	○	○	○	×	○	○	×	×
	TIOCA6 (input/output)	PC6	○	×	×	×				
	TIOCB6 (input/output)	PC7	○	×	×	×				
	TIOCC6 (input/output)	PC4	○	×	×	×				
	TIOCD6 (input/output)	PC5	○	×	×	×				
	TIOCA7 (input/output)	PD0	○	×	×	×				
	TIOCB7 (input/output)	PD1	○	×	×	×				
	TIOCA8 (input/output)	PD2	○	×	×	×				
	TIOCB8 (input/output)	PD3	○	×	×	×				
	TIOCA9 (input/output)	PE2	○	×	×	×				
	TIOCB9 (input/output)	PE3	○	×	×	×				
	TIOCC9 (input/output)	PE0	○	×	×	×				
	TIOCD9 (input/output)	PE1	○	×	×	×				
	TIOCA10 (input/output)	PE4	○	×	×	×				
	TIOCB10 (input/output)	PE5	○	×	×	×				
	TIOCA11 (input/output)	PE6	○	×	×	×				
	TIOCB11 (input/output)	PE7	○	×	×	×				
	TCLKA (input)	P14	○	○	○	○	○	○	×	×
		PC2	○	○	○	×	○	○	×	×
	TCLKB (input)	P15	○	○	○	○	○	○	×	×
		PA3	○	○	○	○	○	○	×	×
		PC3	○	○	○	×	○	○	×	×
	TCLKC (input)	P16	○	○	○	○	○	○	○	○
		PB2	○	○	×	×	○	○	×	×
		PC0	○	○	×	×	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
16-bit timer pulse unit	TCLKD (input)	P17	○	○	○	○	○	○	○	○
		PB3	○	○	○	○	○	○	×	×
		PC1	○	○	×	×	○	○	○	×
	TCLKE (input)	PC4	○	×	×	×				
	TCLKF (input)	PC5	○	×	×	×				
	TCLKG (input)	PD1	○	×	×	×				
	TCLKH (input)	PD3	○	×	×	×				
Programmable pulse generator	PO0 (output)	P20	○	○	×	×	○	○	×	×
	PO1 (output)	P21	○	○	×	×	○	○	×	×
	PO2 (output)	P22	○	○	×	×	○	○	×	×
	PO3 (output)	P23	○	○	×	×	○	○	×	×
	PO4 (output)	P24	○	○	×	×	○	○	×	×
	PO5 (output)	P25	○	○	×	×	○	○	×	×
	PO6 (output)	P26	○	○	○	○	○	○	×	×
	PO7 (output)	P27	○	○	○	○	○	○	×	×
	PO8 (output)	P30	○	○	○	○	○	○	×	×
	PO9 (output)	P31	○	○	○	○	○	○	×	×
	PO10 (output)	P32	○	○	×	×	○	○	×	×
	PO11 (output)	P33	○	○	×	×	○	○	×	×
	PO12 (output)	P34	○	○	×	×	○	○	×	×
	PO13 (output)	P13	○	○	×	×	○	○	×	×
		P15	○	○	○	○	○	○	×	×
	PO14 (output)	P16	○	○	○	○	○	○	×	×
	PO15 (output)	P14	○	○	○	○	○	○	×	×
		P17	○	○	○	○	○	○	×	×
	PO16 (output)	P73	○	×	×	×	○	×	×	×
		PA0	○	○	○	×	○	○	×	×
	PO17 (output)	PA1	○	○	○	○	○	○	×	×
		PC0	○	○	×	×	○	○	×	×
	PO18 (output)	PA2	○	○	×	×	○	○	×	×
		PC1	○	○	×	×	○	○	×	×
		PE1	○	○	○	○	○	○	×	×
	PO19 (output)	P74	○	×	×	×	○	×	×	×
		PA3	○	○	○	○	○	○	×	×
	PO20 (output)	P75	○	×	×	×	○	×	×	×
		PA4	○	○	○	○	○	○	×	×
	PO21 (output)	PA5	○	○	×	×	○	○	×	×
		PC2	○	○	○	×	○	○	×	×
	PO22 (output)	P76	○	×	×	×	○	×	×	×
		PA6	○	○	○	○	○	○	×	×
	PO23 (output)	P77	○	×	×	×	○	×	×	×
		PA7	○	○	×	×	○	○	×	×
		PE2	○	○	○	○	○	○	×	×
	PO24 (output)	PB0	○	○	○	○	○	○	×	×
		PC3	○	○	○	×	○	○	×	×
	PO25 (output)	PB1	○	○	○	○	○	○	×	×
		PC4	○	○	○	○	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Programmable pulse generator	PO26 (output)	P80	○	×	×	×	○	×	×	×
		PB2	○	○	×	×	○	○	×	×
		PE3	○	○	○	○	○	○	×	×
	PO27 (output)	P81	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	×	×
	PO28 (output)	P82	○	×	×	×	○	×	×	×
		PB4	○	○	×	×	○	○	×	×
		PE4	○	○	○	○	○	○	×	×
	PO29 (output)	PB5	○	○	○	○	○	○	×	×
		PC5	○	○	○	○	○	○	×	×
	PO30 (output)	PB6	○	○	○	×	○	○	×	×
		PC6	○	○	○	○	○	○	×	×
	PO31 (output)	PB7	○	○	○	×	○	○	×	×
		PC7	○	○	○ *2	○	○	○	×	×
8-bit timer	TMO0 (output)	P22	○	○	×	×	○	○	×	×
		PB3	○	○	○	○	○	○	×	×
		PH1	×	×	×	×	○	○	○	×
	TMCI0 (input)	P01	○	×	×	×	○	×	×	×
		P21	○	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	×	×
	TMRI0 (input)	P00	○	×	×	×	○	×	×	×
		P20	○	○	×	×	○	○	×	×
		PA4	○	○	○	○	○	○	○	○
		PH2	×	×	×	×	○	○	○	×
	TMO1 (output)	P17	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	TMCI1 (input)	P02	○	×	×	×	○	×	×	×
		P12	○	○	×	×	○	○	○	○
		P54	○	○	○ *2	×	○	○	×	×
		PC4	○	○	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	×	×	○	○	×	×
		PB5	○	○	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○	○	○
		PC7	○	○	○ *2	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○	×	×
		P31	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○	×	×
		PC5	○	○	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	×	×	○	○	○	○
		P32	○	○	×	×	○	○	×	×
		P55	○	○	○ *2	×	○	○	×	×
	TMCI3 (input)	P27	○	○	○	○	○	○	○	○
		P34	○	○	×	×	○	○	○	○
		PA6	○	○	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○	○	○
		P33	○	○	×	×	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Ethernet controller	REF50CK (input)	P76	○	×	×	×				
		PB2	○	○	×	×				
		PE5	○	○	×	×				
	RMII_CRS_DV (input)	P83	○	×	×	×				
		PB7	○	○	×	×				
	RMII_TXD0 (output)	P81	○	×	×	×				
		PB5	○	○	×	×				
	RMII_TXD1 (output)	P82	○	×	×	×				
		PB6	○	○	×	×				
	RMII_RXD0 (input)	P75	○	×	×	×				
		PB1	○	○	×	×				
	RMII_RXD1 (input)	P74	○	×	×	×				
		PB0	○	○	×	×				
	RMII_TXD_EN (output)	P80	○	×	×	×				
		PA0	○	○	×	×				
		PB4	○	○	×	×				
	RMII_RX_ER (input)	P77	○	×	×	×				
		PB3	○	○	×	×				
	ET_CRS (input)	P83	○	×	×	×				
		PB7	○	○	×	×				
	ET_RX_DV (input)	PC2	○	○	×	×				
	ET_EXOUT (output)	P55	○	○	×	×				
		PA6	○	○	×	×				
	ET_LINKSTA (input)	P54	○	○	×	×				
		PA5	○	○	×	×				
	ET_ETXD0 (output)	P81	○	×	×	×				
		PB5	○	○	×	×				
	ET_ETXD1 (output)	P82	○	×	×	×				
		PB6	○	○	×	×				
	ET_ETXD2 (output)	PC5	○	○	×	×				
	ET_ETXD3 (output)	PC6	○	○	×	×				
	ET_ERXD0 (input)	P75	○	×	×	×				
		PB1	○	○	×	×				
	ET_ERXD1 (input)	P74	○	×	×	×				
		PB0	○	○	×	×				
	ET_ERXD2 (input)	PC1	○	○	×	×				
		PE4	○	○	×	×				
	ET_ERXD3 (input)	PC0	○	○	×	×				
		PE3	○	○	×	×				
	ET_TX_EN (output)	P80	○	×	×	×				
		PA0	○	○	×	×				
		PB4	○	○	×	×				
	ET_TX_ER (output)	PC3	○	○	×	×				
	ET_RX_ER (input)	P77	○	×	×	×				
		PB3	○	○	×	×				

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Ethernet controller	ET_TX_CLK (input)	PC4	○	○	×	×				
	ET_RX_CLK (input)	P76	○	×	×	×				
		PB2	○	○	×	×				
		PE5	○	○	×	×				
	ET_COL (input)	PC7	○	○	×	×				
	ET_WOL (output)	P73	○	×	×	×				
		PA1	○	○	×	×				
		PA7	○	○	×	×				
	ET_MDC (output)	P72	○	×	×	×				
		PA4	○	○	×	×				
	ET_MDIO (input/output)	P71	○	×	×	×				
		PA3	○	○	×	×				
Serial communications interface	RXD0 (input) / SMISO0 (input/output) / SSCL0 (input/output)	P21	○	○	×	×	○	○	×	×
		P33	○	○	×	×	○	○	×	×
	TXD0 (output) / SMOSI0 (input/output) / SSDA0 (input/output)	P20	○	○	×	×	○	○	×	×
		P32	○	○	×	×	○	○	×	×
	SCK0 (input/output)	P22	○	○	×	×	○	○	×	×
		P34	○	○	×	×	○	○	×	×
	CTS0# (input) / RTS0# (output) / SS0# (input)	P23	○	○	×	×	○	○	×	×
		PJ3	○	○	×	×	○	○	×	×
	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	○	○	○	○	○	×	×
		P30	○	○	○	○	○	○	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○	○	○
		P27	○	○	○	○	○	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	○	○	○	○	×	×
		P31	○	○	○	○	○	○	○	○
	RXD2 (input) / SMISO2 (input/output) / SSCL2 (input/output)	P12	○	○	×	×	○	○	○	○
		P52	○	○	×	×	○	○	×	×
	TXD2 (output) / SMOSI2 (input/output) / SSDA2 (input/output)	P13	○	○	×	×	○	○	○	○
		P50	○	○	×	×	○	○	×	×
	SCK2 (input/output)	P51	○	○	×	×	○	○	×	×
	CTS2# (input) / RTS2# (output) / SS2# (input)	P54	○	○	×	×	○	○	×	×
		PJ5	×	×	×	×	○	×	×	×
	RXD3 (input) / SMISO3 (input/output) / SSCL3 (input/output)	P16	○	○	×	×	○	○	○	○
		P25	○	○	×	×	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Serial communications interface	TXD3 (output) / SMOSI3 (input/output) / SSDA3 (input/output)	P17	○	○	×	×	○	○	○	○
		P23	○	○	×	×	○	○	×	×
	SCK3 (input/output)	P15	○	○	×	×	○	○	×	×
		P24	○	○	×	×	○	○	×	×
	CTS3# (input) / RTS3# (output) / SS3# (input)	P26	○	○	×	×	○	○	○	○
	RXD4 (input) / SMISO4 (input/output) / SSCL4 (input/output)	PB0	○	×	×	×	○	×	×	×
	TXD4 (output) / SMOSI4 (input/output) / SSDA4 (input/output)	PB1	○	×	×	×	○	×	×	×
	SCK4 (input/output)	PB3	○	×	×	×	○	×	×	×
	CTS4# (input) / RTS4# (output) / SS4# (input)	PB2	○	×	×	×	○	×	×	×
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA2	○	○	×	×	○	○	○	○
		PA3	○	○	○	○	○	○	×	×
		PC2	○	○	○	×	○	○	×	×
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC3	○	○	○	×	○	○	×	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	○	×	×	○	○	○	×
		PC4	○	○	○	○	○	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	○	○	○	○	○	○	○
		PC0	○	○	×	×	○	○	○	×
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	P01	○	×	×	×	○	×	×	×
		P33	○	○	×	×	○	○	×	×
		PB0	○	○	○	○	○	○	×	×
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	P00	○	×	×	×	○	×	×	×
		P32	○	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	×	×
	SCK6 (input/output)	P02	○	×	×	×	○	×	×	×
		P34	○	○	×	×	○	○	×	×
		PB3	○	○	○	○	○	○	×	×
	CTS6# (input) / RTS6# (output) / SS6# (input)	PB2	○	○	×	×	○	○	×	×
		PJ3	○	○	×	×	○	○	×	×
	RXD7 (input) / SMISO7 (input/output) / SSCL7 (input/output)	P92	○	×	×	×	○	×	×	×
	TXD7 (output) / SMOSI7 (input/output) / SSDA7 (input/output)	P90	○	×	×	×	○	×	×	×
		P55	×	×	×	×	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Serial communications interface	SCK7 (input/output)	P91	○	×	×	×	○	×	×	×
		P56	×	×	×	×	○	×	×	×
	CTS7# (input) / RTS7# (output) / SS7# (input)	P93	○	×	×	×	○	×	×	×
	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6	○	○	○*2	○	○	○	○	○
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7	○	○	○*2	○	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○*2	○	○	○	○	○
	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4	○	○	○*2	○	○	○	○	○
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6	○	○	○	×	○	○	○	○
	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7	○	○	○	×	○	○	○	○
	SCK9 (input/output)	PB5	○	○	○	×	○	○	○	○
	CTS9# (input) / RTS9# (output) / SS9# (input)	PB4	○	○	×	×	○	○	×	×
	RXD10 (input) / SMISO10 (input/output) / SSCL10 (input/output)	P81	○	×	×	×	○	×	×	×
		P86	×	×	×	×	○	×	×	×
		PC6	×	×	×	×	○	○	○	○
	TXD10 (output) / SMOSI10 (input/output) / SSDA10 (input/output)	P82	○	×	×	×	○	×	×	×
		P87	×	×	×	×	○	×	×	×
		PC7	×	×	×	×	○	○	○	○
	SCK10 (input/output)	P80	○	×	×	×	○	×	×	×
		P83	×	×	×	×	○	×	×	×
		PC5	×	×	×	×	○	○	○	○
	CTS10# (input) / RTS10# (output) / SS10# (input)	P83	○	×	×	×	×	×	×	×
		PC4	×	×	×	×	○	○	○	○
	RTS10# (output)	P80					○	×	×	×
	CTS10# (input) / SS10# (input)	P83					○	×	×	×
	RXD11 (input) / SMISO11 (input/output) / SSCL11 (input/output)	P76	○	×	×	×	○	×	×	×
		PB6	×	×	×	×	○	○	○	○
	TXD11 (output) / SMOSI11 (input/output) / SSDA11 (input/output)	P77	○	×	×	×	○	×	×	×
		PB7	×	×	×	×	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Serial communications interface	SCK11 (input/output)	P75	○	×	×	×	○	×	×	×
		PB5	×	×	×	×	○	○	○	○
	CTS11# (input) / RTS11# (output) / SS11# (input)	P74	○	×	×	×	×	×	×	×
		PB4	×	×	×	×	○	○	×	×
	RTS11# (output)	P75					○	×	×	×
	CTS11# (input) / SS11# (input)	P74					○	×	×	×
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○	○	○	○	○	○	○	×
		PA2	×	×	×	×	○	○	○	○
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○	○	○	○	○	○	○	×
		PA4	×	×	×	×	○	○	○	○
	SCK12 (input/output)	PE0	○	○	○	×	○	○	○	×
		PA1	×	×	×	×	○	○	○	○
	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○	○	○	○	○	○	×	×
		PA6	×	×	×	×	○	○	○	○
I²C bus interface	SCL0[FM+] (input/output)	P12	○	○	×	×	○	○	○	○
	SDA0[FM+] (input/output)	P13	○	○	×	×	○	○	○	○
	SCL1 (input/output)	P21	○	×	×	×	○	○	×	×
	SDA1 (input/output)	P20	○	×	×	×	○	○	×	×
	SCL2-DS (input/output)	P16	○	○	○	○	○	○	○	○
	SDA2-DS (input/output)	P17	○	○	○	○	○	○	○	○
	SCL3 (input/output)	PC0	○	×	×	×				
	SDA3 (input/output)	PC1	○	×	×	×				
USB 2.0 FS Host/Function module	USB0_VBUS (input)	P16	○	○	○	○	○	○	○	×
	USB0_EXICEN (output)	P21	○	○	×	×	○	○	×	×
		PC6	×	×	○	○	×	×	×	×
	USB0_VBUSEN (output)	P16	○	○	○	○	○	○	×	×
		P24	○	○	×	×	○	○	×	×
		P26	×	×	○	○	×	×	×	×
		P32	○	○	×	×	○	○	×	×
	USB0_OVRCUR (input)	P14	○	○	○	○	○	○	×	×
	USB0_OVRCURB (input)	P16	○	○	○	○	○	○	×	×
		P22	×	×	×	×	○	○	×	×
	USB0_ID (input)	P20	○	○	×	×	○	○	×	×
		PC5	×	×	○	○	×	×	×	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
USB 2.0 FS Host/Function module	USB0_DPUPE (output)	P14	○	○	○	○				
		P23	○	○	×	×				
		P31	○	○	○	○				
	USB0_DPRPD (output)	P25	○	○	×	×				
		P34	○	○	×	×				
		PC4	×	×	○	○				
	USB0_DP (input/output)*1	PH1					○	○	○	×
	USB0_DM (input/output)*1	PH2					○	○	○	×
	USB1_VBUS (input)	P73	×	×	×	×	○*7	×	×	×
		P17	×	×	○*3	×	×	×	×	×
	USB1_DPUPE (output)	P15	×	×	○*3	×				
	USB1_VBUSEN (output)	P73					○*7	×	×	×
		P74					○*7	×	×	×
		P82					○*7	×	×	×
	USB1_OVRCURA (input)	P75					○*7	×	×	×
	USB1_OVRCURB (input)	P73					○*7	×	×	×
		P81					○*7	×	×	×
	USB1_ID (input)	P77					○*7	×	×	×
CAN module	CRX0 (input)	P33	○	○	×	×	○	○	×	×
		PD2	○	○	×	×	○	○	×	×
	CTX0 (output)	P32	○	○	×	×	○	○	×	×
		PD1	○	○	×	×	○	○	×	×
	CRX1-DS (input)	P15	○	○	○	○	○	○	×	×
	CRX1 (input)	P55	○	○	○*2	×	○	○	×	×
	CTX1 (output)	P14	○	○	○	○	○	○	×	×
		P54	○	○	○*2	×	○	○	×	×
	CRX2 (input)*4	P67	○	×	×	×				
	CTX2 (output)*4	P66	○	×	×	×				
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	×	×	○	○	×	×
		PB0	○	○	○	○	×	×	×	×
		PC5	○	○	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	×	×	×	×
		PA6	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	×	×	×	×
		PA7	○	○	×	×	○	○	○	×
		PC7	○	○	○*2	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC4	○	○	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	×	○	○	×	×
		PC0	○	○	×	×	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Serial peripheral interface	SSLA2 (output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	○	×	×	○	○	○	×
	SSLA3 (output)	PA2	○	○	×	×	○	○	○	○
		PC2	○	○	○	×	○	○	×	×
	RSPCKB (input/output)	P27	○	○	○	○	○	○	○	○
		PE1	○	○	○	○	×	×	×	×
		PE5	○	○	○	×	○	○	×	×
	MOSIB (input/output)	P26	○	○	○	○	○	○	○	○
		PE2	○	○	○	○	×	×	×	×
		PE6	○	○	×	×	○	○	○	○
	MISOB (input/output)	P30	○	○	○	○	○	○	○	○
		PE3	○	○	○	○	×	×	×	×
		PE7	○	○	×	×	○	○	○	○
	SSLB0 (input/output)	P31	○	○	○	○	○	○	○	○
		PE4	○	○	○	○	○	○	×	×
	SSLB1 (output)	P50	○	○	×	×	○	○	×	×
		PE0	○	○	○	×	○	○	○	×
	SSLB2 (output)	P51	○	○	×	×	○	○	×	×
		PE1	○	○	○	○	○	○	○	×
	SSLB3 (output)	P52	○	○	×	×	○	○	×	×
		PE2	○	○	○	○	○	○	○	×
	RSPCKC (input/output)	PD3	○	×	×	×	○	○	×	×
		P56	×	×	×	×	○	×	×	×
	MOSIC (input/output)	PD1	○	×	×	×	○	○	×	×
		P54	×	×	×	×	○	○	×	×
	MISOC (input/output)	PD2	○	×	×	×	○	○	×	×
		P55	×	×	×	×	○	○	×	×
	SSLC0 (input/output)	PD4	○	×	×	×	○	○	×	×
	SSLC1 (output)	PD5	○	×	×	×	○	○	×	×
	SSLC2 (output)	PD6	○	×	×	×	○	○	×	×
	SSLC3 (output)	PD7	○	×	×	×	○	○	×	×
IEBus controller	IERXD (input)	P16	○	○	○	○				
		PC2	○	○	○	×				
	IETXD (output)	P17	○	○	○	○				
		PC3	○	○	○	×				
Realtime clock	RTCOUT (output)	P16	○	○	○	×	○	○	○	×
		P32	○	○	×	×	○	○	×	×
	RTCIC0 (input)*1	P30	○	○	○	×	○	○	○	×
	RTCIC1 (input)*1	P31	○	○	○	×	○	○	○	×
	RTCIC2 (input)*1	P32	○	○	×	×	○	○	×	×
Parallel data capture unit	PIXCLK (input)	P24	○	×	×	×				
	VSYNC (input)	P32	○	×	×	×				
	HSYNC (input)	P25	○	×	×	×				
	PIXD7 (input)	P23	○	×	×	×				
	PIXD6 (input)	P22	○	×	×	×				
	PIXD5 (input)	P21	○	×	×	×				
	PIXD4 (input)	P20	○	×	×	×				
	PIXD3 (input)	P17	○	×	×	×				

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Parallel data capture unit	PIXD2 (input)	P87	○	×	×	×				
	PIXD1 (input)	P86	○	×	×	×				
	PIXD0 (input)	P15	○	×	×	×				
	PCKO (output)	P33	○	×	×	×				
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	○	×	○	○	○	○
	AN004 (input)*1	P44	○	○	○	×	○	○	×	×
	AN005 (input)*1	P45	○	○	×	×	○	○	×	×
	AN006 (input)*1	P46	○	○	○	○	○	○	×	×
	AN007 (input)*1	P47	○	○	×	×	○	○	×	×
	AN008 (input)*1	PD0	○	○	×	×				
		PE0	×	×	○	×				
	AN009 (input)*1	PD1	○	○	×	×				
		PE1	×	×	○	○				
	AN010 (input)*1	PD2	○	○	×	×				
		PE2	×	×	○	○				
	AN011 (input)*1	PD3	○	○	×	×				
		PE3	×	×	○	○				
	AN012 (input)*1	PD4	○	○	×	×				
		PE4	×	×	○	○				
	AN013 (input)*1	PD5	○	○	×	×				
		PE5	×	×	○	×				
	AN014 (input)*1	P90	○	×	×	×				
	AN015 (input)*1	P91	○	×	×	×				
	AN016 (input)*1	P92	○	×	×	×				
	AN017 (input)*1	P93	○	×	×	×				
	AN018 (input)*1	P00	○	×	×	×				
	AN019 (input)*1	P01	○	×	×	×				
	AN020 (input)*1	P02	○	×	×	×				
	ADTRG0# (input)	P07	○	○	×	×	○	○	×	×
		P16	○	○	○	○	○	○	○	○
		P25	○	○	×	×	○	○	×	×
	AN100 (input)*1	PD7					○	○	○	×
	AN101 (input)*1	PD6					○	○	○	×
	AN102 (input)*1	PD5					○	○	○	○
	AN103 (input)*1	PD4					○	○	○	○
	AN104 (input)*1	PD3					○	○	○	○
	AN105 (input)*1	PD2					○	○	○	○
	AN106 (input)*1	PD1					○	○	×	×
	AN107 (input)*1	PD0					○	○	×	×
	AN108 (input)*1	P90					○	×	×	×
	AN109 (input)*1	P02					○	×	×	×
	AN110 (input)*1	P01					○	×	×	×
	AN111 (input)*1	P00					○	×	×	×
	ANEX0 (output)*1	PE0					○	○	○	×
	ANEX1 (input)*1	PE1					○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
12-bit A/D converter	ADTRG1# (input)	P13					○	○	○	○
		P17					○	○	○	○
10-bit A/D converter	AN0 (input)*1	PE2	○	○	×	×				
	AN1 (input)*1	PE3	○	○	×	×				
	AN2 (input)*1	PE4	○	○	×	×				
	AN3 (input)*1	PE5	○	○	×	×				
	AN4 (input)*1	PE6	○	○	×	×				
	AN5 (input)*1	PE7	○	○	×	×				
	AN6 (input)*1	PD6	○	○	×	×				
	AN7 (input)*1	PD7	○	○	×	×				
	ANEX0 (output)*1	PE0	○	○	×	×				
	ANEX1 (input)*1	PE1	○	○	×	×				
	ADTRG# (input)	P13	○	○	×	×				
		P17	○	○	×	×				
D/A converter	DA0 (output)*1	P03	○	×	×	×				
	DA1 (output)*1	P05	○	○	○	×				
Compare match timer W	TOC0 (output)	PC7					○	○	○	○
	TIC0 (input)	PC6					○	○	○	○
	TOC1 (output)	PE7					○	○	○	○
	TIC1 (input)	PE6					○	○	○	○
	TOC2 (output)	PD3					○	○	○	○
	TIC2 (input)	PD2					○	○	○	○
	TOC3 (output)	PE3					○	○	×	×
	TIC3 (input)	PE2					○	○	○	×
Battery backup	TAMPI0 (input)*1	P30					○	○	○	×
	TAMPI1 (input)*1	P31					○	○	○	×
	TAMPI2 (input)*1	P32					○	○	×	×
Serial communications interface	TAMPI0 (input)	P30					○	○	○	×
	TAMPI1 (input)	P31					○	○	○	×
	TAMPI2 (input)	P32					○	○	×	×
	RXD010 (input) / SMISO010 (input/output) / SSCL010 (input/output)	P81					○	×	×	×
		P86					○	×	×	×
		PC6					○	○	○	○
	TXD010 (output) / SMOSI010 (input/output) / SSDA010 (input/output)	P82					○	×	×	×
		P87					○	×	×	×
		PC7					○	○	○	○
	SCK010 (input/output)	P80					○	×	×	×
		P83					○	×	×	×
		PC5					○	○	○	○
	RTS010# (output)	P80					○	×	×	×
	CTS010# (input) / SS010# (input)	P83					○	×	×	×
	CTS010# (input) / RTS010# (output) / SS010# (input)	PC4					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Serial communications interface	DE010 (output)	P80					○	×	×	×
		PC4					○	○	○	○
	RXD011 (input) / SMISO011 (input/output) / SSCL011 (input/output)	P76					○	×	×	×
		PB6					○	○	○	○
		PC0					○	○	○	×
	TXD011 (output) / SMOSI011 (input/output) / SSDA011 (input/output)	P77					○	×	×	×
		PB7					○	○	○	○
		PC1					○	○	○	×
	SCK011 (input/output)	P75					○	×	×	×
		PB5					○	○	○	○
	TXDA011 (output)	PC1					○	○	○	×
	TXDB011 (output)	PC2					○	○	×	×
	RTS011# (output)	P75					○	×	×	×
	CTS011# (input) / SS011# (input)	P74					○	×	×	×
	CTS011# (input) / RTS011# (output) / SS011# (input)	PB4					○	○	×	×
	DE011 (output)	P75					○	×	×	×
		PB4					○	○	×	×
High-speed I^2C bus interface	SCLHS0[FM+ /HS] (input/output)	P12					○	○	○	○
	SDAHS0[FM+ /HS] (input/output)	P13					○	○	○	○
Serial peripheral interface	RSPCK0 (input/output)	PA5					○	○	×	×
		PC5					○	○	○	○
	MOSI0 (input/output)	PA6					○	○	○	○
		PC6					○	○	○	○
	MISO0 (input/output)	PA7					○	○	○	×
		PC7					○	○	○	○
	SSL00 (input/output)	PA4					○	○	○	○
		PC4					○	○	○	○
	SSL01 (output)	PA0					○	○	×	×
		PC0					○	○	○	×
	SSL02 (output)	PA1					○	○	○	○
		PC1					○	○	○	×
	SSL03 (output)	PA2					○	○	○	○
		PC2					○	○	×	×
Quad SPI memory interface	QSPCLK (input/output)	P77					○	×	×	×
		PD5					○	○	○	○
	QSSL (output)	P76					○	×	×	×
		PD4					○	○	○	○
	QIO0 (input/output)	PC3					○	○	×	×
		PD6					○	○	○	×
		PE6					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Quad SPI memory interface	QIO1 (input/output)	PC4					○	○	○	○
		PD7					○	○	○	×
		PE7					○	○	○	○
	QIO2 (input/output)	P80					○	×	×	×
		PD2					○	○	○	○
	QIO3 (input/output)	P81					○	×	×	×
		PD3					○	○	○	○
Serial sound interface	AUDIO_CLK (input)	P22					○	○	×	×
		PC4					○	○	○	○
	SSIBCK0 (input/output)	P23					○	○	×	×
		PC5					○	○	○	○
	SSILRCK0 (input/output)	P21					○	○	×	×
		PC6					○	○	○	○
	SSIRXD0 (input)	P20					○	○	×	×
		P53					○	○	○	○
	SSITXD0 (output)	P17					○	○	○	○
		PC7					○	○	○	○
SD host interface	SDHI_CLK (output)	P21					○	○	×	×
		P77					○	×	×	×
		PD5					○	○	○	○
	SDHI_CMD (input/output)	P20					○	○	×	×
		P76					○	×	×	×
		PD4					○	○	○	○
	SDHI_CD (input)	P25					○	○	×	×
		P81					○	×	×	×
		PA1					○	○	○	○
		PE6					○	○	○	○
	SDHI_WP (input)	P24					○	○	×	×
		P80					○	×	×	×
		PA2					○	○	○	○
		PE7					○	○	○	○
	SDHI_D0 (input/output)	P22					○	○	×	×
		PC3					○	○	×	×
		PD6					○	○	○	×
		PE6					○	○	○	○
	SDHI_D1 (input/output)	P23					○	○	×	×
		PC4					○	○	○	○
		PD7					○	○	○	×
		PE7					○	○	○	○
	SDHI_D2 (input/output)	P75					○	×	×	×
		P87					○	×	×	×
		PD2					○	○	○	○
	SDHI_D3 (input/output)	P17					○	○	○	○
		PC2					○	○	×	×
		PD3					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX63N				RX671			
			145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin	145-/ 144 -Pin	100 -Pin	64 -Pin	48 -Pin
Clock generation circuit	CLKOUT (output)	P25					○	○	×	×
	EXCIN (input)*1	PJ3					○	○	×	×
	EXTAL (input)*1	P36					○	○	○	○
	XTAL (output)*1	P37					○	○	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	PA0					○	○	×	×
		PC7					○	○	○	○
Capacitive touch sensing unit	TSCAP (—)	PC4					○	○	○	○
	TS0 (output)	P34					○	○	○	○
	TS1 (output)	P33					○	○	×	×
	TS2 (output)	P27					○	○	○	○
	TS3 (output)	P26					○	○	○	○
	TS4 (output)	P25					○	○	×	×
	TS5 (output)	P24					○	○	×	×
	TS6 (output)	P23					○	○	×	×
	TS7 (output)	P22					○	○	×	×
	TS8 (output)	P21					○	○	×	×
	TS9 (output)	P20					○	○	×	×
	TS10 (output)	P15					○	○	×	×
	TS11 (output)	P14					○	○	×	×
	TS12 (output)	P53					○	○	○	○
	TS13 (output)	PC6					○	○	○	○
	TS14 (output)	PC5					○	○	○	○
	TS15 (output)	PC1					○	○	○	×
	TS16 (output)	PC0					○	○	○	×
Remote control signal receiver	PMC0-DS (input)*1	P53					○	○	○	○
		PB3					○	○	×	×
		PC3					○	○	×	×

Notes: 1. For these pin functions, ensure that the corresponding pin is set as general input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).
2. Not implemented on RX631 Group 64-pin TFLGA products.
3. Not implemented on RX631 Group 64-pin LQFP products.
4. On the RX63N Group this pin is not implemented on products with a ROM capacity of 1 MB or less.
5. Not implemented on RX671 Group 145-pin TFLGA (0.65 mm pin pitch) products.
6. Not implemented on RX671 Group 64-pin TFBGA products.
7. On the RX671 Group this pin is implemented only on 145-pin TFLGA (0.65 mm pin pitch) products.

Table 2.38 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX63N (n = 0 to 3, 5, 7)	RX671 (n = 0 to 3, 5, 7)
P00PFS P01PFS P02PFS P07PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0)	Pin function select bits (b5 to b0)
P0nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P00: AN018 (177/176/145/144-pin) P01: AN019 (177/176/145/144-pin) P02: AN020 (177/176/145/144-pin) P03: DA0 (177/176/145/144-pin) P05: DA1 (177/176/145/144/100/64-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P00: AN111 (145/144-pin) P01: AN110 (145/144-pin) P02: AN109 (145/144-pin)

Table 2.39 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 2 to 7)
P10PFS	—	P10 pin function control register	—
P11PFS	—	P11 pin function control register	—
P12PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5U 00101b: TMCI1 01010b: RXD2/SMISO2/SSCL2 01111b: SCL0[FM+]	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 100101b: SCLHS0[FMF/HS]
P13PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: TIOCA5 00101b: TMO3 00110b: PO13 01001b: ADTRG# 01010b: TXD2/SMOSI2/SSDA2 01111b: SDA0[FM+]	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 101111b: SDAHS0[FMF/HS]

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 2 to 7)
P14PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: TIOCB5 00100b: TCLKA 00101b: TMRI2 00110b: PO15 01011b: CTS1#/RTS1#/SS1# 10000b: CTX1 10001b: USB0_DPUPE 10010b: USB0_OVRCURA	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 101011b: TS11
P15PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00011b: TIOCB2 00100b: TCLKB 00101b: TMCI2 00110b: PO13 01010b: RXD1/SMISO1/SSCL1 01011b: SCK3 10000b: CRX1-DS 10001b: USB1_DPUPE 11100b: PIXD0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 101011b: TS10
P16PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00011b: TIOCB1 00100b: TCLKC 00101b: TMO2 00110b: PO14 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01011b: RXD3/SMISO3/SSCL3 01101b: MOSIA 01111b: SCL2-DS 10000b: IERXD 10001b: USB0_VBUS 10010b: USB0_VBUSEN 10011b: USB0_OVRCURB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000011b: TIOCB1 000100b: TCLKC 000101b: TMO2 000110b: PO14 000111b: RTCOUT 001001b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001111b: SCL2-DS 010001b: USB0_VBUS 010010b: USB0_VBUSEN 010011b: USB0_OVRCURB

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 2 to 7)
P17PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00011b: TIOCB0 00100b: TCLKD 00101b: TMO1 00110b: PO15 00111b: POE8# 01001b: ADTRG# 01010b: SCK1 01011b: TXD3/SMOSI3/SSDA3 01101b: MISOA 01111b: SDA2-DS 10000b: IETXD 10001b: USB1_VBUS 11100b: PIXD3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS 010111b: SSITXD0 011010b: SDHI_D3-C
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (177/176-pin) P11: IRQ1 (177/176-pin) P12: IRQ2 (177/176/145/144/100-pin) P13: IRQ3 (177/176/145/144/100-pin) P14: IRQ4 (177/176/145/144/100/64/48-pin) P15: IRQ5 (177/176/145/144/100/64/48-pin) P16: IRQ6 (177/176/145/144/100/64/48-pin) P17: IRQ7 (177/176/145/144/100/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (145/144/100/64/48-pin) P13: IRQ3 (145/144/100/64/48-pin) P14: IRQ4 (145/144/100-pin) P15: IRQ5 (145/144/100-pin) P16: IRQ6 (145/144/100/64/48-pin) P17: IRQ7 (145/144/100/64/48-pin)

Table 2.40 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
P20PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00011b: TIOCB3 00101b: TMRI0 00110b: PO0 01010b: TXD0/SMOSI0/SSDA0 01111b: SDA1 10011b: USB0_ID 11100b: PIXD4	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRI0 000110b: PO0 001010b: TXD0/SMOSI0/SSDA0 001111b: SDA1 010011b: USB0_ID 010111b: SSIRXD0 011010b: SDHI_CMD-C 101011b: TS9
P21PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: TIOCA3 00101b: TMCI0 00110b: PO1 01010b: RXD0/SMISO0/SSCL0 01111b: SCL1 10011b: USB0_EXICEN 11100b: PIXD5	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCI0 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 001111b: SCL1 010011b: USB0_EXICEN 011010b: SDHI_CLK-C 101011b: TS8
P22PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKC 00011b: TIOCC3 00101b: TMO0 00110b: PO2 01010b: SCK0 10011b: USB0_DRPD 11000b: EDREQ0 11100b: PIXD6	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRCURB 010111b: AUDIO_CLK 011000b: EDREQ0 011010b: SDHI_D0-C 101011b: TS7

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
P23PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKD 00011b: TIOCD3 00110b: PO3 01010b: TXD3/SMOSI3/SSDA3 01011b: CTS0#/RTS0#/SS0# 10011b: USB0_DPUPE 11000b: EDACK0 11100b: PIXD7	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0# 010111b: SSIBCK0 011000b: EDACK0 011010b: SDHI_D1-C 101011b: TS6
P24PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00010b: MTCLKA 00011b: TIOCB4 00101b: TMRI1 00110b: PO4 01010b: SCK3 10011b: USB0_VBUSEN 11000b: EDREQ1 11100b: PIXCLK	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUSEN 011000b: EDREQ1 011010b: SDHI_WP 101011b: TS5
P25PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTCLKB 00011b: TIOCA4 00110b: PO5 01001b: ADTRG0# 01010b: RXD3/SMISO3/SSCL3 10011b: USB0_DPRPD 11000b: EDACK1 11100b: HSYNC	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 011000b: EDACK1 011010b: SDHI_CD 101010b: CLKOUT 101011b: TS4

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
P26PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 00110b: PO6 01010b: TXD1/SMOSI1/SSDA1 01011b: CTS3#/RTS3#/SS3# 01101b: MOSIB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3# 001101b: MOSIB-A 101011b: TS3
P27PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMCI3 00110b: PO7 01010b: SCK1 01101b: RSPCKB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A 101011b: TS2
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (177/176/145/144/100-pin) P21: IRQ9 (177/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (145/144/100-pin) P21: IRQ9 (145/144/100-pin) P22: IRQ15 (145/144/100-pin) P23: IRQ3 (145/144/100-pin) P24: IRQ12 (145/144/100-pin) P25: IRQ5 (145/144/100-pin) P26: IRQ6 (145/144/100/64/48-pin) P27: IRQ7 (145/144/100/64/48-pin)

Table 2.41 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX63N (n = 0 to 4)	RX671 (n = 0 to 4)
P30PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMRI3 00110b: PO8 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1 01101b: MISOB 10011b: USB0_DRPD	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000110b: PO8 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 001101b: MISOB-A

Register	Bit	RX63N (n = 0 to 4)	RX671 (n = 0 to 4)
P31PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI2 00110b: PO9 01011b: CTS1#/RTS1#/SS1# 01101b: SSLB0 10011b: USB0_DPUPE	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 000110b: PO9 001011b: CTS1#/RTS1#/SS1# 001101b: SSLB0-A
P32PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: TIOCC0 00101b: TMO3 00110b: PO10 00111b: RTCOUT 01010b: TXD6/SMOSI6/SSDA6 01011b: TXD0/SMOSI0/SSDA0 10000b: CTX0 10011b: USB0_VBUSEN 11100b: VSYNC	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: TIOCC0 000101b: TMO3 000110b: PO10 000111b: RTCOUT 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 010011b: USB0_VBUSEN 100001b: POE10#
P33PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: TIOCD0 00101b: TMRI3 00110b: PO11 00111b: POE3# 01010b: RXD6/SMISO6/SSCL6 01011b: RXD0/SMISO0/SSCL0 10000b: CRX0 11100b: PCKO	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 100001b: POE11# 101011b: TS1

Register	Bit	RX63N (n = 0 to 4)	RX671 (n = 0 to 4)
P34PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00101b: TMCI3 00110b: PO12 00111b: POE2# 01010b: SCK6 01011b: SCK0 10011b: USB0_DPRPD	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 101011b: TS0

Table 2.42 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX63N (n = 0 to 2, 4 to 7)	RX671 (n = 0 to 6)
P50PFS P51PFS P52PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0)	Pin function select bits (b5 to b0)
P53PFS	—	—	P53 pin function control register
P54PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 01011b: CTS2#/RTS2#/SS2# 10000b: CTX1 10001b: ET_LINKSTA 11000b: EDACK0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 011000b: EDACK0
P55PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMO3 10000b: CRX1 10001b: ET_EXOUT 11000b: EDREQ0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 001101b: MISOC-B 010000b: CRX1 011000b: EDREQ0
P56PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00011b: TIOCA1 11000b: EDACK1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1
P57PFS	—	—	P57 pin function control register

Table 2.43 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX63N (n = 0, 1, 6, 7)	RX671 (n = 0 to 7)
P62PFS	—	—	P62 pin function control register
P6PFS	—	—	P63 pin function control register
P6PFS	—	—	P64 pin function control register
P6PFS	—	—	P65 pin function control register
P66PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 10000b: CTX2*1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: MTIOC7D
P67PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 10000b: CRX2*1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: MTIOC7C
P6nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P67: IRQ15 (177/176/145/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ0 (145/144-pin) P61: IRQ1 (145/144-pin) P62: IRQ2 (145/144-pin) P63: IRQ3 (145/144-pin) P64: IRQ4 (145/144-pin) P65: IRQ13 (145/144-pin) P66: IRQ14 (145/144-pin) P67: IRQ15 (145/144-pin)

Note: 1. Not implemented on products with a ROM capacity of 1 MB or less.

Table 2.44 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
P71PFS	PSEL[4:0]	Pin function select bits (b4 to b0)	—
P72PFS	PSEL[4:0]	Pin function select bits (b4 to b0)	—
P73PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00110b: PO16 10001b: ET_WOL	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000110b: PO16 010001b: USB1_VBUS 010010b: USB1_VBUSEN 010011b: USB1_OVRCURB

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
P74PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00110b: PO19 01011b: CTS11#/RTS11/SS11# 10001b: ET_ERXD1 10010b: RMII_RXD1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000110b: PO19 001011b: CTS11#/SS11# 010011b: USB1_VBUSEN 101101b: CTS011#/SS011#
P75PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00110b: PO20 01010b: SCK11 10001b: ET_ERXD0 10010b: RMII_RXD0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010010b: USB1_OVRCURA 011010b: SDHI_D2-A 101100b: SCK011 101101b: RTS011# 101110b: DE011
P76PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00110b: PO22 01010b: RXD11/SMISO11/SSCL11 10001b: ET_RX_CLK 10010b: REF50CK	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000110b: PO22 001010b: RXD11/SMISO11/SSCL11 011010b: SDHI_CMD-A 011011b: QSSL-A 101100b: RXD011/SMISO011/ SSCL011
P77PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00110b: PO23 01010b: TXD11/SMOSI11/SSDA11 10001b: ET_RX_ER 10010b: RMII_RX_ER	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000110b: PO23 001010b: TXD11/SMOSI11/SSDA11 010011b: USB1_ID 011010b: SDHI_CLK-A 011011b: QSPCLK-A 101100b: TXD011/SMOSI011/ SSDA011
P7nPFS	ISEL	—	Interrupt input function select bit

Table 2.45 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX63N (n = 0 to 3, 6, 7)	RX671 (n = 0 to 3, 6, 7)
P80PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00110b: PO26 01010b: SCK10 10001b: ET_TX_EN 10010b: RMII_TXD_EN 11000b: EDREQ0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010011b: USB1_EXICEN 011000b: EDREQ0 011010b: SDHI_WP 011011b: QIO2-A 101100b: SCK010 101101b: RTS010# 101110b: DE010
P81PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00110b: PO27 01010b: RXD10/SMISO10/SSCL10 10001b: ET_ETXD0 10010b: RMII_TXD0 11000b: EDACK0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: RXD10/SMISO10/SSCL10 010011b: USB1_OVRCURB 011000b: EDACK0 011010b: SDHI_CD 011011b: QIO3-A 101100b: RXD010/SMISO010/ SSCL010
P82PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00110b: PO28 01010b: TXD10/SMOSI10/SSDA10 10001b: ET_ETXD1 10010b: RMII_TXD1 11000b: EDREQ1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: TXD10/SMOSI10/SSDA10 010011b: USB1_VBUSEN 011000b: EDREQ1 101100b: TXD010/SMOSI010/ SSDA010

Register	Bit	RX63N (n = 0 to 3, 6, 7)	RX671 (n = 0 to 3, 6, 7)
P83PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4C 01011b: CTS10#/RTS10#/SS10# 10001b: ET_CRS 10010b: RMII_CRS_DV 11000b: EDACK1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 011000b: EDACK1 101100b: SCK010 101101b: CTS010#/SS010#
P86PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCA0 11100b: PIXD1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
P87PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCA2 11100b: PIXD2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: TXD10/SMOSI10/SSDA10 011010b: SDHI_D2-C 101100b: TXD010/SMOSI010/ SSDA010
P8nPFS	ISEL	—	Interrupt input function select bit

Table 2.46 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX63N (n = 0 to 3)	RX671 (n = 0 to 3)
P90PFS P91PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0)	Pin function select bits (b5 to b0)
P92PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01010b: RXD7/SMISO7/SSCL7	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: POE4# 001010b: RXD7/SMISO7/SSCL7
P93PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 01011b: CTS7#/RTS7#/SS7#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: POE0# 001011b: CTS7#/RTS7#/SS7#
P9nPFS	ISEL	—	Interrupt input function select bit

Table 2.47 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PA0PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: TIOCA0 00110b: PO16 01101b: SSLA1 10001b: ET_TX_EN 10010b: RMII_TXD_EN	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 001110b: SSL01-B
PA1PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: TIOCB0 00110b: PO17 01010b: SCK5 01101b: SSLA2 10001b: ET_WOL	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5 001100b: SCK12 001101b: SSLA2-B 001110b: SSL02-B 110001b: SDHI_CD

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PA2PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00110b: PO18 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA3-B 001110b: SSL03-B 110001b: SDHI_WP
PA3PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: TIOCD0 00100b: TCLKB 00110b: PO19 01010b: RXD5/SMISO5/SSCL5 10001b: ET_MDIO	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5
PA4PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: TIOCA1 00101b: TMRI0 00110b: PO20 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 10001b: ET_MDC	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: SSLA0-B 001110b: SSL00-B
PA5PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCB1 00110b: PO21 01101b: RSPCKA 10001b: ET_LINKSTA	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 001110b: RSPCK0-B

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PA6PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: TIOCA2 00101b: TMCI3 00110b: PO22 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 10001b: ET_EXOUT	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA-B 001110b: MOSI0-B
PA7PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCB2 00110b: PO23 01101b: MISOA 10001b: ET_WOL	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000011b: TIOCB2 000110b: PO23 001101b: MISOA-B 001110b: MISO0-B
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: RQ11 (177/176/145/144/100/64/48-pin) PA3: IRQ6-DS (177/176/145/144/100/64/48-pin) PA4: IRQ5-DS (177/176/145/144/100/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (145/144/100-pin) PA1: IRQ11 (145/144/100/64/48-pin) PA2: IRQ10 (145/144/100/64/48-pin) PA3: IRQ6-DS (145/144/100-pin) PA4: IRQ5-DS (145/144/100/64/48-pin) PA5: IRQ5 (145/144/100-pin) PA6: IRQ14 (145/144/100/64/48-pin) PA7: IRQ7 (145/144/100/64-pin)

Table 2.48 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PB0PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: TIOCA3 00110b: PO24 01010b: RXD4/SMISO4/SSCL4 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 10001b: ET_ERXD1 10010b: RMII_RXD1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6
PB1PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00011b: TIOCB3 00101b: TMCI0 00110b: PO25 01010b: TXD4/SMOSI4/SSDA4 01011b: TXD6/SMOSI6/SSDA6 10001b: ET_ERXD0 10010b: RMII_RXD0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6
PB2PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCC3 00100b: TCLKC 00110b: PO26 01010b: CTS4#/RTS4#/SS4# 01011b: CTS6#/RTS6#/SS6# 10001b: ET_RX_CLK 10010b: REF50CK	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00011b: TIOCD3 00100b: TCLKD 00101b: TMO0 00110b: PO27 00111b: POE3# 01010b: SCK4 01011b: SCK6 10001b: ET_RX_ER 10010b: RMII_RX_ER	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PB4PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCA4 00110b: PO28 01011b: CTS9#/RTS9#/SS9# 10001b: ET_TX_EN 10010b: RMII_TXD_EN	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#*1/RTS011#*1/ SS011# 101110b: DE011
PB5PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00011b: TIOCB4 00101b: TMRI1 00110b: PO29 00111b: POE1# 01010b: SCK9 10001b: ET_ETXD0 10010b: RMII_TXD0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 100100b: SCK11 101100b: SCK011
PB6PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: TIOCA5 00110b: PO30 01010b: RXD9/SMISO9/SSCL9 10001b: ET_ETXD1 10010b: RMII_TXD1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/SSCL11 101100b: RXD011/SMISO011/ SSCL011

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PB7PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: TIOCB5 00110b: PO31 01010b: TXD9/SMOSI9/SSDA9 10001b: ET_CRS 10010b: RMII_CRS_DV	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/SSDA11 101100b: TXD011/SMOSI011/ SSDA011
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (177/176/145/144/100/64/48 -pin) PB1: IRQ4-DS (177/176/145/144/100/64/48 -pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (145/144/100-pin) PB1: IRQ4-DS (145/144/100-pin) PB2: IRQ2 (145/144/100-pin) PB3: IRQ3 (145/144/100-pin) PB4: IRQ4 (145/144/100-pin) PB5: IRQ13 (145/144/100/64/48-pin) PB6: IRQ6 (145/144/100/64/48-pin) PB7: IRQ15 (145/144/100/64/48-pin)

Note: 1. Not usable as CTS011# when SCR1.CRSEP = 1. Can be used as RTS011#.

Table 2.49 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PC0PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00011b: TCLKC 00110b: PO17 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1 01111b: SCL3 10001b: ET_ERXD3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1-A 001110b: SSL01-A 101011b: TS16 101100b: RXD011/SMISO011/ SSCL011

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PC1PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00011b: TCLKD 00110b: PO18 01010b: SCK5 01101b: SSLA2 01111b: SDA3 10001b: ET_ERXD2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 001110b: SSL02-A 101011b: TS15 101100b: TXD011/SMOSI011/ SSDA011/TXDA011
PC2PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: TCLKA 00110b: PO21 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 10000b: IERXD 10001b: ET_RX_DV	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 001110b: SSL03-A 011010b: SDHI_D3-A 101100b: TXDB011
PC3PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: TCLKB 00110b: PO24 01010b: TXD5/SMOSI5/SSDA5 10000b: IETXD 10001b: ET_TX_ER	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 011010b: SDHI_D0-A 011011b: QIO0-A

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PC4PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00011b: TIOCC6 00100b: TCLKE 00101b: TMCI1 00110b: PO25 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 10001b: ET_TX_CLK	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0-A 001110b: SSL00-A 010111b: AUDIO_CLK 011010b: SDHI_D1-A 011011b: QIO1-A 100100b: CTS10#/RTS10#/SS10# 101011b: TSCAP 101100b: CTS010#*1/RTS010#*1/ SS010# 101110b: DE010
PC5PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00011b: TIOCD6 00100b: TCLKF 00101b: TMRI2 00110b: PO29 01010b: SCK8 01101b: RSPCKA 10001b: ET_ETXD2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001101b: RSPCKA-A 001110b: RSPCK0-A 010111b: SSIBCK0 100100b: SCK10 101011b: TS14 101100b: SCK010

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PC6PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00011b: TIOCA6 00101b: TMCI2 00110b: PO30 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 10001b: ET_ETXD3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A 001110b: MOSI0-A 010111b: SSILRCK0 011101b: TIC0 100100b: RXD10/SMISO10/SSCL10 101011b: TS13 101100b: RXD010/SMISO010/ SSCL010
PC7PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00011b: TIOCB6 00101b: TMO2 00110b: PO31 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA 10001b: ET_COL	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000110b: PO31 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA-A 001110b: MISO0-A 010111b: SSITXD0 011101b: TOC0 100100b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PCnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (177/176/145/144/100-pin) PC1: IRQ12 (177/176/145/144/100-pin) PC6: IRQ13 (177/176/145/144/100/64/48-pin) PC7: IRQ14 (177/176/145/144/100/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (145/144/100/64-pin) PC1: IRQ12 (145/144/100/64-pin) PC2: IRQ10 (145/144/100-pin) PC3: IRQ11 (145/144/100-pin) PC4: IRQ12 (145/144/100/64/48-pin) PC5: IRQ5 (145/144/100/64/48-pin) PC6: IRQ13 (145/144/100/64/48-pin) PC7: IRQ14 (145/144/100/64/48-pin)

Note: 1. Not usable as CTS011# when SCR1.CRSEP = 1. Can be used as RTS011#.

Table 2.50 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PD0PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCA7	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: POE4#
PD1PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: TIOCB7 00100b: TCLKG 01101b: MOSIC 10000b: CTX0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0
PD2PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: TIOCA8 01101b: MISOC 10000b: CRX0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PD3PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCB8 00100b: TCLKH 00111b: POE8# 01101b: RSPCKC	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2
PD4PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00111b: POE3# 01101b: SSLC0	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B 001101b: SSLC0-A 011010b: SDHI_CMD-B 011011b: QSSL-B
PD5PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5W 00111b: POE2# 01101b: SSLC1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 011010b: SDHI_CLK-B 011011b: QSPCLK-B
PD6PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5V 00111b: POE1# 01101b: SSLC2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011010b: SDHI_D0-B 011011b: QIO0-B
PD7PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5U 00111b: POE0# 01101b: SSLC3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011010b: SDHI_D1-B 011011b: QIO1-B

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PDnPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN008 (177/176/145/144/100-pin) PD1: AN009 (177/176/145/144/100-pin) PD2: AN010 (177/176/145/144/100-pin) PD3: AN011 (177/176/145/144/100-pin) PD4: AN012 (177/176/145/144/100-pin) PD5: AN013 (177/176/145/144/100-pin) PD6: AN6 (177/176/145/144/100-pin) PD7: AN7 (177/176/145/144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN107 (145/144/100-pin) PD1: AN106 (145/144/100-pin) PD2: AN105 (145/144/100/64/48-pin) PD3: AN104 (145/144/100/64/48-pin) PD4: AN103 (145/144/100/64/48-pin) PD5: AN102 (145/144/100/64/48-pin) PD6: AN101 (145/144/100/64-pin) PD7: AN100 (145/144/100/64-pin)

Table 2.51 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PE0PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCC9 01100b: SCK12 01101b: SSLB1	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B
PE1PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: TIOCD9 00110b: PO18 01100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 01101b: SSLB2 01110b: RSPCKB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12 001101b: SSLB2-B

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PE2PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: TIOCA9 00110b: PO23 01100b: RXD12/SMISO12/ SSSL12/RXDX12 01101b: SSLB3 01110b: MOSIB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLB3-B 011101b: TIC3
PE3PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: TIOCB9 00110b: PO26 00111b: POE8# 01100b: CTS12#/RTS12#/SS12# 01101b: MISOB 10001b: ET_ERXD3	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3
PE4PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 00011b: TIOCA10 00110b: PO28 01101b: SSLB0 10001b: ET_ERXD2	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B
PE5PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTIOC2B 00011b: TIOCB10 01101b: RSPCKB 10001b: ET_RX_CLK 10010b: REF50CK	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PE6PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCA11 01101b: MOSIB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011010b: SDHI_CD 011011b: QIO0-B 011101b: TIC1 110001b: SDHI_D0-B
PE7PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00011b: TIOCB11 01101b: MISOB	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011010b: SDHI_WP 011011b: QIO1-B 011101b: TOC1 110001b: SDHI_D1-B
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (177/176/145/144/100/64/48-pin) PE5: IRQ5 (177/176/145/144/100/64-pin) PE6: IRQ6 (177/176/145/144/100-pin) PE7: IRQ7 (177/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (145/144/100/64-pin) PE1: IRQ9 (145/144/100/64-pin) PE2: IRQ7-DS (145/144/100/64-pin) PE3: IRQ11 (145/144/100-pin) PE4: IRQ12 (145/144/100-pin) PE5: IRQ5 (145/144/100-pin) PE6: IRQ6 (145/144/100/64/48-pin) PE7: IRQ7 (145/144/100/64/48-pin)

Register	Bit	RX63N (n = 0 to 7)	RX671 (n = 0 to 7)
PEnPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (64/48-pin), ANEX0 (177/176/145/144/100-pin) PE1: AN009 (64/48-pin), ANEX0 (177/176/145/144/100-pin) PE2: AN010 (64/48-pin), AN0 (177/176/145/144/100-pin) PE3: AN011 (64/48-pin), AN1 (177/176/145/144/100-pin) PE4: AN012 (64/48-pin), AN2 (177/176/145/144/100-pin) PE5: AN013 (64/48-pin), AN3 (177/176/145/144/100-pin) PE6: AN4 (177/176/145/144/100-pin) PE7: AN5 (177/176/145/144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: ANEX0 (145/144/100/64-pin) PE1: ANEX1 (145/144/100/64-pin)

Table 2.52 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX63N (n = 0 to 2, 5)	RX671 (n = 5)
PF0PFS	—	PF0 pin function control register	—
PF1PFS	—	PF1 pin function control register	—
PF2PFS	—	PF2 pin function control register	—
PF5PFS	PSEL[4:0] (RX63N)	Pin function select bits (b4 to b0)	—

Table 2.53 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX63N	RX671
PHnPFS	—	—	PHn pin function control register (n = 1, 2)

Table 2.54 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX63N (n = 3)	RX671 (n = 3, 5)
PJ3PFS	PSEL[4:0] (RX63N) PSEL[5:0] (RX671)	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 01010b: CTS6#/RTS6#/SS6# 01011b: CTS0#/RTS0#/SS0#	Pin function select bits (b5 to b0) b5 b0 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 011000b: EDACK1
PJ5PFS	—	—	PJ5 pin function control register
PJnPFS	ISEL	—	Interrupt input function select bit

Table 2.55 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX63N	RX671
PFBCR0	ADRHMS2	—	A16 to A23 output enable 2 bit
	BCLKO	—	BCLK forced output bit
	DH32E	—	D16 to D31 output enable
	WR32BC32E	—	WR3#/BC3# and WR2#/BC2# output enable bit
PFBCR1	WAITS[1:0]	WAIT select bits b1 b0 0 0: Configures P57 as the WAIT# input pin. 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.	WAIT select bits b1 b0 0 0: Invalid setting 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.
PFBCR2	—	—	External bus control register 2
PFBCR3	—	—	External bus control register 3
PFENET	—	Ethernet control register	—
PFUSB0	—	USB0 control register	—
PFUSB1	—	USB1 control register	—

2.19 Multi-Function Timer Pulse Units 2 and 3

Table 2.56 is a comparative overview of multi-function timer pulse units 2 and 3, and Table 2.57 is a comparison of multi-function timer pulse unit 2 and 3 registers.

Table 2.56 Comparative Overview of Multi-Function Timer Pulse Units 2 and 3

Item	RX63N (MTU2a)	RX671 (MTU3a)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	Seven and eight clocks for each channel (four clocks for MTU5)	11 clocks for each channel (14 for MTU0, 12 for MTU2, 10 for MTU5, and four each for MTU1 and MTU2 (when LWA = 1))
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU8] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous clearing by compare match or input capture (excluding MTU8) • Simultaneous register input/output by synchronous counter operation (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[MTU0, MTU3, MTU4] Ability to specify buffer operation	[MMTU0, MTU3, MTU4, MTU6, MTU7, MTU8] Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation
	[MTU3, MTU4] Ability to produce six-phase waveform output, including three phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode

Item	RX63N (MTU2a)	RX671 (MTU3a)
Available operations	[MTU3, MTU4] Ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	[MTU3, MTU4] Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
	[MTU5] Dead time compensation counter	[MTU5] Can be used as a dead time compensation counter.
	—	[MTU0/MTU5, MTU1, MTU2, MTU8] Ability to use the MTU1 and MTU2 in combination and specify 32-bit phase counting mode linked to the MTU0 or MTU5 and MTU8
Interrupt skipping function	• Interrupts at counter peak or trough • A/D converter conversion start trigger skipping function	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	43 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate programmable pulse generator (PPG) output triggers • Ability to generate A/D converter start trigger	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delay function, and ability to synchronize operation with PWM output
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.57 Comparison of Multi-Function Timer Pulse Unit 2 and 3 Registers

Register	Bit	RX63N (MTU2a)	RX671 (MTU3a)
TCR2	—	—	Timer control register 2
TMDR (RX63N) TMDR1 (RX671)	MD[3:0]	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Setting prohibited 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough)	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Phase counting mode 5 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough)
TMDR2A TMDR2B	—	—	Timer mode register 2
TMDR3	—	—	Timer mode register 3

Register	Bit	RX63N (MTU2a)	RX671 (MTU3a)
MTU1.TIOR	IOB[3:0]	I/O control B bits b7 b4 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Input capture at occurrence of MTU0.TGRC compare match or input capture.	I/O control B bits b7 b4 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 0 0: Input capture at occurrence of MTU0.TGRC compare match or input capture. 1 1 1 x: Input capture at occurrence of MTU8.TGRC compare match.

Register	Bit	RX63N (MTU2a)	RX671 (MTU3a)
MTU0.TIORH	IOA[3:0]	I/O control A bits b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Capture input source is count clock on MTU1. Input capture at MTU1.TCNT up-count or down-count.	I/O control A bits b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 0 0: Capture input source is count clock on MTU1. Input capture at MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1) up-count or down-count. 1 1 1 x: Input capture at occurrence of MTU8.TGRC compare match.
TIORU TIORV TIORW	IOC[4:0]	I/O control C bits b4 b0 0 0 0 0 0: Compare match 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge. 1 0 0 1 0: Input capture at falling edge. 1 0 0 1 1: Input capture at both edges. 1 0 1 x x: Setting prohibited	I/O control C bits b4 b0 0 0 0 0 0: No function 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge. 1 0 0 1 0: Input capture at falling edge. 1 0 0 1 1: Input capture at both edges. 1 0 1 x x: Capture at occurrence of MTU8.TGRC compare match.

Register	Bit	RX63N (MTU2a)	RX671 (MTU3a)
TIORU TIORV TIORW	IOC[4:0]	1 1 0 0 0: Setting prohibited 1 1 0 0 1: Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 0 1 0: Measurement of low pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 0 1 1: Measurement of low pulse width of external input signal. Capture at crest and trough in complementary PWM mode. 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 1 1 0: Measurement of high pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 1 1 1: Measurement of high pulse width of external input signal. Capture at crest and trough in complementary PWM mode.	1 1 0 0 0: Setting prohibited 1 1 0 0 1: Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 0 1 0: Measurement of low pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 0 1 1: Measurement of low pulse width of external input signal. Capture at crest and trough in complementary PWM mode. 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 1 1 0: Measurement of high pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 1 1 1: Measurement of high pulse width of external input signal. Capture at crest and trough in complementary PWM mode.
MTU0.TIER2	TTGE2	—	A/D conversion start request enable 2 bit
TSR	—	Timer status register Initial values after a reset are different.	Timer status register
MTU.TSTR (RX63N) TSTRA (RX671)	CST8	—	Counter start 8 bit
TSTRB	—	—	Timer start register
TSYR (RX63N) TSYRA (RX671)	—	Timer synchronous register	Timer synchronous register
TSYRB	—	—	Timer synchronous register
TRWER (RX63N) TRWERA (RX671)	—	Timer read/write enable register	Timer read/write enable register
TRWERB	—	—	Timer read/write enable register

Register	Bit	RX63N (MTU2a)	RX671 (MTU3a)
TOER (RX63N) TOERA (RX671)	—	Timer output master enable register	Timer output master enable register
TOERB	—	—	Timer output master enable register
TOCR1 (RX63N) TOCR1A (RX671)	—	Timer output control register 1	Timer output control register 1
TOCR1B	—	—	Timer output control register 1
TOCR2 (RX63N) TOCR2A (RX671)	—	Timer output control register 2	Timer output control register 2
TOCR2B	—	—	Timer output control register 2
TOLBR (RX63N) TOLBRA (RX671)	—	Timer output level buffer register	Timer output level buffer register
TOLBRB	—	—	Timer output level buffer register
TGCR (RX63N) TGCRA (RX671)	—	Timer gate control register	Timer gate control register A
TCNTS (RX63N) TCNTSA (RX671)	—	Timer subcounter	Timer subcounter
TCNTSB	—	—	Timer subcounter
TDDR (RX63N) TDDRA (RX671)	—	Timer dead time data register	Timer dead time data register
TDDRB	—	—	Timer dead time data register
TCDR (RX63N) TCDRA (RX671)	—	Timer cycle data register	Timer cycle data register
TCDRB	—	—	Timer cycle data register
TCBR (RX63N) TCBRA (RX671)	—	Timer cycle buffer register	Timer cycle buffer register
TCBRB	—	—	Timer cycle buffer register
TITCR (RX63N) TITCR1A (RX671)	—	Timer interrupt skipping set register	Timer interrupt skipping set register 1
TITCR1B	—	—	Timer interrupt skipping set register 1
TITCNT (RX63N) TITCNT1A (RX671)	—	Timer interrupt skipping counter	Timer interrupt skipping counter 1
TITCR1B	—	—	Timer interrupt skipping counter 1
TBTER (RX63N) TBTERA (RX671)	—	Timer buffer transfer set register	Timer buffer transfer set register
TBTERB	—	—	Timer buffer transfer set register
TDER (RX63N) TDERA (RX671)	—	Timer dead time enable register	Timer dead time enable register
TDERB	—	—	Timer dead time enable register
TWCR (RX63N) TWCRA (RX671)	SCC	—	Synchronous clear control bit
TWCRB	—	—	Timer waveform control register
TCNTLW	—	—	Timer longword counter
TGRALW TGRBLW	—	—	Timer longword general register
MTU.TSTR (RX63N) MTU.TSTRA (RX671)	—	Timer start register	Timer start register
TBTER (RX63N) TBTERA (RX671)	—	Timer buffer transfer set register	Timer buffer transfer set register

Register	Bit	RX63N (MTU2a)	RX671 (MTU3a)
TCSYSTR	—	—	Timer counter synchronous start register
NFCR (RX63N) NFCRn (RX671)	—	Noise filter control register	Noise filter control register n (n = 0 to 4, 6, 7, 8, and C)
TSYCR	—	—	Timer synchronous clear register
TCNTLW	—	—	Timer longword counter
TGRALW TGRBLW	—	—	Timer longword general register
TCSYSTR	—	—	Timer counter synchronous start register
TGCRA	—	—	Timer gate control register A
TCNTSA TCNTSB	—	—	Timer subcounter
NFCR5	—	—	Noise filter control register 5
TITMRA TITMRB	—	—	Timer interrupt skipping mode register
TITCR2A TITCR2B	—	—	Timer interrupt skipping set register 2
TITCNT2A TITCNT2	—	—	Timer interrupt skipping counter 2

2.20 Port Output Enable 2 and 3

Table 2.58 is a comparative overview of port output enable 2 and 3, and Table 2.59 is a comparison of port output enable 2 and 3 registers.

Table 2.58 Comparative Overview of Port Output Enable 2 and 3

Item	RX63N (POE2a)	RX671 (POE3a)
Pin status while output is disabled	High-impedance	High-impedance
High-impedance control target pins	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)
Conditions for generating high-impedance request	• Input pin changes When signal input occurs on pin POE0# to POE3#, or POE8#. • Short circuit of output pins: A match (short circuit) of signal levels lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11# • Short circuit of output pins: A match (short circuit) of signal levels lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator

Item	RX63N (POE2a)	RX671 (POE3a)
Functions	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0# to POE3# and POE8# input pins. • Pins for complementary PWM output from the MTU can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE0# to POE3# pins. • Pins for output from MTU0 can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE8# pin. • Pins for complementary PWM output from the MTU and pins for output from MTU0 can be placed in the high-impedance state when oscillation by the clock generation circuit stops. • It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, the pins can be placed in the high-impedance state. • Pins for complementary PWM output from the MTU and pins for output from MTU0 can be placed in the high-impedance state by modifying settings of POE registers. • Interrupts can be generated in response to the results of POE0# to POE3# and POE8# input-level detection or MTU complementary PWM output-level comparison.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins. • Output on all control target pins can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE0#, POE4#, POE8#, POE10#, and POE11# pins. • Output on all control target pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops. • It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be placed in the high-impedance state. • Output on all control target pins can be placed in the high-impedance state by modifying settings of POE registers. • Interrupts can be generated in response to the results of input level sampling or output-level comparison.

Table 2.59 Comparison of Port Output Enable 2 and 3 Registers

Register	Bit	RX63N (POE2a)	RX671 (POE3a)
ICSR1	POE1M[1:0]	POE1 mode select bits	—
	POE2M[1:0]	POE2 mode select bits	—
	POE3M[1:0]	POE3 mode select bits	—
	POE1F	POE1 flag	—
	POE2F	POE2 flag	—
	POE3F	POE3 flag	—
ICSR2 (RX63N) ICSR3 (RX671)	PIE2 (RX63N) PIE3 (RX671)	Port interrupt enable 2 bit	Port interrupt enable 3 bit
ICSR3 (RX63N) ICSR6 (RX671)	—	Input level control/status register 3	Input level control/status register 6
ICSR2 (RX671)	—	—	Input level control/status register 2
ICSR4	—	—	Input level control/status register 4
ICSR5	—	—	Input level control/status register 5
SPOER	CH34HIZ (RX63N) MTUCH34HIZ (RX671)	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 pin high-impedance enable bit
	MTUCH67HIZ	—	MTU6 and MTU7 pin high-impedance enable bit
	CH0HIZ (RX63N) MTUCH0HIZ (RX671)	MTU0 output high-impedance enable bit (b1)	MTU0 pin high-impedance enable bit (b2)
POECR1	PE0ZE (RX63N) MTU0AZE (RX671)	MTIOC0A high-impedance enable bit	MTIOC0A pin high-impedance enable bit
	PE1ZE (RX63N) MTU0BZE (RX671)	MTIOC0B high-impedance enable bit	MTIOC0B pin high-impedance enable bit
	PE2ZE (RX63N) MTU0CZE (RX671)	MTIOC0C high-impedance enable bit	MTIOC0C pin high-impedance enable bit
	PE3ZE (RX63N) MTU0DZE (RX671)	MTIOC0D high-impedance enable bit	MTIOC0D pin high-impedance enable bit

Register	Bit	RX63N (POE2a)	RX671 (POE3a)
POECR2	—	Port output enable control register 2 POECR2 is an 8-bit register.	Port output enable control register 2 POECR2 is a 16-bit register.
	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit
	P3CZEA (RX63N) MTU4BDZE (RX671)	MTU port 3 high-impedance enable bit (b4)	MTIOC4B/MTIOC4D pin high-impedance enable bit (b8)
	P2CZEA (RX63N) MTU4ACZE (RX671)	MTU port 2 high-impedance enable bit (b5)	MTIOC4A/MTIOC4C pin high-impedance enable bit (b9)
	P1CZEA (RX63N) MTU3BDZE (RX671)	MTU port 1 high-impedance enable bit (b6)	MTIOC3B/MTIOC3D pin high-impedance enable bit (b10)
OCSR2	—	—	Output level control/status register 2
ALR1	—	—	Active level register 1
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2

2.21 16-Bit Timer Pulse Unit

Table 2.60 is a comparative overview of 16-bit timer pulse units.

Table 2.60 Comparative Overview of 16-Bit Timer Pulse Units

Item	RX63N (TPUa)	RX671 (TPUa)
Pulse input/output	Max. 32 (unit 0: 16, unit 1: 16)	Max. 16
Count clocks	Seven or eight types are provided for each channel.	Seven or eight types are provided for each channel.
Available operations	• Waveform output at compare match • Input capture function (noise filters can be set) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascaded operation	• Waveform output at compare match • Input capture function (noise filters can be set) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascaded operation
Buffer operation	• Channels 0, 3, 6, and 9 • Automatic transfer of register data	• TPU0 and TPU3 • Automatic transfer of register data
Phase coefficient mode	Channels 1, 2, 4, 5, 7, 8, 10, and 11	TPU1, TPU2, TPU4, and TPU5
Interrupt sources	52 sources (unit 0: 26, unit 1: 26)	26 sources
Trigger generation	• Programmable pulse generator (PPG) output trigger can be generated. • Conversion start trigger for the A/D converter can be generated.	• Programmable pulse generator (PPG) output trigger can be generated. • Conversion start trigger for the A/D converter can be generated.
Event link function (output)	—	Six types of event signal can be output to the ELC. • Compare match A (TPU0 to TPU3) • Compare match B (TPU0 to TPU3) • Compare match C (TPU0, TPU3) • Compare match D (TPU0, TPU3) • Overflow (TPU0 to TPU3) • Underflow (TPU1, TPU)
Event link function (input)	—	Any of the three operations in response to event input is possible. • Starting counts (TPU0 to TPU3) • Restarting counts (TPU0 to TPU3) • Input capture operation (TPU0 to TPU3)
Low power consumption function	Module stop state can be set for each unit.	Ability to transition to module stop state

2.22 Programmable Pulse Generator

Table 2.61 is a comparison of programmable pulse generator registers.

Table 2.61 Comparison of the Programmable Pulse Generator Registers

Register	Bit	RX63N (PPG)	RX671 (PPG)
NDRH2	—	—	Next data register H2
NDRL2	—	—	Next data register L2

2.23 8-Bit Timer

Table 2.62 is a comparative overview of 8-bit timers, and Table 2.63 is a comparison of 8-bit timer registers.

Table 2.62 Comparative Overview of 8-Bit Timers

Item	RX63N (TMR)	RX671 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Each unit can be placed in a module stop state	Ability to transition each unit to the module stop state

Table 2.63 Comparison of 8-Bit Timer Registers

Register	Bit	RX63N (TMR)	RX671 (TMRb)
TCSTR	—	—	Time counter start register

2.24 Compare Match Timer

Table 2.64 is a comparative overview of the compare match timers.

Table 2.64 Comparative Overview of Compare Match Timers

Item	RX63N (CMT)	RX671 (CMT)
Count clocks	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	Event signal output at CMT1 compare match
Event link function (input)	—	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.25 Realtime Clock

Table 2.65 is a comparative overview of the realtime clocks, and Table 2.66 is a comparison of realtime clock registers.

Table 2.65 Comparative Overview of Realtime Clocks

Item	RX63N (RTCa)	RX671 (RTCd)
Count modes	Calendar count mode	Calendar count mode, binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment — Start/stop function — Binary display of 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz status. — Time error adjustment function — Clock (1 Hz) output	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment • Binary count mode — Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz/64 Hz) output
Interrupts	• Alarm interrupt (ALM) Year, month, date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt. • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) Indicates occurrence of a carry to the seconds counter or a carry to the 64 Hz counter when reading the 64 Hz counter.	• Alarm interrupt (ALM) Any of the following can be selected as conditions for the alarm interrupt: — Calendar count mode: Year, month, date, day of the week, hours, minutes, and seconds — Binary count mode: Each bit of 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings — When a carry from the 64 Hz counter to the second counter is generated. — When the 64 Hz counter is changed and the R64CNT register is read at the same time.

Item	RX63N (RTCa)	RX671 (RTCd)
Interrupts	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Times when any of three event signals are input can be captured. At each input event the month, date, hour, minute, and second is captured.	Time capture using edge detection on the time capture event input pin is available. At each input event the month, date, hour, minute, and second is captured, or the 32-bit counter value is captured.
Event link function	—	Periodic event output

Table 2.66 Comparison of Realtime Clock Registers

Register	Bit	RX63N (RTCa)	RX671 (RTCd)
BCNT0*1	—	—	Binary counter 0
BCNT1*1	—	—	Binary counter 1
BCNT2*1	—	—	Binary counter 2
BCNT3*1	—	—	Binary counter 3
BCNT0AR*1	—	—	Binary counter 0 alarm register
BCNT1AR*1	—	—	Binary counter 1 alarm register
BCNT2AR*1	—	—	Binary counter 2 alarm register
BCNT3AR*1	—	—	Binary counter 3 alarm register
BCNT0AER*1	—	—	Binary counter 0 alarm enable register
BCNT1AER*1	—	—	Binary counter 1 alarm enable register
BCNT2AER*1	—	—	Binary counter 2 alarm enable register
BCNT3AER*1	—	—	Binary counter 3 alarm enable register
RCR1	RTCOS	—	RTCOUT output select bit
RCR2	CNTMD	—	Count mode select bit
BCNT0CPn*1	—	—	BCNT0 capture register n (n = 0 to 2)
BCNT1CPn*1	—	—	BCNT1 capture register n (n = 0 to 2)
BCNT2CPn*1	—	—	BCNT2 capture register n (n = 0 to 2)
BCNT3CPn*1	—	—	BCNT3 capture register n (n = 0 to 2)

Note: 1. In binary count mode

2.26 Watchdog Timer

Table 2.67 is a comparative overview of the watchdog timers, and Table 2.68 is a comparison of watchdog timer registers.

Table 2.67 Comparative Overview of Watchdog Timers

Item	RX63N (WDTA)	RX671 (WDTA)
Count source	Peripheral clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	Divide by 4, 64, 128, 512, 2,048, or 8,192	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the WDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. (auto-start mode: automatic, register start mode: refresh)	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption state • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Watchdog timer reset sources	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Interrupt sources	Interrupt request output sources • Generation of a non-maskable interrupt (WUNI) by an underflow of the down-counter • Refresh outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the WDTSR register.	The down-counter value can be read by reading the WDTSR register.

Table 2.68 Comparison of Watchdog Timer Registers

Register	Bit	RX63N (WDTA)	RX671 (WDTA)
WDTRCR	RSTIRQS	Reset interrupt request selection bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request selection bit 0: Non-maskable interrupt request or interrupt request output is enabled.*1 1: Reset output is enabled.

Note: 1. A non-maskable interrupt is generated when the value of the NMIER.WDTEN bit is 1, and a maskable interrupt is generated when it is 0.

2.27 Independent Watchdog Timer

Table 2.69 is a comparative overview of the independent watchdog timers, and Table 2.70 is a comparison of independent watchdog timer registers.

Table 2.69 Comparative Overview of Independent Watchdog Timers

Item	RX63N (IWDTa)	RX671 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Count restarts automatically in auto-start mode, or by refreshing the counter in register start mode.	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Interrupt sources	Interrupt request output sources • Generation of a non-maskable interrupt (WUNI) by an underflow of the down-counter • Refresh outside the refresh-permitted period (refresh error)	Non-maskable interrupt/interrupt sources • Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.	The down-counter value can be read by reading the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX63N (IWDTa)	RX671 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.70 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX63N (IWDTa)	RX671 (IWDTa)
IWDTRCR	RSTIRQS	Reset interrupt request selection bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request selection bit 0: Non-maskable interrupt request or interrupt request output is enabled.*1 1: Reset output is enabled.

Note: 1. A non-maskable interrupt is generated when the value of the NMIER.IWDTEN bit is 1, and a maskable interrupt is generated when it is 0.

2.28 USB 2.0 Host/Function Module

Table 2.71 is a comparative overview of the USB 2.0 Host/Function modules, and Table 2.72 is a comparison of USB 2.0 Host/Function module registers.

Table 2.71 Comparative Overview of USB 2.0 Host/Function Modules

Item	RX63N (USBa)	RX671 (USBb)
Features	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 Two ports are provided. — USB0: Support for Host controller, Function controller, and USB OTG functionality — USB1: Support for Function controller • Internal host controller and function controller (which can be switched by software) • Self-power mode or bus-power mode can be selected. When Host controller operation is selected: • Full-speed transfer (12 Mbps) is supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub When Function controller operation is selected: • Support for full-speed transfer (12 Mbps) • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 — Support for Host controller, Function controller, and USB OTG functionality (two channels) • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected. When Host controller operation is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub When Function controller operation is selected: • Support for full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Internal bus interface	Connected to internal peripheral bus 3	Connected to internal peripheral bus 3

Item	RX63N (USBa)	RX671 (USBb)
Pipe configuration	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9. Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 8, 16, 32, and 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting), isochronous transfer buffer size: 1 to 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 1 to 64 bytes (single buffer)	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9. Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 64 bytes (support for double buffer setting), isochronous transfer buffer size: 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 64 bytes (single buffer)
Other functions	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip D+/D– pull-up and pull-down resistors
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state

Note: 1. Low-speed transfer (1.5 Mbps) is not supported when Function controller operation is selected.

Table 2.72 Comparison of USB 2.0 Host/Function Module Registers

Register	Bit	RX63N (USBa)	RX671 (USBb)
SYSSTS0	SOFEA	—	SOF active monitor flag when the host controller is selected
SOFCFG	TRNENSEL	Transaction-enabled time select bit 0: Low-speed communication is not supported. 1: Setting prohibited.	Transaction-enabled time select bit 0: Low-speed communication is not supported. 1: Low-speed communication is supported.
DEVADDn (n = 0 to 5)	USBSPD [1:0]	Transfer speed of communication target device bits b7 b6 0 0: DEVADDn register is not used. 0 1: Setting prohibited. 1 0: Full speed 1 1: Setting prohibited.	Transfer speed of communication target device bits b7 b6 0 0: DEVADDn register is not used. 0 1: Low speed 1 0: Full speed 1 1: Setting prohibited.
PHYSLEW	—	—	PHY cross point adjustment register
DPUSR0R	RPUE0	—	USB0 D+ pull-up resistor control bit
	DRPD0	—	USB0 D+/D– pull-down resistor control bit
	SRPC1	USB1 single end receiver control bit	—
	FIXPHY1	USB1 transceiver output fix bit	—
	DP1	USB1 DP input	—
	DM1	USB1 DM input	—
	DOVCA0	—	USB0 OVRCURA input flag
	DOVCB0	—	USB0 OVRCURB input flag
	DVBSTS0	—	USB0 VBUS input flag
	DVBSTS1	USB1 VBUS input	—
DPUSR1R	DPINTE1	USB1 DP interrupt enable/clear bit	—
	DMINTE1	USB1 DM interrupt enable/clear bit	—
	DVBSE1	USB1 VBUS interrupt enable/clear bit	—
	DPINT1	USB1 DP interrupt source recovery bit	—
	DMINT1	USB1 DM interrupt source recovery bit	—
	DVBINT1	USB1 VBUS interrupt source recovery bit	—

2.29 Serial Communications Interface

Table 2.73 is a comparative overview of the serial communications interfaces, Table 2.74 is a comparative listing of serial communications interface channels, and Table 2.75 is a comparison of serial communications interface registers.

Table 2.73 Comparative Overview of Serial Communications Interfaces

Item		RX63N (SCIc, SCId)	RX671 (SCIk, SCIm, SCIh)
Number of channels		• SCIc: 12 channels • SCId: 1 channel	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable using on-chip baud rate generator.	Bit rate specifiable using on-chip baud rate generator.
Full-duplex communication		• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering	• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering
Data transfer		Selectable between LSB-first and MSB-first	Selectable between LSB-first and MSB-first
I/O signal level inversion		—	Ability to invert levels of input and output signals independently
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error • Completion of generation of a start condition, restart condition, or stop condition (simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, data match • Completion of generation of a start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		Ability to set module stop state for each channel	Ability to transition each channel to module stop state
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even, odd, or none
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	Ability to use CTSn# and RTSn# pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control

Item		RX63N (SCIc, SCId)	RX671 (SCIk, SCIm, SCIh)
Asynchronous mode	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception
	Data match detection	—	Ability to compare receive data and comparison data, and generates an interrupt when they match
	Start-bit detection	—	Selectable between low level and falling edge
	Receive data sampling timing adjustment	—	Ability to change the sampling point for receive data forward or backward relative to a reference point at the center of the data
	Transmit signal change timing adjustment	—	Ability to delay the falling or rising edge of the transmit data
	Break detection	Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly	Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly or reading the SPTR.RXDMON flag
	Clock source	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)
	Double-speed mode	—	Ability to select baud rate generator double-speed mode
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation function	The input signal paths from the RXDn pins incorporate digital noise filters.	The input signal paths from the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	Ability to use CTSn and RTSn pins for transmission and reception control	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception
Smart card interface mode	Error processing	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention

Item		RX63N (SCIc, SCId)	RX671 (SCIk, SCIm, SCIh)
Simple I²C mode	Communication format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	• Max. 384 kbps • Support for fast mode	Support for fast mode
	Noise cancellation	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.
	Clock settings	Ability to select among four clock phase and clock polarity settings	Ability to select among four clock phase and clock polarity settings
Event link function (supported by SCI5 only)		—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output
Bit rate modulation function		—	Ability to reduce errors by correcting output from the on-chip baud rate generator
Extended serial mode (supported by SCI12 only)	Start Frame transmission	• Ability to output Break Field low width/output completion interrupt function • Bus collision detection function/detection interrupt function	• Ability to output Break Field low width/output completion interrupt function • Bus collision detection function/detection interrupt function
	Start Frame reception	• Ability to detect Break Field low width/detection completion interrupt function • Control Field 0 and Control Field 1 data comparison/ match interrupt function • Ability to select between two data types for comparison (primary and secondary) in Control Field 1 • Ability to set priority interrupt bit in Control Field 1 • Support for Start Frames that do not include a Break Field • Support for Start Frames that do not include Control Field 0 • Bit rate measurement function	• Ability to detect Break Field low width/detection completion interrupt function • Control Field 0 and Control Field 1 data comparison/ match interrupt function • Ability to select between two data types for comparison (primary and secondary) in Control Field 1 • Ability to set priority interrupt bit in Control Field 1 • Support for Start Frames that do not include a Break Field • Support for Start Frames that do not include Control Field 0 • Bit rate measurement function

Item		RX63N (SCIc, SCId)	RX671 (SCIk, SCIm, SCIh)
Extended serial mode (supported by SCI12 only)	I/O control function	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12
	Timer function	Usable as reload timer	Usable as reload timer

Table 2.74 Comparative Listing of Serial Communications Interface Channels

Item	RX63N (SCIc, SCId)	RX671 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI0 to SCI12	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI12	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI12	SCI0 to SCI12
Simple I^2C mode	SCI0 to SCI12	SCI0 to SCI12
Simple SPI mode	SCI0 to SCI12	SCI0 to SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	—	SCI5
FIFO mode	—	SCI10, SCI11
Data match detection	—	SCI0 to SCI11
Peripheral module clock	PCLKB: SCI0 to SCI12	PCLKB: SCI0 to SCI9, SCI12 PCLKA: SCI10, SCI11

Table 2.75 Comparison of Serial Communications Interface Registers

Register	Bit	RX63N (SCIc, SCId)	RX671 (SCIk, SCIm, SCIh)
SMR (When SCMR.SMIF = 0)	CHR	Character length bit (Valid only in asynchronous mode) 0: Selects 8 bits as the data length for transmission and reception 1: Selects 7 bits as the data length for transmission and reception	Character length bit (Valid only in asynchronous mode) Selection is made in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Selects 9 bits as the data length for transmission and reception 0 1: Selects 9 bits as the data length for transmission and reception 1 0: Selects 8 bits as the data length for transmission and reception 1 1: Selects 7 bits as the data length for transmission and reception
SSR	RDRF	—	Receive data full flag
	TDRE	—	Transmit data empty flag

Register	Bit	RX63N (SCIc, SCId)	RX671 (SCIk, SCIm, SCIh)
SSRFIFO	—	—	Serial status register (When SCMR.SMIF bit = 0 and FCR.FM bit = 1)
SCMR	CHR1	—	Character length bit 1
SEMR	ITE	—	Immediate transmit enable bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Clock-synchronous basic clock select extended bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited.	Bus collision detection clock select bits • When SEMR.BGDM bit = 0, or SEMR.BGDM bit = 1 and SMR.CKS[1.0] bits = other than 00b b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited. • When SEMR.BGDM bit = 1 and SMR.CKS[1.0] bits = 00b b5 b4 0 0: SCI base clock frequency divided by 2 0 1: SCI base clock frequency divided by 4 1 0: Setting prohibited. 1 1: Setting prohibited.
RDRH, RDRL, RDRHL	—	—	Receive data register H, L, HL
FRDR	—	—	Receive FIFO data register
TDRH, TDRL, TDRHL	—	—	Transmit data register H, L, HL
FTDR	—	—	Transmit FIFO data register
MDDR	—	—	Modulation duty register
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register

2.30 I²C bus Interface

Table 2.76 is a comparative overview of the I²C bus interfaces, and Table 2.77 is a comparison of I²C bus interface registers.

Table 2.76 Comparative Overview of I²C Bus Interfaces

Item	RX63N (RIIC)	RX671 (RIICa)
Communication format	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Up to 1 Mbps	Fast mode is supported (up to 1 Mbps).
Serial clock (SCL)	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	• Start, restart, and stop conditions are generated automatically. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are generated automatically. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Three slave addresses can be specified. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles (wait function)	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX63N (RIIC)	RX671 (RIICa)
Arbitration	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events (detection of AL, NACK, time-out, a start condition including a restart condition, or a stop condition) • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete	Four sources: • Error in transfer or occurrence of events (detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition) • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode

Item	RX63N (RIIC)	RX671 (RIICa)
Event link function (output)	—	Four sources (RIIC0): • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Table 2.77 Comparison of I²C Bus Interface Registers

Register	Bit	RX63N (RIIC)	RX671 (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT	—	Timeout internal counter	—

2.31 CAN Module

Table 2.78 is a comparative overview of the CAN modules.

Table 2.78 Comparative Overview of CAN Modules

Item	RX63N (CAN)	RX671 (CAN)
Number of channels	3 channels	2 channels
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX63N (CAN)	RX671 (CAN)
Transmission	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLKB), CANMCLK	Peripheral module clock (PCLKB), CANMCLK

Item	RX63N (CAN)	RX671 (CAN)
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2.32 Serial Peripheral Interface

Table 2.79 is a comparative overview of the serial peripheral interfaces, and Table 2.80 is a comparison of serial peripheral interface registers.

Table 2.79 Comparative Overview of Serial Peripheral Interfaces

Item	RX63N (RSPI)	RX671 (RSPId)
Number of channels	3 channels	3 channels
RSPI transfer functions	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Ability to perform transmit-only operation • Capable of serial communications in master/slave mode • Ability to switch the polarity of serial transfer clock • Ability to switch the phase of serial transfer clock	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Communication mode: Selectable between full-duplex and simplex (transmit-only or receive-only (in slave mode)) • Ability to switch the polarity of RSPCK • Ability to switch the phase of RSPCK
Data format	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame)	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame) • Ability to swap transmit/receive data in byte units • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4). — Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for both the transmit and receive buffers • 128 bits for the transmit/receive buffers

Item	RX63N (RSPI)	RX671 (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection When master receive and the RSPCK auto-stop function are enabled, the transfer clock stops at the point in time when overrun error detection occurs, so no overrun error is generated. • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLn0 to SSLn3) per channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode, the SSLn0 pin is input, and SSLn1 to SSLn3 pins are either output or unused. • In slave mode, the SSLn0 pin is input, and SSLn1 to SSLn3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLx0 to SSLx3) per channel • In single-master mode, SSLx0 to SSLx3 pins are output. • In multi-master mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are either output or unused. • In slave mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity
Control during master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified.	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified. • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.

Item	RX63N (RSPI)	RX671 (RSPId)
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt (mode fault, overrun, underrun, or parity error) • Idle interrupt • Communication end interrupt
Event link function (output)	—	The following events can be output to the event link controller (RSPI0): • Receive buffer full event signal • Transmit buffer empty event signal • Error events (mode fault, overrun, underrun, parity error) • Idle events • Communication completion events
Other functions	• Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.80 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX63N (RSPI)	RX671 (RSPId)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurred 1: A mode fault error occurred	Mode fault error flag 0: No mode fault error occurred, no underrun error occurred. 1: A mode fault error occurred, an underrun error occurred.
	UDRF	—	Underrun error flag
	SPTEF	—	Transmit buffer empty flag
	SPCF	—	Communication completion flag
	SPRF	—	Receive buffer full flag
SPDR	—	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: No transmit data parity bit appended No parity checking is performed on receive data. 1: A transmit data parity bit is appended. Parity checking is performed on receive data.	Parity enable bit 0: No transmit data parity bit appended No parity checking is performed on receive data. 1: A transmit data parity bit is appended, and parity checking is performed on receive data (when SPCR.TXMD = 0). A parity bit is appended to transmit data, but no parity checking is performed on receive data (when SPCR.TXMD = 1).
	SCKASE	—	RSPCK auto-stop function enable bit
SPDCR2	—	—	RSPI data control register 2
SPCR3	—	—	RSPI control register 3

2.33 CRC Calculator

Table 2.81 is a comparative overview of the CRC calculators, and Table 2.82 is a comparison of CRC calculator registers.

Table 2.81 Comparative Overview of CRC Calculators

Item	RX63N (CRC)	RX671 (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on eight bits in parallel	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	CRC code generation for LSB-first or MSB-first communication selectable	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Module stop state can be set	Ability to transition to module stop state	

Table 2.82 Comparison of CRC Calculator Registers

Register	Bit	RX63N (CRC)	RX671 (CRCA)
CRCCR	GPS[1:0] (RX63N) GPS[2:0] (RX671)	CRC generating polynomial switching bits (b1, b0) b1 b0 0 0: No calculation is executed. 0 1: $X^8 + X^2 + X + 1$ 1 0: $X^{16} + X^{15} + X^2 + 1$ 1 1: $X^{16} + X^{12} + X^5 + 1$	CRC generating polynomial switching bits (b2 to b0) b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register • When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)	CRC data input register • When generating 32-bit CRCs CRC data input register (b31 to b0) • When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)
CRCDOR	—	CRC data output register • When generating 16-bit CRCs CRC data output register (b15 to b0) The bottom byte (b7 to b0) is used when generating 8-bit CRCs.	CRC data output register • When generating 32-bit CRCs CRC data output register (b31 to b0) • When generating 16-bit CRCs CRC data output register (b15 to b0) • When generating 8-bit CRCs CRC data output register (b7 to b0)

2.34 Boundary Scan

Table 2.83 is a comparative overview of the boundary scan functions, and Table 2.84 is a comparison of boundary scan registers.

Table 2.83 Comparative Overview of Boundary Scan Functions

Item	RX63N	RX671
Boundary scan enable/disable	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.
Dedicated boundary scan pins	The following pins are used exclusively by the JTAG when the boundary scan function is enabled (TDO, TCK, TDI, TMS, and TRST#): • 177-pin TFLGA and 176-pin LFBGA products: PF0, PF1, PF2, PF3, and PF4 • 145-pin TFLGA products: P26, P27, P30, P31, and P34	The following pins are used exclusively by the JTAG when the boundary scan function is enabled (TDO, TCK, TDI, TMS, and TRST#): • 145-pin TFLGA and 64-pin TFBGA products: P26, P27, P30, P31, and P34
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

Table 2.84 Comparison of Boundary Scan Registers

Register	Bit	RX63N	RX671
JTIDR	—	ID code register	ID code register
		Initial value after a reset differs.	

2.35 12-Bit A/D Converter

Table 2.85 is a comparative overview of the 12-bit A/D converters, and Table 2.86 is a comparison of 12-bit A/D converter registers and Table 2.87 is a comparison of A/D conversion start triggers that can be set in the ADSTRGR registers.

Table 2.85 Comparative Overview of 12-Bit A/D Converters

Item	RX63N (S12ADa)	RX671 (S12ADFa)
Number of units	1 unit	2 units (S12AD and S12AD1)
Input channels	Up to 21 channels	S12AD: 8 channels S12AD1: 12 channels + one extended channel
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when operating with A/D conversion clock ADCLK = 50 MHz)	(0.48 µs) per channel (12-bit conversion mode) (0.45 µs) per channel (10-bit conversion mode) (0.42 µs) per channel (8-bit conversion mode) (Operating with A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock (ADCLK)	4 clocks: PCLK, PCLK/2, PCLK/4, PCLK/8	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the division ratio is one of the following: — PCLK: ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 • ADCLK is set using the clock generation circuit.
Data register	• For analog input: 21 data registers • For temperature sensor: One data register • For internal reference voltage: One data register • The results of A/D conversion are stored in 12-bit A/D data registers.	• For analog input: 20 data registers (S12AD: 8 data registers, S12AD1: 12 data registers), one data register for each unit for A/D conversion data multiplexing in double trigger mode, two data registers for each unit for A/D conversion data multiplexing in double trigger mode extended operation • For temperature sensor: One data register (S12AD1) • For internal reference voltage: One data register (S12AD1) • 1 register per unit for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion

Item	RX63N (S12ADa)	RX671 (S12ADFa)
Data register	• In A/D-converted value addition mode, A/D conversion results are stored in a 14-bit A/D data register.	• In value addition mode, the value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 21 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 21 user-selected channels.	Operating modes can be set independently for two units. • Single scan mode: — A/D conversion is performed only once on the analog inputs of user-selected channel. — A/D conversion is performed only once on the temperature sensor output (S12AD1). — A/D conversion is performed only once on the internal reference voltage (S12AD1). — A/D conversion is performed only once on the extended analog input (S12AD1). • Continuous scan mode: — A/D conversion is performed repeatedly on the arbitrarily selected analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1).

Item	RX63N (S12ADa)	RX671 (S12ADFa)
Operating mode		• Group scan mode: — Either two (A and B) or three (A, B, and C) groups can be selected. (When the number of groups selected is two, only the combination of group A and group B is selectable.) — The analog inputs of user-selected channels, the temperature sensor output (S12AD1), or the internal reference voltage (S12AD1) are divided up among group A and group B, or among groups A, B, and C, and A/D conversion is performed only once on the analog inputs selected as a group unit. — The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (with group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, and TMR. • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, TMR, and ELC. • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin (S12AD) or ADTRG1# pin (S12AD1). (independently for two units)

Item	RX63N (S12ADa)	RX671 (S12ADFa)
Functions	• Sample-and-hold function • Variable sampling state count • Selectable A/D-converted value adding mode	• Variable sampling state count (ability to set for each channel independently) • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Function for switching among 12-, 10-, and 8-bit conversion • A/D data register auto-clear function • Extended analog input function • Compare function (window A, window B)
Interrupt sources	• An scan end interrupt request (S12ADI0) can be generated on completion of A/D conversion.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a single scan. (independently for two units) • In double trigger mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan. (independently for two units) • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (S12GBADI or S12GBADI1) can be generated, and on completion of a group C scan a dedicated group C scan end interrupt request (S12GCADI or S12GCADI1) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of two scans of group A. On completion of two scans of group B or C a dedicated group B or group C scan end interrupt request (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated.

Item	RX63N (S12ADa)	RX671 (S12ADFa)
Interrupt sources	• An S12ADI0 interrupt can activate the DMAC and DTC.	• A compare interrupt (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated when the digital compare function comparison conditions are met. • The DMA controller (DMAC) or data transfer controller (DTC) can be activated by the S12ADI/S12ADI1, S12GBADI/S12GBADI1, or S12GCADI/S12GCADI1 interrupt.
Event link function	—	• An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.86 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX63N (S12ADa)	RX671 (S12ADFa)
ADCSR	—	A/D control register ADCSR is an 8-bit register.	A/D control register ADCSR is a 16-bit register.
	EXTRG	Trigger select bit (b0)	Trigger select bit (b8)
	TRGE	Trigger start enable bit (b1)	Trigger start enable bit (b9)
	CKS[1:0]	A/D conversion clock select bits	—
	ADIE	Scan end interrupt enable bit (b4)	Scan end interrupt enable bit (b12)
	ADCS (RX63N) ADCS[1:0] (RX671)	Scan mode select bit (b6) 0: Single scan mode 1: Continuous scan mode	Scan mode select bits (b14, b13) b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited
	ADST	A/D conversion start bit (b7)	A/D conversion start bit (b15)
	DBLANS[4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
ADANS0 (RX63N) ADANSA0 (RX671)	—	A/D channel select register 0	A/D channel select register A0
ADANS1	—	A/D channel select register 1	—
ADANSB0	—	—	A/D channel select register B0
ADANSC0	—	—	A/D channel select register C0
ADADS0	—	A/D-converted value addition mode select register 0	A/D-converted value addition/ average function select register 0
ADADS1	—	A/D-converted value addition mode select register 1	—

Register	Bit	RX63N (S12ADa)	RX671 (S12ADFa)
ADADC	ADC[1:0] (RX63N) ADC[2:0] (RX671)	Addition count select bits (b1, b0) b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	Addition count select bits (b2 to b0) b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Settings other than the above are prohibited.
	AVEE	—	Average mode enable bit
ADCER	ADPRC[1:0]	—	A/D conversion resolution setting bit
	DIAGVAL[1:0]	—	Self-diagnostic conversion voltage select bits
	DIAGLD	—	Self-diagnostic mode select bit
	DIAGM	—	Self-diagnostic enable bit
ADSTRGR	ADSTRS[3:0] (RX63N) TRSA[5:0] (RX671)	A/D conversion start trigger select bits (b3 to b0) Refer to Table 2.87 for details	A/D conversion start trigger select bits (b13 to b8) Refer to Table 2.87 for details
	TRSB[5:0]	—	A/D conversion start trigger select for group B bits
ADEXICR	TSS (RX63N) TSSA (RX671)	Temperature sensor output A/D conversion select bit	Temperature sensor output A/D conversion select bit
	OCS (RX63N) OCSA (RX671)	A/D internal reference voltage A/D conversion select bit	A/D internal reference voltage A/D conversion select bit
	TSSB	—	Temperature sensor output A/D conversion select bit
	OCSB	—	Internal reference voltage A/D conversion select bit
	EXSEL[1:0]	—	Extended analog input select bits
	EXOEN	—	Extended analog output control bit
ADDRy	—	A/D Data Register y (y = 0 to 20)	A/D Data Register y (y = 0 to 11)
ADSSTR01 (RX63N) ADSSTRn (RX671)	—	A/D sampling state register 01	A/D sampling state register n (n = 0 to 11)
ADSSTR23 (RX63N) ADSSTRT (RX671)	—	A/D sampling state register 23	A/D sampling state register T
ADSSTRO	—	—	A/D sampling state register O
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A

Register	Bit	RX63N (S12ADa)	RX671 (S12ADFa)
ADDBLDRB	—	—	A/D data duplication register B
ADRD	—	—	A/D self-diagnosis data register
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADDISCR	—	—	A/D disconnection detection control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0
ADCMPANSER	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	A/D comparison function window A comparison condition setting register 0
ADCMPLER	—	—	A/D comparison function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADSAM	—	—	A/D conversion time setting register
ADSAMPR	—	—	A/D conversion time setting protection release register

Table 2.87 Comparison of A/D Conversion Start Triggers Set in ADSTRGR Register

Bit	RX63N (S12ADa)	RX671 (S12ADFa)
ADSTRS[3:0] (RX63N) TRSA[5:0] (RX671)	A/D conversion start trigger select bits b3 b0 0 0 0 0: Asynchronous trigger 0 0 0 1: TRG0AN_0 0 0 1 0: TRG0BN_0 0 0 1 1: TRGAN_0 0 1 0 0: TRGAN_1 0 1 0 1: TRG0EN_0 0 1 1 0: TRG0FN_0 0 1 1 1: TRG04ABN_0 1 0 0 0: TRG04ABN_1 1 0 0 1: TMTRG0AN_0 1 0 1 0: TMTRG0AN_1	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 1 1 0 0 0 0: ELCTRG0N/ELCTRG1N

2.36 Temperature Sensor

Table 2.88 is a comparison of temperature sensor registers.

Table 2.88 Comparison of Temperature Sensor Registers

Register	Bit	RX63N	RX671 (TEMPS)
TSCDRH, TSCDRL (RX63N) TSCDR (RX671)	—	Temperature sensor calibration data register (b7 to b0) Bits 3 to 0 in TSCDRH and bits 7 to 0 in TSCDRL hold the temperature sensor calibration data measured for each chip at the time of shipment.	Temperature sensor calibration data register (b31 to b0) Bits 11 to 0 hold the temperature sensor calibration data measured for each chip at the time of shipment.

2.37 RAM

Table 2.89 is a comparative overview of the RAM, and Table 2.90 is a comparison of RAM registers.

Table 2.89 Comparative Overview of RAM

Item	RX63N	RX671
Capacity	• 64 KB RAM0: 64 KB • 128 KB RAM0: 64 KB, RAM1: 64 KB • 192 KB RAM0: 64 KB, RAM1: 128 KB • 256 KB RAM0: 64 KB, RAM1: 192 KB	• 384 KB
Address	• When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: None • When the RAM capacity is 128 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0001 FFFFh (64 KB) • When the RAM capacity is 192 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0002 FFFFh (128 KB) • When the RAM capacity is 256 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0003 FFFFh (192 KB)	0000 0000h to 0003 FFFFh
Memory bus	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. — The number of cycles required is doubled when an access spans an 8-byte boundary. • The RAM can be enabled or disabled.
Data retention function	Data in RAM0 can be retained in deep software standby mode.	Not available in deep software standby mode
Low power consumption function	The module stop state is independently selectable for RAM0 and RAM1.	Ability to transition to the module stop state.
Error checking function	—	• Parity check: Detection of 1-bit errors • Generation of non-maskable interrupt or interrupt when an error occurs

Table 2.90 Comparison of RAM Registers

Register	Bit	RX63N	RX671
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.38 Flash Memory

Table 2.91 is a comparative overview of the flash memory, and Table 2.92 is a comparison of flash memory registers.

Table 2.91 Comparative Overview of Flash Memory

Item	RX63N		RX671 (FLASH)	
	ROM	E2 DataFlash	Code Flash Memory	Data Flash Memory
Memory capacity	User area: 2 MB, 1.5 MB, 1 MB, 768 KB, 512 KB, 384 KB, 256 KB	Data area: 32 KB	User area: 2 MB, 1.5 MB, 1 MB	Data area: 8 KB
Address	• Products with capacity of 2 MB: FFE0 0000h to FFFF FFFFh • Products with capacity of 1.5 MB: FFE8 0000h to FFFF FFFFh • Products with capacity of 1 MB: FFF0 0000h to FFFF FFFFh • Products with capacity of 768 KB: FFF4 0000h to FFFF FFFFh • Products with capacity of 512 KB: FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB: FFFC 0000h to FFFF FFFFh	0010 0000h to 0010 7FFFh	• Products with capacity of 2 MB: FFE0 0000h to FFFF FFFFh • Products with capacity of 1.5 MB: FFE8 0000h to FFFF FFFFh • Products with capacity of 1 MB: FFF0 0000h to FFFF FFFFh	0010 0000h to 0010 1FFFh
ROM cache	—		• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—

Item	RX63N		RX671 (FLASH)	
	ROM	E2 DataFlash	Code Flash Memory	Data Flash Memory
Read cycles	High-speed read operation using 1 cycle of ICLK is supported.	A read operation takes six cycles of FCLK6 in words or bytes	• While ROM cache operation is enabled: —When the cache is hit: One cycle —When the cache is missed: One to two cycles when ICLK ≤ 60 MHz; two to three cycles when ICLK > 60 MHz • When ROM cache operation is disabled: —One cycle when ICLK ≤ 60 MHz —Two cycles when ICLK > 60 MHz	Reading proceeds in every cycle of FCLK.
Value after erase	FFh	Undfined	FFh	Undfined
Programming/ erasing method	• The chip incorporates a dedicated sequencer (FCU) for programming of the ROM/E2 DataFlash. • Programming and erasing the ROM/ E2 DataFlash are handled by issuing commands to the FCU.		• Use of FACI commands specified in the FACI command issuing area (007E 0000h) to program and erase the code flash memory and data flash memory, and to program the option-setting memory (self-programming) • Programming/erasure through communication by a serial-programmer via a serial interface (serial programming)	
Security function	Protects against illicit tampering with or reading out of data in flash memory		Protects against illicit tampering with or reading out of data in flash memory	
Protection function	Protection against rewriting of the flash memory (software protection, error protection, and boot program protection)		Protection against rewriting of the flash memory (software protection, error protection, startup program protection, area protection, and dual bank function)	

Item	RX63N		RX671 (FLASH)	
	ROM	E2 DataFlash	Code Flash Memory	Data Flash Memory
Dual bank function	—		The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area • Dual mode: the code flash memory is divided into two areas	—
Trusted Memory (TM) function	—		Protection against unauthorized reading of the code flash memory • Linear mode: blocks 8, 9 • Dual mode: blocks 8, 9 ,46, and 47	—
Background operation (BGO) function	The CPU is able to execute program code from the ROM while the E2 DataFlash memory is being programmed or erased.		• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area or user boot area: 128 bytes • Units of erasure for the user area: In block units • Units of erasure for the user boot area: 16 KB	• Unit of programming for the data area: 2 bytes • Unit of erasure for the data area: 32 bytes	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: 64, 128, or 256 bytes
Other functions	• Ability to accept interrupts during self-programming • Ability to specify initial settings for the microcontroller in option-setting memory		• Ability to accept interrupts during self-programming • Ability to specify initial settings for the microcontroller in option-setting memory	

Item	RX63N		RX671 (FLASH)	
	ROM	E2 DataFlash	Code Flash Memory	Data Flash Memory
On-board programming (Serial programming/ self-programming)	Programming in boot mode — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area can also be programmed. • Programming in USB boot mode — USB0 is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming in user boot mode — Users can create their own boot programs. • Programming by a routine for ROM/E2 DataFlash programming within the user program — This allows ROM/E2 DataFlash programming without resetting the system.		• Programming/erasing in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Programming/erasing in boot mode (for the USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasing in boot mode (FINE interface) — Uses FINE. • Programming and erasure in single-chip mode — Programming and erasure can be performed by a code flash memory or data flash memory programming routine in a user program.	
Off-board programming	A flash programmer can be used to program the user area and user boot area. (products with 100 pins or more)	A flash programmer cannot be used to program the data area. (products with 100 pins or more)	A parallel programmer can be used to program and erase the code flash memory and option-setting memory.	A parallel programmer cannot be used to program and erase the data flash memory.
Unique ID	A 16-byte ID code is provided for each MCU. (This unique ID can be used on G-version products only.)		A 16-byte ID code provided for each MCU	

Table 2.92 Comparison of Flash Memory Registers

Register	Bit	RX63N	RX671 (FLASH)
FWEPROR	FLWE[1:0]	Flash programming/erasure bits b1 b0 0 0: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking disabled. 0 1: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking enabled. 1 0: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking disabled. 1 1: Programming/erasure, programming/erasure of lock bits, reading of lock bits, and blank checking disabled.	Flash programming and erasure enable bits b1 b0 0 0: Programming/erasure and blank checking disabled. 0 1: Programming/erasure and blank checking enabled. 1 0: Programming/erasure and blank checking disabled. 1 1: Programming/erasure and blank checking disabled.
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	E2 DataFlash programming/erasure protection violation flag	—
	DFLRPE	E2 DataFlash read protection violation flag	—
	DFLAE (RX63N) DFAE (RX671)	E2 DataFlash access violation flag	Data flash memory access violation flag
	ROMAE (RX63N) CFAE (RX671)	ROM access violation flag	Code flash memory access violation flag
FAEINT	—	Flash access error interrupt enable register	Flash access error interrupt enable register
		Initial values after a reset are different.	
	DFLWPEIE	E2 DataFlash programming/erasure protection violation interrupt enable bit	—
	DFLRPEIE	E2 DataFlash read protection violation interrupt enable bit	—
	DFLAEIE (RX63N) DFAEIE (RX671)	E2 DataFlash access violation interrupt enable bit	Data flash memory access violation interrupt enable bit*1
	ROMAEIE (RX63N) CFAEIE (RX671)	ROM access violation interrupt enable bit	Code flash memory access violation interrupt enable bit
DFLRE0	—	E2 DataFlash read enable register 0	—

Register	Bit	RX63N	RX671 (FLASH)
DFLRE1	—	E2 DataFlash read enable register 1	—
DFLWE0	—	E2 DataFlash P/E enable register 0	—
DFLWE1	—	E2 DataFlash P/E enable register 1	—
FCURAME	—	FCURAM enable register	—
FSTATR0 (RX63N) FSTATR (RX671)	—	Flash status register 0 FSTATR0 is an 8-bit register.	Flash status register FSTATR is a 32-bit register.
	PRGSPD	Programming suspend status flag (b0)	Programming suspend status flag (b8)
	ERSSPD	Erasure suspend status flag (b1)	Erasure suspend status flag (b9)
	DBFULL	—	Data buffer full flag
	SUSRDY	Suspend ready flag (b3)	Suspend ready flag (b11)
	PRGERR	Programming error flag (b4)	Programming error flag (b12)
	ERSERR	Erasure error bit (b5)	Erasure error flag (b13)
	ILGLERR	Illegal command error flag (b6)	Illegal command error flag (b14)
	FRDY	Flash ready flag (b7)	Flash ready flag (b15)
	FLWEERR	—	Flash write/erase protect error flag
	OTERR	—	Other error flag
	SECERR	—	Security error flag
	FESETERR	—	FENTRY setting error flag
	ILGCOMERR	—	Illegal command error flag
FSTATR1	—	Flash status register 1	—
FENTRYR	FENTRY0	ROM P/E mode entry 0 bit	—
	FENTRY1	ROM P/E mode entry 1 bit	—
	FENTRY2	ROM P/E mode entry 2 bit	—
	FENTRY3	ROM P/E mode entry 3 bit	—
	FENTRYC	—	Code flash P/E mode entry bit
	FEKEY[7:0] (RX63N) KEY[7:0] (RX671)	Key code bits	Key code bits
FPROTR	—	Flash protection register	—
FRESETR	—	Flash reset register	—
DFLBCCNT	—	E2 DataFlash blank check control register	—
FPESTAT	—	Flash P/E status register	—
DFLBCSTAT	—	E2 DataFlash blank check status register	—
PCKAR (RX63N) FPCKAR (RX671)	KEY[7:0]	—	Key code bits
UIDRn	—	Unique ID registers n (n = 0 to 15)	Unique ID registers n (n = 0 to 3)
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register
NCRGn	—	—	Non-cacheable area n address register (n = 0 or 1)

Register	Bit	RX63N	RX671 (FLASH)
NCRCn	—	—	Non-cacheable area n setting register (n = 0 or 1)
FSADDR	—	—	FACI command processing start address register
FEADDR	—	—	FACI command processing end address register
FSUINITR	—	—	Flash sequencer set-up initialization register
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FAWMON	—	—	Flash access window monitor register
FSUACR	—	—	Start-up area control register
EEPFCLK	—	—	Data flash memory access frequency setting register

2.39 Packages

As indicated in Table 2.93, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.93 Packages

Package Type	Renesas Code	
	RX63N	**RX671**
177-pin TFLGA	○	×
176-pin LFBGA	○	×
176-pin LQFP	○	×
145-pin TFLGA	PTLG0145KA-A	PTLG0145JC-A, PTLG0145KB-A
100-pin TFLGA	PTLG0100JA-A	PTLG0100JB-A
64-pin LQFP (RX63N) 64-pin LFQFP (RX671)	PLQP0064KB-A	PLQP0064KB-C
64-pin TFLGA	○	×
64-pin TFBGA	×	○
48-pin LQFP	○	×
48-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 145-Pin TFLGA Package (RX671: 0.65 mm Pin Pitch)

Table 3.1 is a comparative listing of the pin functions of 145-pin TFLGA package (RX671: 0.65 mm pin pitch) products.

Table 3.1 Comparative Listing of 145-Pin TFLGA Package Pin Functions (RX671: 0.65 mm Pin Pitch)

145-Pin TFLGA	RX63N	RX671 (0.65 mm Pin Pitch)
A1	AVSS0	AVSS0
A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
A6	P90/A16/TXD7/SMOSI7/SSDA7/AN014	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/AN108
A7	P92/A18/RXD7/SMISO7/SSCL7/AN016	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ IRQ10
A8	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/ CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
A9	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/ IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
A10	VSS	VSS
A11	P62/CS2#/RAS#	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
A12	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A13	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/ PO26/POE8#/CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3/AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
B1	VREFH	AVCC1
B2	AVCC0	AVCC0
B3	P05/IRQ13/DA1	P05/IRQ13
B4	VREFL0	VREFL0
B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B7	P91/A17/SCK7/AN015	P91/A17/SCK7/IRQ9
B8	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
B9	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
B10	VCC	VCC
B11	P61/CS1#/SDCS#	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
B12	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/ PO23/RXD12/SMISO12/SSCL12/RXDX12/ SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ TIOCA10/PO28/SSLB0/ET_ERXD2/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
C1	VREFL	AVSS1

145-Pin TFLGA	RX63N	RX671 (0.65 mm Pin Pitch)
C2	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10/AN109
C3	VREFH0	VREFH0
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
C6	VSS	VSS
C7	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/ MOSIC/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
C8	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/ RSPCKC/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/ IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
C10	P63/CS3#/CAS#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
C11	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
C12	P70/SDCLK	P70/SDCLK/IRQ0
C13	VSS	VSS
D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN111
D2	PF5/IRQ4	PF5/IRQ4
D3	P03/IRQ11/DA0	P03/IRQ11
D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN110
D5	VCC	VCC
D6	P93/A19/CTS7#/RTS7#/SS7#/AN017	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
D7	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/ IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/ AN102
D8	P60/CS0#	P60/CS0#/IRQ0
D9	P64/CS4#/WE#	P64/CS4#/WE#/D3[A3/D3]/IRQ4
D10	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/ AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
D11	VCC	VCC
D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ TIOCB10/RSPCKB/ET_RX_CLK/REF50CK/ IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
D13	PE6/D14[A14/D14]/TIOCA11/MOSIB/IRQ6/ AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
E1	VSS	VSS
E2	VCL	VCL
E3	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
E4	EMLE	EMLE
E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
E10	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/ SSLA1/ET_TX_EN/RMII_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E11	P66/CS6#/DQM0/CTX2*2	P66/CS6#/DQM0/MTIOC7D/IRQ14
E12	P65/CS5#/CKE	P65/CS5#/CKE/IRQ13
E13	P67/CS7#/DQM1/CRX2*2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT

145-Pin TFLGA	RX63N	RX671 (0.65 mm Pin Pitch)
F3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
F4	VBATT	VBATT
F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ET_MDIO/ IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/IRQ6-DS
F11	VSS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/ IRQ5-DS
F12	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/ET_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
F13	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/ IRQ10
G1	XTAL/P37	XTAL/P37
G2	RES#	RES#
G3	MD/FINED	MD/FINED
G4	BSCANP	BSCANP
G10	PA5/A5/TIOCB1/PO21/RSPCKA/ ET_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA/ ET_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14
G12	VCC	VSS_USB
G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ ET_MDC/IRQ5-DS	USB1_DP
H1	EXTAL/P36	EXTAL/P36
H2	VCC	VCC
H3	VSS	VSS
H4	P35/NMI	UPSEL/P35/NMI
H10	P72/CS2#/ET_MDC	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ IRQ12
H11	P71/CS1#/ET_MDIO	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ RSPCKA/ET_ERXD1/RMII_RXD1/IRQ12	VCC_USB
H13	PA7/A7/TIOCB2/PO23/MISOA/ET_WOL	USB1_DM
J1	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/ SCK6/SCK0/USB0_DPRPD/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
J2	P33/MTIOC0D/TIOCD0/TMRI3/PO11/ POE3#/RXD6/RXD0/SMISO6/SMISO0/ SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2

145-Pin TFLGA	RX63N	RX671 (0.65 mm Pin Pitch)
J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB/ USB0_DRPD/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE3#/SCK4/SCK6/ ET_RX_ER/RMII_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
J11	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/ET_TX_EN/RMII_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/ET_ERXD0/RMII_RXD0/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/IRQ4-DS
K1	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A/IRQ7/TS2
K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/ IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
K5	TRDATA2/P54/ALE/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
K6	BCLK/P53*1	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
K8	VCC	VCC
K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/ET_TX_EN/RMII_TXD_EN	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ USB1_EXICEN/SDHI_WP/QIO2-A/IRQ8
K10	P76/CS6#/PO22/RXD11/SMISO11/SSCL11/ ET_RX_CLK/REF50CK	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14
K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/ET_CRS/RMII_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/ET_ETXD1/RMII_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE1#/SCK9/ET_ETXD0/ RMII_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT

145-Pin TFLGA	RX63N	RX671 (0.65 mm Pin Pitch)
L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/USB0_DPUPE/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/ SCL2-DS/IERXD/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
L6	P56/EDACK1/MTIOC3C/TIOCA1	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6
L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
L8	TRCLK/P83/EDACK1/MTIOC4C/CTS10#/ RTS10#/SS10#/ET_CRS/RMII_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/PO29/SCK8/ RSPCKA/ET_ETXD2	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/ TCLKE/TMCI1/PO25/POE0#/SCK5/CTS8#/ RTS8#/SS8#/SSLA0/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/ TSCAP
L11	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD/ET_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
L12	P73/CS3#/PO16/ET_WOL	TRDATA4/P73/CS3#/PO16/USB1_VBUS/ USB1_VBUSEN/USB1_OVRCURB/IRQ8
L13	VSS	VSS
M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_DRPD/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
M2	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/PIXD3/ IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
M3	P86/TIOCA0/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/ IRQ14
M4	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
M5	VCC_USB	VCC_USB
M6	VSS_USB	VSS_USB
M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0

145-Pin TFLGA	RX63N	RX671 (0.65 mm Pin Pitch)
M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/ TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/ ET_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
M9	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ RXD10/SMISO10/SSCL10/ ET_ETXD0/ RMII_TXD0	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ SMISO10/SSCL10/RXD10/SMISO010/ SSCL010/RXD010/USB1_OVRCURB/ SDHI_CD/QIO3-A/IRQ9
M10	P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/ ET_RX_ER/RMII_RX_ER	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/SMOSI011/SSDA011/ TXD011/USB1_ID/SDHI_CLK-A/QSPCLK-A/ IRQ7
M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1/SCL3/ET_ERXD3/ IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2/SDA3/ET_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
M13	VCC	VCC
N1	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/ SMISO0/SSCL0/SCL1/USB0_EXICEN/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/PIXD4/ IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
N3	P87/TIOCA2/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
N5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
N6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
N7	TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/ET_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
N8	VSS	VSS
N9	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/ TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/ ET_COL/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ MISOA-A/SSITXD0/SMOSI010/SSDA010/ TXD010/MISO0-A/IRQ14
N10	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ TXD10/SMOSI10/SSDA10/ET_ETXD1/ RMII_TXD1	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/USB1_VBUSEN/IRQ2
N11	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD/ET_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
N12	P75/CS5#/PO20/SCK11/ET_ERXD0/ RMII_RXD0	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ SCK011/RTS011#/DE011/USB1_OVRCURA/ SDHI_D2-A/IRQ13

145-Pin TFLGA	RX63N	RX671 (0.65 mm Pin Pitch)
N13	P74/CS4#/PO19/CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/USB1_VBUSEN/ IRQ12

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Valid only on products with a ROM capacity of 2 MB or 1.5 MB.

3.2 145-Pin TFLGA Package (RX671: 0.50 mm Pin Pitch)

Table 3.2 is a comparative listing of the pin functions of 145-pin TFLGA package (RX671: 0.50 mm pin pitch) products.

Table 3.2 Comparative Listing of 145-Pin TFLGA Package Pin Functions (RX671: 0.50 mm Pin Pitch)

145-Pin TFLGA	RX63N	RX671 (0.50 mm Pin Pitch)
A1	AVSS0	AVSS0
A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
A6	P90/A16/TXD7/SMOSI7/SSDA7/AN014	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/AN108
A7	P92/A18/RXD7/SMISO7/SSCL7/AN016	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ IRQ10
A8	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/ CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
A9	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/ IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
A10	VSS	VSS
A11	P62/CS2#/RAS#	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
A12	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A13	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/ PO26/POE8#/CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3/AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
B1	VREFH	AVCC1
B2	AVCC0	AVCC0
B3	P05/IRQ13/DA1	P05/IRQ13
B4	VREFL0	VREFL0
B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
B7	P91/A17/SCK7/AN015	P91/A17/SCK7/IRQ9
B8	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
B9	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
B10	VCC	VCC
B11	P61/CS1#/SDCS#	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
B12	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/ PO23/RXD12/SMISO12/SSCL12/RXDX12/ SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ TIOCA10/PO28/SSLB0/ET_ERXD2/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
C1	VREFL	AVSS1
C2	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10/AN109
C3	VREFH0	VREFH0
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
C6	VSS	VSS

145-Pin TFLGA	RX63N	RX671 (0.50 mm Pin Pitch)
C7	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/MOSIC/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC-A/IRQ1/AN106
C8	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/RSPCKC/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/SDHI_D1-B/QIO1-B/IRQ7/AN100
C10	P63/CS3#/CAS#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
C11	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/SSLB1-B/IRQ8/ANEX0
C12	P70/SDCLK	P70/SDCLK/IRQ0
C13	VSS	VSS
D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN111
D2	PF5/IRQ4	PF5/IRQ4
D3	P03/IRQ11/DA0	P03/IRQ11
D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN110
D5	VCC	VCC
D6	P93/A19/CTS7#/RTS7#/SS7#/AN017	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
D7	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/AN102
D8	P60/CS0#	P60/CS0#/IRQ0
D9	P64/CS4#/WE#	P64/CS4#/WE#/D3[A3/D3]/IRQ4
D10	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/QIO1-B/IRQ7
D11	VCC	VCC
D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/TIOCB10/RSPCKB/ET_RX_CLK/REF50CK/IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/MTIOC2B/RSPCKB-B/IRQ5
D13	PE6/D14[A14/D14]/TIOCA11/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/QIO0-B/IRQ6
E1	VSS	VSS
E2	VCL	VCL
E3	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
E4	EMLE	EMLE
E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
E10	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/SSLA1/ET_TX_EN/RMII_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E11	P66/CS6#/DQM0/CTX2*2	P66/CS6#/DQM0/MTIOC7D/IRQ14
E12	P65/CS5#/CKE	P65/CS5#/CKE/IRQ13
E13	P67/CS7#/DQM1/CRX2*2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT
F3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
F4	VBATT	VBATT
F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS

145-Pin TFLGA	RX63N	RX671 (0.50 mm Pin Pitch)
F11	VSS	VSS
F12	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/ET_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
F13	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/IRQ10
G1	XTAL/P37	XTAL/P37
G2	RES#	RES#
G3	MD/FINED	MD/FINED
G4	BSCANP	BSCANP
G10	PA5/A5/TIOCB1/PO21/RSPCKA/ ET_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA/ ET_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/ SS12#/IRQ14
G12	VCC	VCC
G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ ET_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
H1	EXTAL/P36	EXTAL/P36
H2	VCC	VCC
H3	VSS	VSS
H4	P35/NMI	UPSEL/P35/NMI
H10	P72/CS2#/ET_MDC	P72/A19/CS2#/IRQ10
H11	P71/CS1#/ET_MDIO	P71/A18/CS1#/IRQ1
H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ RSPCKA/ET_ERXD1/RMII_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ IRQ12
H13	PA7/A7/TIOCB2/PO23/MISOA/ET_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
J1	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/ SCK6/SCK0/USB0_DPRPD/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
J2	P33/MTIOC0D/TIOCD0/TMRI3/PO11/ POE3#/RXD6/RXD0/SMISO6/SMISO0/ SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
J4	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB/ USB0_DRPD/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE3#/SCK4/SCK6/ ET_RX_ER/RMII_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
J11	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/ET_TX_EN/RMII_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4

145-Pin TFLGA	RX63N	RX671 (0.50 mm Pin Pitch)
J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/ET_ERXD0/RMII_RXD0/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/IRQ4-DS
K1	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2
K2	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
K3	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/ IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
K5	TRDATA2/P54/ALE/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/ ET_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
K6	BCLK/P53*1	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
K8	VCC	VCC
K9	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/ET_TX_EN/RMII_TXD_EN	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ SDHI_WP/QIO2-A/IRQ8
K10	P76/CS6#/PO22/RXD11/SMISO11/SSCL11/ ET_RX_CLK/REF50CK	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14
K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/ET_CRS/RMII_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/ET_ETXD1/RMII_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE1#/SCK9/ET_ETXD0/ RMII_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/USB0_DPUPE/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/ SCL2-DS/IERXD/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#

145-Pin TFLGA	RX63N	RX671 (0.50 mm Pin Pitch)
L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
L6	P56/EDACK1/MTIOC3C/TIOCA1	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6
L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
L8	TRCLK/P83/EDACK1/MTIOC4C/CTS10#/ RTS10#/SS10#/ET_CRS/RMII_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/PO29/SCK8/ RSPCKA/ET_ETXD2	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/ TS14
L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/ TCLKE/TMCI1/PO25/POE0#/SCK5/CTS8#/ RTS8#/SS8#/SSLA0/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/ TSCAP
L11	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD/ET_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
L12	P73/CS3#/PO16/ET_WOL	TRDATA4/P73/CS3#/PO16/IRQ8
L13	VSS	VSS
M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_DRPD/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
M2	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/PIXD3/ IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
M3	P86/TIOCA0/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/ IRQ14
M4	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
M5	VCC_USB	VCC_USB
M6	VSS_USB	VSS_USB
M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/ TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/ ET_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
M9	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ RXD10/SMISO10/SSCL10/ET_ETXD0/ RMII_TXD0	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ SMISO10/SSCL10/RXD10/SMISO010/ SSCL010/RXD010/SDHI_CD/QIO3-A/IRQ9

145-Pin TFLGA	RX63N	RX671 (0.50 mm Pin Pitch)
M10	P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/ ET_RX_ER/RMII_RX_ER	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/SMOSI011/SSDA011/ TXD011/SDHI_CLK-A/QSPCLK-A/IRQ7
M11	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1/SCL3/ET_ERXD3/ IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2/SDA3/ET_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
M13	VCC	VCC
N1	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/ SMISO0/SSCL0/SCL1/USB0_EXICEN/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/PIXD4/ IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
N3	P87/TIOCA2/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
N5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
N6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
N7	TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/ET_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
N8	VSS	VSS
N9	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/ TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/ ET_COL/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ MISOA-A/SSITXD0/SMOSI010/SSDA010/ TXD010/MISO0-A/IRQ14
N10	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ TXD10/SMOSI10/SSDA10/ET_ETXD1/ RMII_TXD1	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/IRQ2
N11	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD/ET_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
N12	P75/CS5#/PO20/SCK11/ET_ERXD0/ RMII_RXD0	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ SCK011/RTS011#/DE011/SDHI_D2-A/ IRQ13
N13	P74/CS4#/PO19/CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/IRQ12

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Valid only on products with a ROM capacity of 2 MB or 1.5 MB.

3.3 144-Pin LQFP/144-Pin LFQFP Package

Table 3.3 is a comparative listing of the pin functions of 144-pin LQFP/144-pin LFQFP package products.

Table 3.3 Comparative Listing of 144-Pin LQFP/144-Pin LFQFP Package Pin Functions

144-Pin	RX63N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/IRQ13
3	VREFH	AVCC1
4	P03/IRQ11/DA0	P03/IRQ11
5	VREFL	AVSS1
6	P02/TMCI1/SCK6/IRQ10/AN020	P02/TMCI1/SCK6/IRQ10/AN109
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN019	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN110
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN018	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN111
9	PF5/IRQ4	PF5/IRQ4
10	EMLE	EMLE
11	PJ5	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	VSS	VSS
13	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
14	VCL	VCL
15	VBATT	VBATT
16	MD/FINED	MD/FINED
17	XCIN	XCIN
18	XCOUT	XCOUT
19	RES#	RES#
20	XTAL/P37	XTAL/P37
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36
23	VCC	VCC
24	P35/NMI	UPSEL/P35/NMI
25	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/ SCK6/SCK0/USB0_DPRPD/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
26	P33/MTIOC0D/TIOCD0/TMRI3/PO11/ POE3#/RXD6/RXD0/SMISO6/SMISO0/ SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/CTX0/ USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
28	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/ IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB/ USB0_DRPD/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
30	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2

144-Pin	RX63N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
32	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
33	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
34	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/USB0_DPUPE/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
35	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_DRPD/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
36	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/ SMISO0/SSCL0/SCL1/USB0_EXICEN/ PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/PIXD4/ IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
38	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/PIXD3/ IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
39	P87/TIOCA2/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
40	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/MOSIA/SCL2-DS/ IERXD/USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
41	P86/TIOCA0/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/IRQ14
42	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
45	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
46	VCC_USB	VCC_USB
47	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
48	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
49	VSS_USB	VSS_USB
50	P56/EDACK1/MTIOC3C/TIOCA1	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6

144-Pin	RX63N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
51	TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET_EXOUT/IRQ10	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/CRX1/MISOC-B/IRQ10
52	TRDATA2/P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET_LINKSTA	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/MOSIC-B/IRQ4
53	BCLK/P53*1	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
54	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/IRQ2
55	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/IRQ1
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A/IRQ0
57	VSS	VSS
58	TRCLK/P83/EDACK1/MTIOC4C/CTS10#/RTS10#/SS10#/ET_CRS/RMII_CRS_DV	TRCLK/P83/EDACK1/MTIOC4C/SS10#/CTS10#/SCK10/SS010#/CTS010#/SCK010/IRQ3
59	VCC	VCC
60	PC7/A23/CS0#/MTIOC3A/MTCLKB/TIOCB6/TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/ET_COL/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/SSITXD0/SMOSI010/SSDA010/TXD010/MISO0-A/IRQ14
61	PC6/A22/CS1#/MTIOC3C/MTCLKA/TIOCA6/TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/ET_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/SSILRCK0/SMISO010/SSCL010/RXD010/MOSI0-A/IRQ13/TS13
62	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TIOCD6/TCLKF/TMRI2/PO29/SCK8/RSPCKA/ET_ETXD2	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/SCK10/RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/IRQ5/TS14
63	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/ET_ETXD1/RMII_TXD1	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/SMOSI10/SSDA10/TXD10/SMOSI010/SSDA010/TXD010/IRQ2
64	TRDATA1/P81/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/ET_ETXD0/RMII_TXD0	TRDATA1/P81/EDACK0/MTIOC3D/PO27/SMISO10/SSCL10/RXD10/SMISO010/SSCL010/RXD010/SDHI_CD/QIO3-A/IRQ9
65	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/SCK10/ET_TX_EN/RMII_TXD_EN	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/SCK010/RTS010#/DE010/SDHI_WP/QIO2-A/IRQ8
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TIOCC6/TCLKE/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/AUDIO_CLK/SS010#/CTS010#/RTS010#/DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/TSCAP
67	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/IETXD/ET_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/QIO0-A/IRQ11
68	P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/ET_RX_ER/RMII_RX_ER	TRDATA7/P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/SDHI_CLK-A/QSPCLK-A/IRQ7

144-Pin	RX63N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
69	P76/CS6#/PO22/RXD11/SMISO11/SSCL11/ET_RX_CLK/REF50CK	TRDATA6/P76/CS6#/PO22/SMISO11/SSCL11/RXD11/SMISO011/SSCL011/RXD011/SDHI_CMD-A/QSSL-A/IRQ14
70	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3/IERXD/ET_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/TXDB011/SSL03-A/SDHI_D3-A/IRQ10
71	P75/CS5#/PO20/SCK11/ET_ERXD0/RMII_RXD0	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/SCK011/RTS011#/DE011/SDHI_D2-A/IRQ13
72	P74/CS4#/PO19/CTS11#/RTS11#/SS11#/ET_ERXD1/RMII_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/CTS11#/SS011#/CTS011#/IRQ12
73	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2/SDA3/ET_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15
74	VCC	VCC
75	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1/SCL3/ET_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/SSCL011/SSL01-A/IRQ14/TS16
76	VSS	VSS
77	P73/CS3#/PO16/ET_WOL	TRDATA4/P73/CS3#/PO16/IRQ8
78	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET_CRS/RMII_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/IRQ15
79	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET_ETXD1/RMII_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SMISO011/SSCL011/RXD011/IRQ6
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE1#/SCK9/ET_ETXD0/RMII_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/IRQ13
81	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET_TX_EN/RMII_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SS011#/CTS011#/RTS011#/DE011/IRQ4
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE3#/SCK4/SCK6/ET_RX_ER/RMII_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/PMC0-DS/IRQ3
83	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET_RX_CLK/REF50CK	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET_ERXD0/RMII_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS
85	P72/CS2#/ET_MDC	P72/A19/CS2#/IRQ10
86	P71/CS1#/ET_MDIO	P71/A18/CS1#/IRQ1
87	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/RSPCKA/ET_ERXD1/RMII_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/IRQ12
88	PA7/A7/TIOCB2/PO23/MISOA/ET_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/IRQ7
89	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA/ET_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/IRQ14
90	PA5/A5/TIOCB1/PO21/RSPCKA/ET_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/RSPCK0-B/IRQ5

144-Pin	RX63N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ ET_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
95	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/IRQ10
96	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/ET_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
97	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/ SSLA1/ET_TX_EN/RMII_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
98	P67/CS7#/DQM1/CRX2*2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	P66/CS6#/DQM0/CTX2*2	P66/CS6#/DQM0/MTIOC7D/IRQ14
100	P65/CS5#/CKE	P65/CS5#/CKE/IRQ13
101	PE7/D15[A15/D15]/TIOCB11/MISOB/IRQ7/ AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
102	PE6/D14[A14/D14]/TIOCA11/MOSIB/IRQ6/ AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
103	VCC	VCC
104	P70/SDCLK	P70/SDCLK/IRQ0
105	VSS	VSS
106	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ TIOCB10/RSPCKB/ET_RX_CLK/REF50CK/ IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
107	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ TIOCA10/PO28/SSLB0/ET_ERXD2/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
108	PE3/D11[A11/D11]/MTIOC4B/TIOCB9/ PO26/POE8#/CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3/AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
109	PE2/D10[A10/D10]/MTIOC4A/TIOCA9/ PO23/RXD12/SMISO12/SSCL12/RXDX12/ SSLB3/MOSIB/IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
110	PE1/D9[A9/D9]/MTIOC4C/TIOCD9/PO18/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2/RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
111	PE0/D8[A8/D8]/TIOCC9/SCK12/SSLB1/ ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/SSLB1-B/IRQ8/ANEX0
112	P64/CS4#/WE#	P64/CS4#/WE#/D3[A3/D3]/IRQ4
113	P63/CS3#/CAS#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
114	P62/CS2#/RAS#	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
115	P61/CS1#/SDCS#	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
116	VSS	VSS
117	P60/CS0#	P60/CS0#/IRQ0
118	VCC	VCC

144-Pin	RX63N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
119	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/SDHI_D1-B/QIO1-B/IRQ7/AN100
120	PD6/D6[A6/D6]/MTIC5V/POE1#/SSLC2/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
121	PD5/D5[A5/D5]/MTIC5W/POE2#/SSLC1/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/AN102
122	PD4/D4[A4/D4]/POE3#/SSLC0/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/AN103
123	PD3/D3[A3/D3]/TIOCB8/TCLKH/POE8#/RSPCKC/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
124	PD2/D2[A2/D2]/MTIOC4D/TIOCA8/MISOC/CRX0/IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
125	PD1/D1[A1/D1]/MTIOC4B/TIOCB7/TCLKG/MOSIC/CTX0/IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC-A/IRQ1/AN106
126	PD0/D0[A0/D0]/TIOCA7/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
127	P93/A19/CTS7#/RTS7#/SS7#/AN017	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
128	P92/A18/RXD7/SMISO7/SSCL7/AN016	P92/A18/POE4#/RXD7/SMISO7/SSCL7/IRQ10
129	P91/A17/SCK7/AN015	P91/A17/SCK7/IRQ9
130	VSS	VSS
131	P90/A16/TXD7/SMOSI7/SSDA7/AN014	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/AN108
132	VCC	VCC
133	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0
141	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0
143	AVCC0	AVCC0
144	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Valid only on products with a ROM capacity of 2 MB or 1.5 MB.

3.4 100-Pin TFLGA Package

Table 3.4 is a comparative listing of the pin functions of 100-pin TFLGA package products.

Table 3.4 Comparative Listing of 100-Pin TFLGA Package Pin Functions

100-Pin TFLGA	RX63N	RX671
A1	P05/IRQ13/DA1	P05/IRQ13
A2	VREFH	AVCC1
A3	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
A4	VREFL0	VREFL0
A5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
A6	PD0/D0[A0/D0]/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
A7	PD4/D4[A4/D4]/POE3#/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
A8	PE0/D8[A8/D8]/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
A9	PE1/D9[A9/D9]/MTIOC4C/PO18/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/ RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A10	PE2/D10[A10/D10]/MTIOC4A/PO23/RXD12/ SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/ IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
B1	EMLE	EMLE
B2	AVSS0	AVSS0
B3	AVCC0	AVCC0
B4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
B5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
B6	PD1/D1[A1/D1]/MTIOC4B/CTX0*2/IRQ1/ AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
B7	PD3/D3[A3/D3]/POE8#/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
B8	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
B9	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
B10	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/ CTS12#/RTS12#/SS12#/MISOB/ET_ERXD3/ AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
C1	VCL	VCL
C2	VREFL	AVSS1
C3	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
C4	VREFH0	VREFH0
C5	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
C6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
C7	PD2/D2[A2/D2]/MTIOC4D/CRX0*2/IRQ2/ AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
C8	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/ AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/ AN102
C9	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ RSPCKB/ET_RX_CLK/REF50CK/IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5

100-Pin TFLGA	RX63N	RX671
C10	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ PO28/SSLB0/ET_ERXD2/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
D1	XCIN	XCIN
D2	XCOUT	XCOUT
D3	MD/FINED	MD/FINED
D4	VBATT	VBATT
D5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
D6	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
D7	PE6/D14[A14/D14]/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
D8	PE7/D15[A15/D15]/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
D9	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/ET_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
D10	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/ SSLA1/ET_TX_EN/RMII_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E1	XTAL/P37	XTAL/P37
E2	VSS	VSS
E3	RES#	RES#
E4	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/ SCK6/SCK0/USB0_DPRPD/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
E5	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
E6	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/ IRQ10
E7	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA/ ET_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14
E8	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ ET_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
E9	PA5/A5/TIOCB1/PO21/RSPCKA/ ET_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
E10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
F1	EXTAL/P36	EXTAL/P36
F2	VCC	VCC
F3	P35/NMI	UPSEL/P35/NMI
F4	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/CTX0*2/ USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
F5	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
F6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE3#/SCK6/ ET_RX_ER/RMII_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ PMC0-DS/IRQ3

100-Pin TFLGA	RX63N	RX671
F7	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/ET_RX_CLK/REF50CK	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/IRQ2
F8	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/RSPCKA/ET_ERXD1/ RMII_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/IRQ12
F9	PA7/A7/TIOCB2/PO23/MISOA/ET_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
F10	VSS	VSS
G1	P33/MTIOC0D/TIOCD0/TMRI3/PO11/ POE3#/RXD6/RXD0/SMISO6/SMISO0/ SSCL6/SSCL0/CRX0*2/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
G2	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/ IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
G3	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB/ USB0_DRPD/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
G4	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/ RSPCKB-A/IRQ7/TS2
G5	BCLK/P53*1	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
G6	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
G7	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE1#/SCK9/ET_ETXD0/ RMII_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
G8	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/ET_TX_EN/RMII_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
G9	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ ET_ERXD0/RMII_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ IRQ4-DS
G10	VCC	VCC
H1	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
H2	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ USB0_DPRPD/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/ SCL2-DS/IERXD/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
H4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
H5	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/ CRX1/ET_EXOUT/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/MISOC-B/IRQ10
H6	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX1/ET_LINKSTA	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/MOSIC-B/ IRQ4

100-Pin TFLGA	RX63N	RX671
H7	PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TXD8/SMOSI8/SSDA8/MISOA/ET_COL/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/SSITXD0/SMOSI010/SSDA010/TXD010/MISO0-A/IRQ14
H8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/RXD8/SMISO8/SSCL8/MOSIA/ET_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/SSILRCK0/SMISO010/SSCL010/RXD010/MOSI0-A/IRQ13/TS13
H9	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET_ETXD1/RMII_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SMISO011/SSCL011/RXD011/IRQ6
H10	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET_CRS/RMII_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/IRQ15
J1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SDHI_WP/IRQ12/TS5
J2	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/IRQ9/TS8
J3	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/IRQ7/ADTRG1#
J4	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/SDAHS0[FM+/HS]/IRQ3/ADTRG1#
J5	VSS_USB	VSS_USB
J6	VCC_USB	VCC_USB
J7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A/IRQ0
J8	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/AUDIO_CLK/SS010#/CTS010#/RTS010#/DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/TSCAP
J9	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1/ET_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/SSCL011/SSL01-A/IRQ14/TS16
J10	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2/ET_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15
K1	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/USB0_DPUPE	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
K2	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_DRPD	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/IRQ15/TS7

100-Pin TFLGA	RX63N	RX671
K3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
K4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
K5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
K6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
K8	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/SCK8/RSPCKA/ET_ETXD2	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
K9	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD/ET_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
K10	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD/ET_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Valid only on products with a ROM capacity of 768 KB or more.

3.5 100-Pin LQFP/100-Pin LFQFP Package

Table 3.5 is a comparative listing of the pin functions of 100-pin LQFP/100-pin LFQFP package products.

Table 3.5 Comparative Listing of 100-Pin LQFP/100-Pin LFQFP Package Pin Functions

100-Pin	RX63N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
1	VREFH	AVCC1
2	EMLE	EMLE
3	VREFL	AVSS1
4	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
5	VCL	VCL
6	VBATT	VBATT
7	MD/FINED	MD/FINED
8	XCIN	XCIN
9	XCOUT	XCOUT
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	P35/NMI	UPSEL/P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/ SCK6/SCK0/USB0_DPRPD/IRQ4	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
17	P33/MTIOC0D/TIOCD0/TMRI3/PO11/ POE3#/RXD6/RXD0/SMISO6/SMISO0/ SSCL6/SSCL0/CRX0*2/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/CTX0*2/ USB0_VBUSEN/ IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0/USB0_DPUPE/ IRQ1-DS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB/ USB0_DRPD/IRQ0-DS	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
21	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A/IRQ7/TS2
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
23	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ USB0_DPRPD/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
24	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
25	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/USB0_DPUPE	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6

100-Pin	RX63N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
26	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_DRPD	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
27	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/ SMISO0/SSCL0/USB0_EXICEN/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/USB0_ID/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
29	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ ADTRG#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/ SCL2-DS/IERXD/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
34	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
37	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
38	VSS_USB	VSS_USB
39	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/ CRX1/ET_EXOUT/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/MISOC-B/IRQ10
40	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX1/ET_LINKSTA	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/MOSIC-B/ IRQ4
41	BCLK/P53*1	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
45	PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TXD8/SMOSI8/SSDA8/MISOA/ ET_COL/IRQ14	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ MISOA-A/SSITXD0/SMOSI010/SSDA010/ TXD010/MISO0-A/IRQ14

100-Pin	RX63N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ PO30/RXD8/SMISO8/SSCL8/MOSIA/ ET_ETXD3/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/SCK8/RSPCKA/ET_ETXD2	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SSLA0/ET_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/ IRQ12/ TSCAP
49	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD/ET_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
50	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD/ET_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
51	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2/ET_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
52	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1/ET_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
53	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/ET_CRS/RMII_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
54	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/ET_ETXD1/RMII_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE1#/SCK9/ET_ETXD0/ RMII_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
56	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/ET_TX_EN/RMII_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE3#/SCK6/ ET_RX_ER/RMII_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ PMC0-DS/IRQ3
58	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/ET_RX_CLK/REF50CK	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/IRQ2
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ ET_ERXD0/RMII_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ IRQ4-DS
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/RSPCKA/ET_ERXD1/ RMII_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/IRQ12
62	VSS	VSS
63	PA7/A7/TIOCB2/PO23/MISOA/ET_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7

100-Pin	RX63N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA/ ET_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/ IRQ14
65	PA5/A5/TIOCB1/PO21/RSPCKA/ ET_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ ET_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ ET_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
68	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/IRQ10
69	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/ET_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
70	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/ SSLA1/ET_TX_EN/RMII_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
71	PE7/D15[A15/D15]/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
72	PE6/D14[A14/D14]/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ RSPCKB/ET_RX_CLK/REF50CK/IRQ5/AN3	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ PO28/SSLB0/ET_ERXD2/AN2	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
75	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/ CTS12#/RTS12#/SS12#/MISOB/ET_ERXD3/ AN1	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
76	PE2/D10[A10/D10]/MTIOC4A/PO23/RXD12/ SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/ IRQ7-DS/AN0	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
77	PE1/D9[A9/D9]/MTIOC4C/PO18/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/ RSPCKB/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
78	PE0/D8[A8/D8]/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/SSLB1-B/IRQ8/ANEX0
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
80	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
81	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/ AN013	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/ SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/ AN102
82	PD4/D4[A4/D4]/POE3#/IRQ4/AN012	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103

100-Pin	RX63N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
83	PD3/D3[A3/D3]/POE8#/IRQ3/AN011	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/ AN104
84	PD2/D2[A2/D2]/MTIOC4D/CRX*2/IRQ2/ AN010	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
85	PD1/D1[A1/D1]/MTIOC4B/CTX0*2/IRQ1/ AN009	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
86	PD0/D0[A0/D0]/IRQ0/AN008	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
87	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0
95	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05/IRQ13

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.
2. Valid only on products with a ROM capacity of 768 KB or more.

3.6 64-Pin TFLGA/64-Pin TFBGA Package

Table 3.6 is a comparative listing of the pin functions of 64-pin TFLGA/64-pin TFBGA package products.

Table 3.6 Comparative Listing of 64-Pin TFLGA/64-Pin TFBGA Package Pin Functions

64-Pin	RX631 (64-Pin TFLGA)	RX671 (64-Pin TFBGA)
A1	P05/IRQ13/DA1	AVCC1
A2	AVCC0	AVSS0
A3	VREFH0	VREFH0
A4	VREFL0	VREFL0
A5	VREFH	PD2/MTIOC4D/TIC2/SDHI_D2-B/QIO2-B/IRQ2/AN105
A6	VREFL	PD7/MTIC5U/POE0#/SDHI_D1-B/QIO1-B/IRQ7/AN100
A7	PE2/MTIOC4A/PO23/RXD12/SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/AN010	PE0/MTIOC3D/SCK12/SSLB1-B/IRQ8/ANEX0
A8	PE3/MTIOC4B/PO26/POE8#/CTS12#/RTS12#/SS12#/MISOB/AN011	PE2/MTIOC4A/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/IRQ7-DS
B1	VCL	EMLE
B2	AVSS0	AVSS1
B3	P40/IRQ8-DS/AN000	AVCC0
B4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
B5	P44/IRQ12-DS/AN004	PD3/MTIOC8D/POE8#/TOC2/SDHI_D3-B/QIO3-B/IRQ3/AN104
B6	P46/IRQ14-DS/AN006	PD6/MTIC5V/MTIOC8A/POE4#/SDHI_D0-B/QIO0-B/IRQ6/AN101
B7	PE1/MTIOC4C/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/AN009	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
B8	PE4/MTIOC4D/MTIOC1A/PO28/SSLB0/AN012	PE6/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/QIO0-B/IRQ6
C1	XCIN	VCL
C2	MD/FINED	VBATT
C3	EMLE	MD/FINED
C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
C5	P43/IRQ11-DS/AN003	PD4/MTIOC8B/POE11#/SDHI_CMD-B/QSSL-B/IRQ4/AN103
C6	PE0/SCK12/SSLB1/AN008	PD5/MTIC5W/MTIOC8C/POE10#/SDHI_CLK-B/QSPCLK-B/IRQ5/AN102
C7	PE5/MTIOC4C/MTIOC2B/RSPCKB/IRQ5/AN013	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/SCK5/SSLA2-B/SSL02-B/SCK12/ SDHI_CD/IRQ11
C8	PA0/MTIOC4A/TIOCA0/PO16/SSLA1	PE7/MTIOC6A/TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/QIO1-B/IRQ7
D1	XCOUT	XCIN
D2	RES#	XCOUT
D3	TCK/FINEC/P27/MTIOC2B/TMCI3/SCK1/RSPCKB	RES#
D4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/CTS1#/RTS1#/SS1#/CTX1/USB0_DPUPE/USB0_OVRCURA/IRQ4	P40/IRQ8-DS/AN000
D5	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	P43/IRQ11-DS/AN003

64-Pin	RX631 (64-Pin TFLGA)	RX671 (64-Pin TFBGA)
D6	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ IRQ5-DS	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ MOSI0-B/CTS12#/RTS12#/SS12#/IRQ14
D7	PA1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/SCL2/IRQ11	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/ SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/ RXDX12/SDHI_WP/IRQ10
D8	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/SDA2/ IRQ6-DS	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0-B/SSL00-B/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ IRQ5-DS
E1	VSS	XTAL/P37
E2	VBATT	VSS
E3	TDI/P30/MTIOC4B/TMRI3/POE8#/RTCIC0/ RXD1/SMISO1/SSCL1/MISOB/ USB0_DRPD/IRQ0-DS	TRST#/P34/MTIOC0A/TMCI3/POE10#/ IRQ4/TS0
E4	TMS/P16/MTIOC3C/MTIOC3D/TIOCB1/ TCLKC/TMO2/RTCOUT/TXD1/SMOSI1/ SSDA1/MOSIA/SCL2-DS/IERXD/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P13/MTIOC0B/TIOCA5/TMO3/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
E5	PC4/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/SCK5/SSLA0/USB0_DPRPD	BSCANP
E6	VCC	PA7/TIOCB2/MISOA-B/MISO0-B/IRQ7
E7	VSS	VCC
E8	PB0/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/RSPCKA/IRQ12	VSS
F1	VCC	EXTAL/P36
F2	P35/NMI	VCC
F3	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0/USB0_DPUPE/ IRQ1-DS	UPSEL/P35/NMI
F4	PC5/MTIOC3B/MTCLKD/TMRI2/PO29/ RSPCKA/USB0_ID	P12/TMCI1/MTIC5U/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
F5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/RXD1/SMISO1/SSCL1/CRX1-DS/ USB1_DPUPE/IRQ5	P53/SSIRXD0/PMC0-DS/IRQ3/TS12
F6	PB1/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB7/MTIOC3B/TIOCB5/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
F7	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE1#/SCK9	PB6/MTIOC3D/TIOCA5/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
F8	PB3/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE3#/SCK6	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ POE4#/SCK9/SCK11/SCK011/IRQ13
G1	EXTAL/P36	TCK/P27/MTIOC2B/TMCI3/SCK1/ RSPCKB-A/IRQ7/TS2
G2	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/MOSIB/USB0_VBUSEN	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS/TAMPI1
G3	VCC_USB	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS/ TAMPI0
G4	VSS_USB	VCC_USB
G5	VCC_USB	VSS_USB

64-Pin	RX631 (64-Pin TFLGA)	RX671 (64-Pin TFBGA)
G6	PC6/MTIOC3C/MTCLKA/TMCI2/PO30/ MOSIA/USB0_EXICEN/IRQ13	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/ CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/ SSDA10/TXD10/MISOA-A/SSITXD0/ SMOSI010/SSDA010/TXD010/MISO0-A/ IRQ14
G7	PC3/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/SDA2/IETXD	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ SCK10/RSPCKA-A/SSIBCK0/SCK010/ RSPCK0-A/ IRQ5/TS14
G8	PB6/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9	PC0/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/ SSLA1-A/RXD011/SMISO011/SSCL011/ SSL01-A/IRQ14/TS16
H1	XTAL/P37	TDO/P26/MTIOC2A/TMO1/TXD1/CTS3#/ RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A/ IRQ6/TS3
H2	TRST#/P17/MTIOC3A/MTIOC3B/TIOCB0/ TCLKD/TMO1/POE8#/SCK1/MISOA/ SDA2-DS/IETXD/USB1_VBUS/IRQ7	P17/MTIOC3A/MTIOC3B/MTIOC4B/ TIOCB0/TCLKD/TMO1/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
H3	USB0_DM	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/IRQ6/ADTRG0#
H4	USB0_DP	PH2/TMRI0/USB0_DM/IRQ1
H5	USB1_DM	PH1/TMO0/USB0_DP/IRQ0
H6	USB1_DP	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ MOSIA-A/SMISO010/SSCL010/RXD010/ MOSI0-A/SSILRCK0/IRQ13/TS13
H7	PC2/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/SCL2/IERXD	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/ RTS10#/SSLA0-A/AUDIO_CLK/SS010#/ CTS010#/RTS010#/DE010/SSL00-A/ SDHI_D1-A/QIO1-A/IRQ12/TSCAP
H8	PB7/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9	PC1/MTIOC3A/TCLKD/SCK5/SSLA2-A/ TXD011/SMOSI011/SSDA011/TXDA011/ SSL02-A/IRQ12/TS15

3.7 64-Pin LQFP/64-Pin LFQFP Package

Table 3.7 is a comparative listing of the pin functions of 64-pin LQFP/64-pin LFQFP package products.

Table 3.7 Comparative Listing of 64-Pin LQFP/64-Pin LFQFP Package Pin Functions

64-Pin	RX631 (64-Pin LQFP)	RX671 (64-Pin LFQFP)
1	EMLE	AVCC1
2	VCL	EMLE
3	MD/FINED	AVSS1
4	XCIN	VCL
5	XCOUT	VBATT
6	RES#	MD/FINED
7	XTAL/P37	XCIN
8	VSS	XCOUT
9	EXTAL/P36	RES#
10	VCC	XTAL/P37
11	P35/NMI	VSS
12	VBATT	EXTAL/P36
13	P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0/USB0_DPUPE/ IRQ1-DS	VCC
14	TDI/P30/MTIOC4B/TMRI3/PO8/POE8#/ RTCIC0/RXD1/SMISO1/SSCL1/MISOB/ USB0_DRPD/IRQ0-DS	UPSEL/P35/NMI
15	TCK/FINEC/P27/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB	TRST#/P34/MTIOC0A/TMCI3/POE10#/ IRQ4/TS0
16	TDO/P26/MTIOC2A/TMO1/PO6/TXD1/ SMOSI1/SSDA1/MOSIB/USB0_VBUSEN	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS/ TAMPI0
17	TRST#/P17/MTIOC3A/MTIOC3B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/MISOA/ SDA2-DS/IETXD/IRQ7	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS/TAMPI1
18	TMS/P16/MTIOC3C/MTIOC3D/TIOCB1/ TCLKC/TMO2/PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/MOSIA/SCL2-DS/IERXD/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	TDO/P26/MTIOC2A/TMO1/TXD1/CTS3#/ RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A/ IRQ6/TS3
19	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/ CRX1-DS/IRQ5	TCK/P27/MTIOC2B/TMCI3/SCK1/ RSPCKB-A/IRQ7/TS2
20	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/USB0_OVRCURA/IRQ4	P17/MTIOC3A/MTIOC3B/MTIOC4B/ TIOCB0/TCLKD/TMO1/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
21	VCC_USB	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/IRQ6/ADTRG0#
22	USB0_DM	P13/MTIOC0B/TIOCA5/TMO3/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
23	USB0_DP	P12/TMCI1/MTIC5U/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
24	VSS_USB	VCC_USB

64-Pin	RX631 (64-Pin LQFP)	RX671 (64-Pin LFQFP)
25	P55/MTIOC4D/TMO3/CRX1/IRQ10	PH2/TMRI0/USB0_DM/IRQ1
26	P54/MTIOC4B/TMCI1/CTX1	PH1/TMO0/USB0_DP/IRQ0
27	PC7/MTIOC3A/MTCLKB/TMO2/PO31/TXD8/ SMOSI8/SSDA8/MISOA/IRQ14	VSS_USB
28	PC6/MTIOC3C/MTCLKA/TMCI2/PO30/ RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN/IRQ13	P53/SSIRXD0/PMC0-DS/IRQ3/TS12
29	PC5/MTIOC3B/MTCLKD/TMRI2/PO29/ SCK8/RSPCKA/USB0_ID	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/ CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/ SSDA10/TXD10/MISOA-A/SSITXD0/ SMOSI010/SSDA010/TXD010/MISO0-A/ IRQ14
30	PC4/MTIOC3D/MTCLKC/TMCI1/PO25/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ USB0_DPRPD	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ MOSIA-A/SMISO010/SSCL010/RXD010/ MOSI0-A/SSILRCK0/IRQ13/TS13
31	PC3/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/ SSDA5/IETXD	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ SCK10/RSPCKA-A/SSIBCK0/SCK010/ RSPCK0-A/IRQ5/TS14
32	PC2/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/ SSCL5/SSLA3/IERXD	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/ RTS10#/SSLA0-A/AUDIO_CLK/SS010#/ CTS010#/RTS010#/DE010/SSL00-A/ SDHI_D1-A/QIO1-A/IRQ12/TSCAP
33	PB7/PC1/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9	PC1/MTIOC3A/TCLKD/SCK5/SSLA2-A/ TXD011/SMOSI011/SSDA011/TXDA011/ SSL02-A/IRQ12/TS15
34	PB6/PC0/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9	PC0/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/ SSLA1-A/RXD011/SMISO011/SSCL011/ SSL01-A/IRQ14/TS16
35	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ PO29/POE1#/SCK9	PB7/MTIOC3B/TIOCB5/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
36	PB3/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/ TMO0/PO27/POE3#/SCK6	PB6/MTIOC3D/TIOCA5/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
37	PB1/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/ PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ POE4#/SCK9/SCK11/SCK011/IRQ13
38	VCC	VCC
39	PB0/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/ SSCL6/RSPCKA/IRQ12	VSS
40	VSS	PA7/TIOCB2/MISOA-B/MISO0-B/IRQ7
41	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ MOSI0-B/CTS12#/RTS12#/SS12#/IRQ14
42	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ IRQ5-DS	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0-B/SSL00-B/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ IRQ5-DS
43	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/IRQ6-DS	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/ SSLA3-B/SSL03-B/RXD12/SMISO12/ SSCL12/RXDX12/SDHI_WP/IRQ10

64-Pin	RX631 (64-Pin LQFP)	RX671 (64-Pin LFQFP)
44	PA1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/IRQ11	PA1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/ SCK5/SSLA2-B/SSL02-B/SCK12/SDHI_CD/ IRQ11
45	PA0/MTIOC4A/TIOCA0/PO16/SSLA1	PE7/MTIOC6A/TOC1/MISOB-B/SDHI_WP/ SDHI_D1-B/QIO1-B/IRQ7
46	PE5/MTIOC4C/MTIOC2B/RSPCKB/IRQ5/ AN013	PE6/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/ SDHI_D0-B/QIO0-B/IRQ6
47	PE4/MTIOC4D/MTIOC1A/PO28/SSLB0/ AN012	PE2/MTIOC4A/TIC3/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/IRQ7-DS
48	PE3/MTIOC4B/PO26/POE8#/CTS12#/ RTS12#/SS12#/MISOB/AN011	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2-B/IRQ9/ ANEX1
49	PE2/MTIOC4A/PO23/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/MOSIB/IRQ7-DS/ AN010	PE0/MTIOC3D/SCK12/SSLB1-B/IRQ8/ ANEX0
50	PE1/MTIOC4C/PO18/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/SSLB2/RSPCKB/ AN009	PD7/MTIC5U/POE0#/SDHI_D1-B/QIO1-B/ IRQ7/AN100
51	PE0/SCK12/SSLB1/AN008	PD6/MTIC5V/MTIOC8A/POE4#/SDHI_D0-B/ QIO0-B/IRQ6/AN101
52	VREFL	PD5/MTIC5W/MTIOC8C/POE10#/ SDHI_CLK-B/QSPCLK-B/IRQ5/AN102
53	P46/IRQ14-DS/AN006	PD4/MTIOC8B/POE11#/SDHI_CMD-B/ QSSL-B/IRQ4/AN103
54	VREFH	PD3/MTIOC8D/POE8#/TOC2/SDHI_D3-B/ QIO3-B/IRQ3/AN104
55	P44/IRQ12-DS/AN004	PD2/MTIOC4D/TIC2/SDHI_D2-B/QIO2-B/ IRQ2/AN105
56	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
57	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
58	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
59	VREFL0	VREFL0
60	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
61	VREFH0	VREFH0
62	AVCC0	AVCC0
63	P05/IRQ13/DA1	AVSS0
64	AVSS0	P05/IRQ13

4. Notes on Migration

This section provides the important information regarding differences between the RX671 Group and the RX63N Group. 4.1 Notes on Pin Design describes notes regarding the hardware and 4.2 Notes on Function Settings describes notes regarding the software.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

Connect a decoupling capacitor rated at 0.22 µF to the VCL pin of the RX671 Group for stabilization of the internal power supply.

4.1.2 Transition to Boot Mode (FINE Interface)

On the RX671 Group a transition to boot mode (FINE interface) occurs when the MD pin is low-level at the time of release from a reset and is then switched to high-level within 20 to 100 msec.

For details on operating modes, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.1.3 Main Clock Oscillator

When connecting a resonator to the EXTAL or XTAL pin of the RX671 Group, select a resonator with an oscillation frequency of 8 MHz to 24 MHz.

4.1.4 Inputting an External Clock

On the RX63N Group it was permissible, when inputting an external clock, to input on the XTAL pin the reverse phase of the clock input on the EXTAL pin. However, this is not permitted on the RX671 Group. Keep this in mind when designing systems.

4.1.5 USB External Connection Circuit

The USB external connection circuit differs on the RX63N Group and RX671 Group.

For details on external connection circuits, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2 Notes on Function Settings

Software operating on the RX63N Group are compatible with some software on the RX671 Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics are different between the Groups.

This section describes notes on software regarding settings of functions that are different between the RX671 Group and the RX63N Group.

For differences in modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware, listed in 5, Reference Documents.

4.2.1 Exception Vector Table

Addresses allocated in the vector table are fixed on the RX63N Group, but on the RX671 Group the vector addresses are relocatable using the value set in the exception table register (EXTB) as the start address.

4.2.2 Performing RAM Self-Diagnostics on Save Register Banks

On the RX671 Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

1. Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
2. Use the SAVE instruction to write data to a bank other than that written to in step 1.
3. Use the RSTR instruction to read data from the bank written to in step 1.

4.2.3 Option-Setting Memory

ID code protection and ID code protection of the on-chip debugger are located in the ROM on the RX63N Group, and in the option-setting memory on the RX671 Group. Note that setting procedures are different between the Groups.

4.2.4 Flash Access Window Setting Register (FAW)

On the RX671 Group, once the access window protect bit (FSPR) in the flash access window setting register (FAW) is written to 0, it cannot be reset to 1.

For further information, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2.5 Software Standby Mode

On the RX671 Group it is possible to select whether the main clock or sub-clock oscillator operates or is stopped in software standby mode. To stop the main clock oscillator, clear the main clock oscillator forced oscillation (MOFXIN) bit in the main clock oscillator forced oscillation control register (MOFCR) to 0.

4.2.6 PLL Circuit

On the RX63N Group the multiplication factor setting range of the PLL circuit is 8× to 50×, but on the RX671 Group it is 10× to 30× (in 0.5× increments). When using the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value. Also, on the RX671 Group use a program to switch the PLL clock.

4.2.7 Operation of Main Clock Oscillation Stop Detection Function

The oscillation stop detection function detects when the operation of the main clock oscillator stops and supplies a LOCO clock using the output of the low-speed on-chip oscillator as the clock source for the system clock, instead of the main clock or PLL clock.

Note that on the RX671 Group, when the HOCO clock is selected as the PLL clock source and the PLL clock is selected as the system clock source, the system clock does not switch to the LOCO clock even if main clock oscillation stop is detected.

4.2.8 MOSCWTCR Register

On the RX63N Group this register counts cycles of the main clock, but on the RX671 Group it counts cycles of the LOCO clock.

4.2.9 Note on RX671 Group 48-Pin Package Products

It is not possible to use the sub-clock and RTC on 48-pin package product versions of the RX671 Group. The sub-clock control circuit is in an unstable state after a cold start, so make sure to set any undefined bits following a cold start.

For further information, refer to the User's Manual: Hardware, listed in 5, Reference Documents.

4.2.10 Inrush Current to VBATT Pin

On the RX671 Group, if the VCC voltage exceeds VBATT + 0.6 V when operating in battery backup mode, current flows from the VCC pin to the VBATT pin via a parasitic diode in the power switch on the VCC side. If this presents a problem, insert a low-dropout diode between the backup power supply and the VBATT pin.

4.2.11 Software Configurable Interrupts

A software configurable interrupt function has been added to the RX671 Group. An interrupt source assigned to each interrupt vector number from 128 to 255 can be selected from multiple sources.

For details on software configurable interrupts, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2.12 Watchdog Timer and Independent Watchdog Timer

On the RX671 Group it is possible to select either maskable or non-maskable as the type of the WDT underflow and refresh error interrupts and the IWDT underflow and refresh error interrupts.

4.2.13 Initialization of Port Direction Register (PDR)

The method of initializing the PDR differs between the RX63N Group and RX671 Group, even on products with the same pin count.

4.2.14 DMAC Activation by the MTU

On the RX671 Group, if the DMAC is activated by the MTU, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may lead to a wait before the DMA transfer starts, even though the activation source has been cleared.

4.2.15 MTIOC Pin Output Level When Counter Stops

During operation with the MTIOC pin set to output, writing 0 to a CSTn bit in TSTRA, TSTRB, or TSTR causes the corresponding counter to stop. At this point, in complementary PWM mode or reset-synchronized PWM mode on the RX671 Group, the output on the MTIOC pin is at the initial output level set in the TOCR1A or TOCR2A register.

In other than complementary PWM mode or reset-synchronized PWM mode, the output compare output level of the MTIOC pin is maintained.

4.2.16 A/D Conversion Start Requests in Complementary PWM Mode

To generate PWM waveforms in complementary PWM mode, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs.

When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA or MTU4.TADCORB (MTU7.TADCORA or MTU7.TADCORB) as the A/D conversion start request.

4.2.17 Note on Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX671 Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.18 High-Impedance Control of Unselected MTU Pins

On the RX671 Group, when high-impedance control is enabled for MTU pins in the POECR1 or POECR2 register and the control conditions are met, output on the pins multiplexed with the MTU function enters the high-impedance state regardless of whether or not the MTU function is selected.

To prevent pin output from entering the high-impedance state unexpectedly, make settings such that the MTU pins selected in the PmnPFS register of the MPC and the MTU pins selected in the pin selection register of the POE3 match.

4.2.19 Eliminating I^2C Bus Interface Noise

The RX63N Group has integrated analog noise filters on the SCL and SDA lines, but the RX671 Group has no integrated analog noise filters.

4.2.20 Restrictions on Comparison Function

On the RX671 Group the comparison function of the 12-bit A/D converter has the following restrictions:

1. Use of the self-diagnostic function and double-trigger mode are prohibited.
2. When temperature sensor or internal reference voltage is selected for window A, operation of window B is prohibited.
3. When temperature sensor or internal reference voltage is selected for window B, operation of window A is prohibited.
4. The same channel cannot be set for both window A and window B.
5. It is necessary to make settings such that high-side reference value ≥ low-side reference value.

4.2.21 Changing Option-Setting Memory by Self-Programming

Making changes to the option-setting memory by self-programming on the RX671 Group is accomplished by programming the configuration setting area in the option-setting memory using the configuration setting command.

For details on the configuration setting command, refer to RX671 Group Flash Memory User's Manual: Hardware Interface, listed in 5, Reference Documents.

4.2.22 Setting Number of Flash Memory Access Wait States

On the RX671 Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

Table 4.1 lists the number of flash memory access wait states, according to ICLK frequency.

Table 4.1 Flash Memory Access Wait States by ICLK Frequency

	ICLK ≤ 60 MHz	**60 MHz < ICLK ≤ 120 MHz**
Wait states	0 or 1	1

For details on register settings and specifications, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2.23 User Boot Mode

UB code A, UB code B, and user boot mode are implemented on the RX63N Group but not on the RX671 Group.

When using the startup program protection function on the RX671 Group, it is possible to use any interface to program and erase the user area in flash memory as an alternative to user boot mode. For details, refer to Startup Program Protection Function, in RX671 Group Flash Memory User's Manual: Hardware Interface, listed in 5, Reference Documents.

4.2.24 Transferring Firmware to FCU RAM

In order to use FCU commands with the RX63N Group, it is necessary first to store the FCU firmware in the FCU RAM. This step is not necessary for the RX671 Group.

4.2.25 Command Usage with Flash Memory

On the RX63N Group it is possible to program and erase the flash memory by issuing FCU commands to the FCU. On the RX671 Group the FCU can be controlled in order to program and erase the flash memory by setting FACI commands in the FACI command issuance area.

Table 4.2 is a comparison of the specifications of the FCU and FACI commands.

Table 4.2 Specification Comparison of FCU and FACI Commands

Item	FCU Command (RX63N)	FACI Command (RX671)
Command issuance area	Programming/erasure address (00E0 0000h to 00FF FFFFh)	FACI command issuance area (007E 0000h)
Usable commands	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2 • Lock bit programming • Blank checking	• Programming • Block erase • Multi-block erase • P/E suspend • P/E resume • Status clear • Forced end • Blank checking • Configuration settings

4.2.26 ROM Cache

The RX671 Group has the ROM cache, and ROM cache operation is disabled after a reset is released.

To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

4.2.27 Notes on Sub-Clock Oscillator

On the RX671 Group set the SOSCCR.SOSTP bit to 1 (stopping the sub-clock oscillator) within two seconds after release from the reset state.

For details on register settings and specifications, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX63N Group, RX631 Group User's Manual: Hardware, Rev. 1.80 (R01UH0041EJ0180)
(The latest version can be downloaded from the Renesas Electronics website.)

RX671 Group User's Manual: Hardware, Rev. 1.10 (R01UH0899EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

RX Family Design Guide for Migration between RX Family Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A147B/E
- TN-RX*-A167A/E
- TN-RX*-A177A/E
- TN-RX*-A186A/E
- TN-RX*-A193A/E
- TN-RX*-A0226A/E
- TN-RX*-A0224B/E
- TN-RX*-A0257A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May 20, 2021	—	First edition issued
1.10	May. 20, 2022	164	*Revised:* Table **2.93** Packages
		205	*Added:* 4.2.27 Notes on Sub-Clock Oscillator

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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