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Renesas Electronics Corporation

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H8/300L SLP Series

Demonstrating the Watchdog Timer

Introduction

Watchdog operation is performed using the watchdog timer function. The overflow period of Timer Counter W is 393.216 ms. By turning on the switch connected to the IRQ0 input pin, Timer Counter W overflows, and a watchdog operation is performed.

Target Device

H8/38024

Contents

1. Specifications

1. Watchdog operation is performed using the watchdog timer function.
2. The overflow period of Timer Counter W is set to 393.216 ms and an internal reset signal is generated unless Timer Counter W is initialized within 393.216 ms.
3. In normal operation, settings are made so that the LED repeats turning on and off at a certain time interval and that Timer Counter W is initialized before it overflows.
4. By turning on the switch connected to the $\overline{\text{IRQ0}}$ input pin, Timer Counter W is not initialized but overflows, and an internal reset signal is generated.
5. The LED is connected to the P92 output pin of Port 9.
6. The P92 pin is a high-current port.
7. Figure 1.1 shows an example of connecting a switch to the $\overline{\text{IRQ0}}$ input pin.

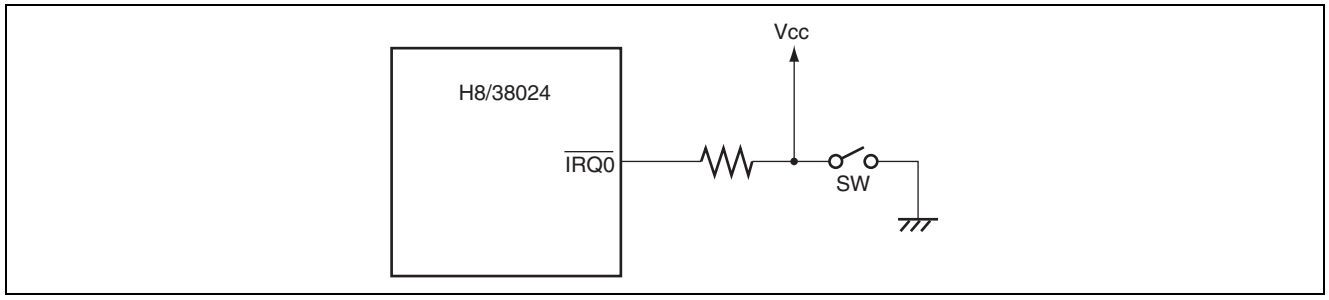


Figure 1.1 Example of Connecting Switch to $\overline{\text{IRQ0}}$ Input Pin

2. Description of Functions

1. In this task example, watchdog operation is performed using the watchdog timer function.
   A. Figure 2.1 shows the block diagram of the watchdog timer function which is described below.
      - The system clock (ϕ) is a 5 MHz clock and a reference clock to operate the CPU and its peripheral functions.
      - Prescaler S (PSS) is a 13-bit counter using ϕ as its input clock and is counted up every cycle.
      - The Timer Counter W (TCW) is an 8-bit read/write up counter and is counted up by an internal clock which is input. The clock input is ϕ/8192.
      - The Timer Control/Status Register W (TCSRW) is an 8-bit read/write register and controls TCSRW and TCW writing, controls watchdog timer operation, and indicates operation status.
      - The calculation method of the TCW overflow period in this task example is shown below.

$$\text{TCW overflow period} = \frac{1}{\text{System clock} / 8192} \times (256 - (\text{TCW reload value}))$$
$$= 1.638\ \text{ms} \times (256 - 16)$$
$$= 393.216\ \text{ms}$$

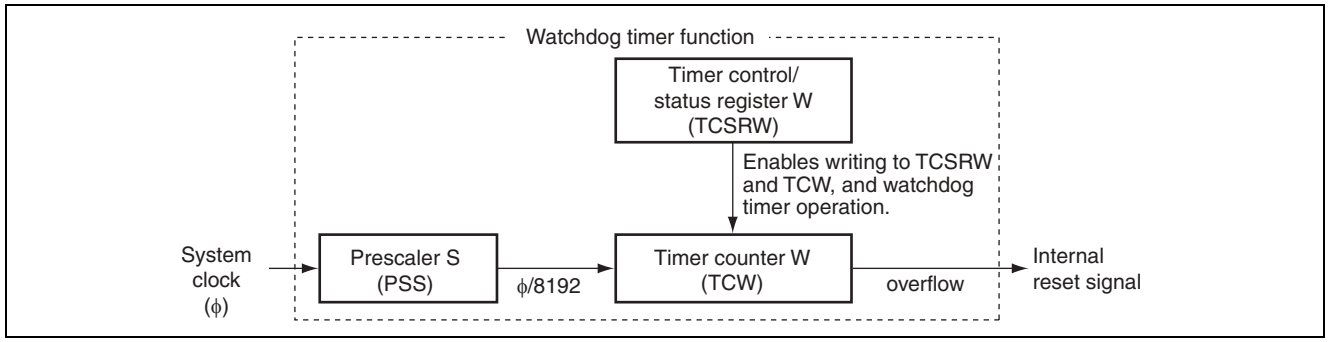


Figure 2.1 Block Diagram of Watchdog Timer Functions

2. Table 2.1 shows the assignment of functions in this task example. The functions are assigned as shown in table 2.1 to perform watchdog operation by the watchdog timer function.

Table 2.1 Assignment of Functions

Function	Assignment
PSS	A 13-bit counter which uses the system clock as input
TCSRW	Controls TCSRW and TCW writing, controls watchdog timer operation, and indicates operation status.
TCW	An 8-bit counter which uses a clock obtained by dividing the system clock by 8192 as input
WDCKS	Selects the system clock/8192 for the clock source of the watchdog timer.
IEG0	Selects the interrupt edges of $\overline{\text{IRQ0}}$ pin.
IEN0	Enables IRQ0 interrupts of SW ($\overline{\text{IRQ0}}$ pin).
IRRI0	Judges ON/OFF of SW ($\overline{\text{IRQ0}}$ pin).
IRQ0	Input pin of SW input
P92	LED output

3. Principle of Operation

1. Figure 3.1 illustrates the principle of operation of this sample task. As shown in figure 3.1, watchdog operation is performed by the watchdog timer function by means of hardware processing and software processing.

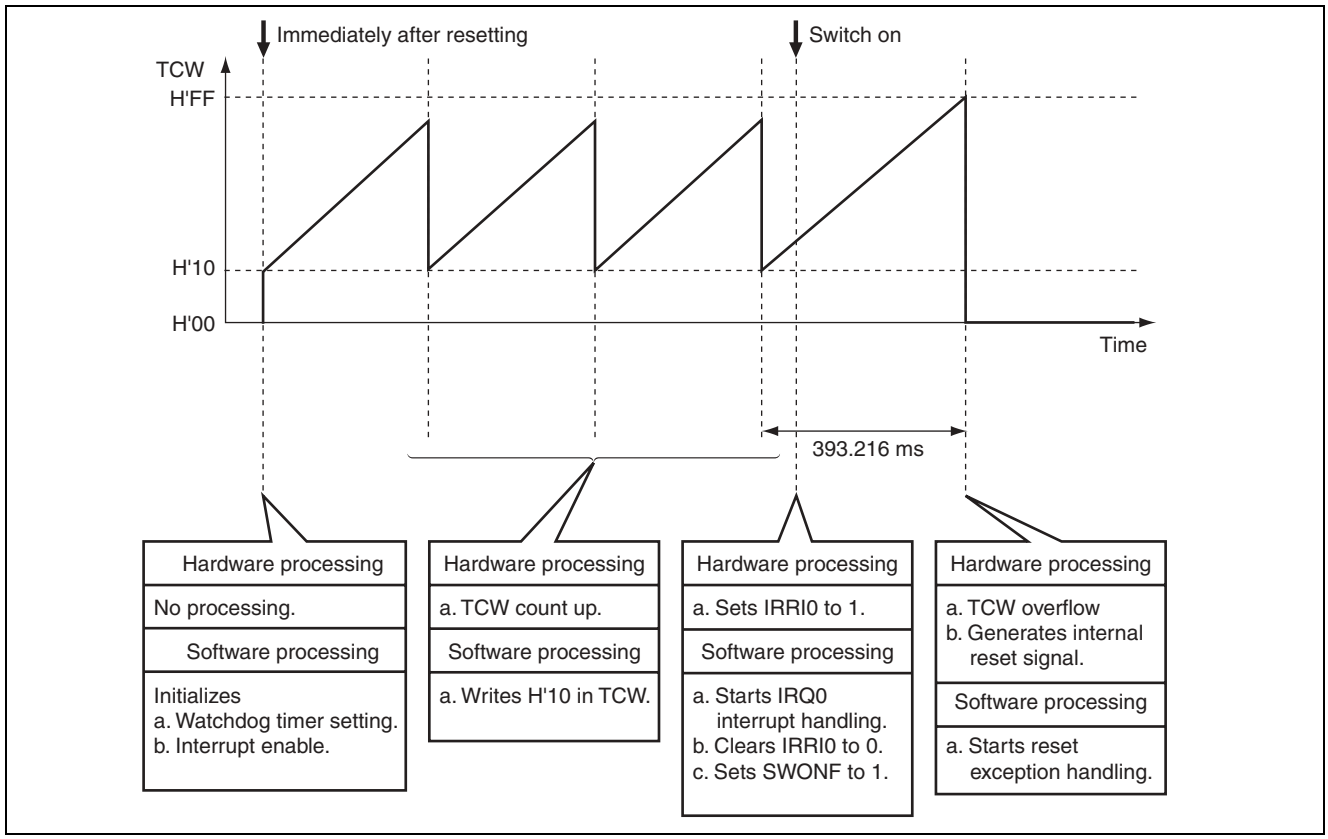


Figure 3.1 Operation Principle of Watchdog Operation by Watchdog Timer Function

4. Description of Software

4.1 Modules

Table 4.1 describes the modules in this task example.

Table 4.1 Description of Modules

Module	Label	Function
Main Routine	main	Sets the watchdog timer function, enables interrupts, controls the LED, and judges whether or not the switch connected to $\overline{\text{IRQ0}}$ is turned on.
Switch On	irq0int	An $\overline{\text{IRQ0}}$ interrupt handling routine. Sets SWONF to 1.

4.2 Arguments

Arguments are not used in this task example.

4.3 Internal registers

Table 4.2 describes the internal registers in this task example.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
TCSRW	B6WI	Timer Control/Status Register W (Bit 6 Write Disable) If B6WI = 0, writing to bit 6 in TCSRW is enabled. If B6WI = 1, writing to bit 6 in TCSRW is disabled.	H'FFC0 Bit 7	1
	TCWE	Timer Control/Status Register W (Timer Counter W Write Enable) If TCWE = 1, writing of 8-bit data to TCW is enabled.	H'FFC0 Bit 6	1
	B4WI	Timer Control/Status Register W (Bit 4 Write Disable) If B4WI = 0, writing to bit 4 in TCSRW is enabled. If B4WI = 1, writing to bit 4 in TCSRW is disabled.	H'FFC0 Bit 5	1
	TCSRWE	Timer Control/Status Register W (Timer Control/Status Register W Write Enable) If TCSRWE = 1, writing to bits 2 and 0 in TCSRW is enabled.	H'FFC0 Bit 4	1
	B2WI	Timer Control/Status Register W (Bit 2 Write Disable) If B2WI = 0, writing to bit 2 in TCSRW is enabled. If B2WI = 1, writing to bit 2 in TCSRW is disabled.	H'FFC0 Bit 3	1
	WDON	Timer Control/Status Register W (Watchdog Timer On) If WDON = 1, watchdog timer operation is enabled.	H'FFC0 Bit 2	1
	B0WI	Timer Control/Status Register W (Bit 0 Write Disable) If B0WI = 0, writing to bit 0 in TCSRW is enabled. If B0WI = 1, writing to bit 0 in TCSRW is disabled.	H'FFC0 Bit 1	1
	WRST	Timer Control/Status Register W (Watchdog Timer Reset) If WRST = 0, TCW has not overflowed and no internal reset signal is generated. If WRST = 1, TCW has overflowed and an internal reset signal is generated.	H'FFC0 Bit 0	0

Register		Function	Address	Setting
TCW		Timer Counter W An 8-bit counter to input a clock obtained by dividing the system clock by 8192.	H'FFC1	H'10
PDR9	P92	Port Data Register 9 (Port Data Register 92) If P92 = 0, the output level of P92 pin is Low. If P92 = 1, the output level of P92 pin is High.	H'FFDC Bit 2	0
PMR2	WDCKS	Port Mode Register 2 (WatchDog Timer Source Clock) If WDCKS = 0, source clock of watchdog timer is ϕ (system clock)/8192. If WDCKS = 1, source clock of watchdog timer is ϕw (subclock) /32.	H'FFE0 Bit 2	0
	IRQ0	Port Mode Register 2 (P43/$\overline{\text{IRQ0}}$ Pin Function Switch) If $\overline{\text{IRQ0}}$ = 0, P43/$\overline{\text{IRQ0}}$ pin functions as P43 input/output pin. If $\overline{\text{IRQ0}}$ = 1, P43/$\overline{\text{IRQ0}}$ pin functions as $\overline{\text{IRQ0}}$ input pin.	H'FFE0 Bit 0	1
IEGR	IEG0	IRQ Edge Select Register (IRQ Edge Select If IEG0 = 0, the falling edge is selected as $\overline{\text{IRQ0}}$ pin input detection edge. If IEG0 = 1, the rising edge is selected as $\overline{\text{IRQ0}}$ pin input detection edge.	H'FFF2 Bit 0	0
IENR1	IEN0	Interrupt Enable Register 1 ($\overline{\text{IRQ0}}$ Interrupt Request Enable) If IEN0 = 0, interrupt requests from the $\overline{\text{IRQ0}}$ pin are disabled. If IEN0 = 1, interrupt requests from the $\overline{\text{IRQ0}}$ pin are enabled.	H'FFF3 Bit 0	1
IRR1	IRRI0	Interrupt Request Register 1 (IRQ0 Interrupt Request Flag) If IRRI0 = 0, $\overline{\text{IRQ0}}$ pin interrupt is not requested. If IRRI0 = 1, $\overline{\text{IRQ0}}$ pin interrupt is requested.	H'FFF6 Bit 0	0

4.4 Description of RAM

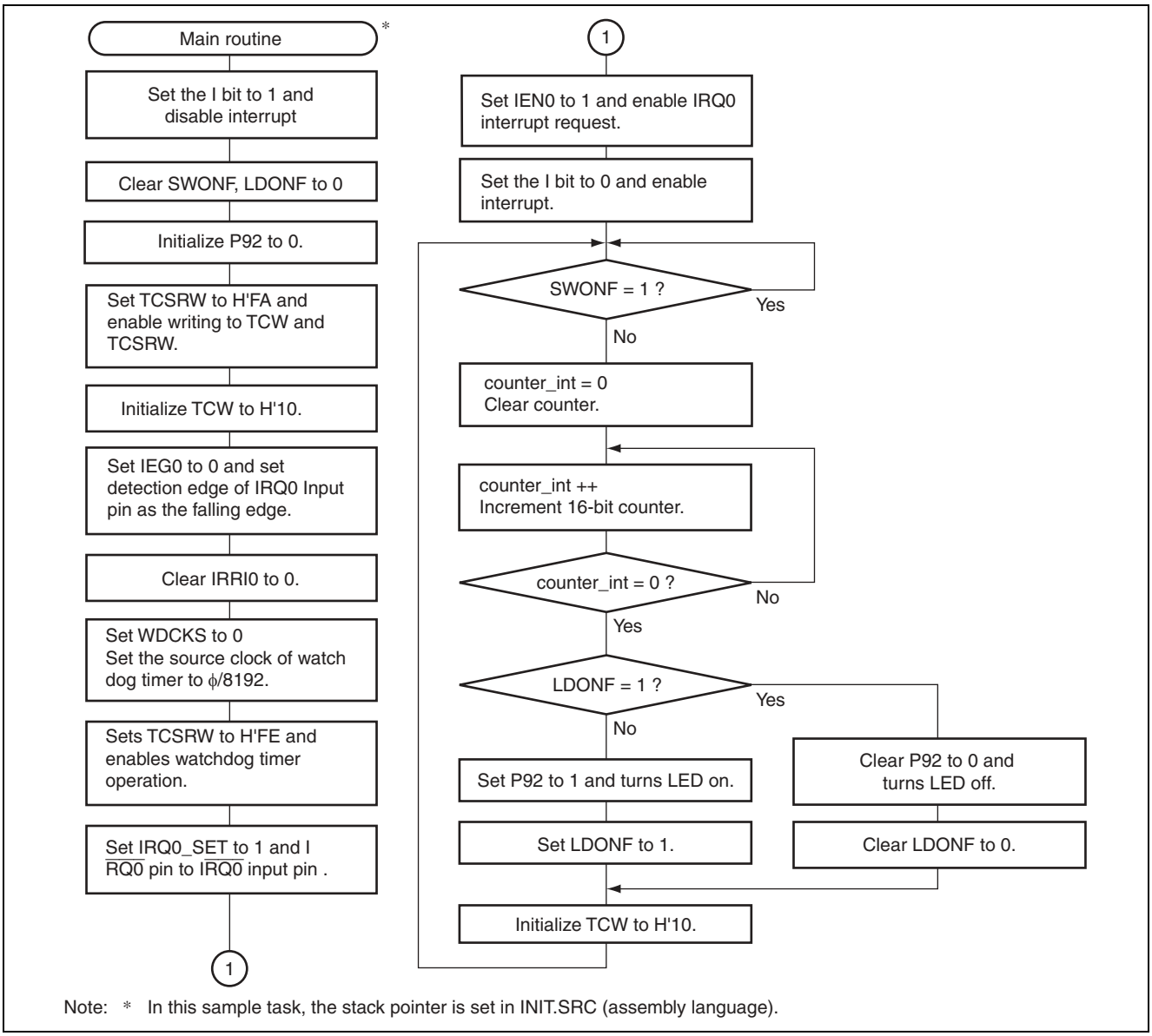
The RAMs used in this task example are described in table 4.3.

Table 4.3 Description of RAM

Label		Function	Address	Used in
counter_int		Up-counter that turns on or off the LED	H'FB80	Main Routine
USRF	SWONF	Flag to judge ON/OFF of switch input	H'FB82 Bit 0	Main Routine Switch On
	LDONF	Flag to judge ON/OFF of the LED	H'FB82 Bit 1	Main Routine

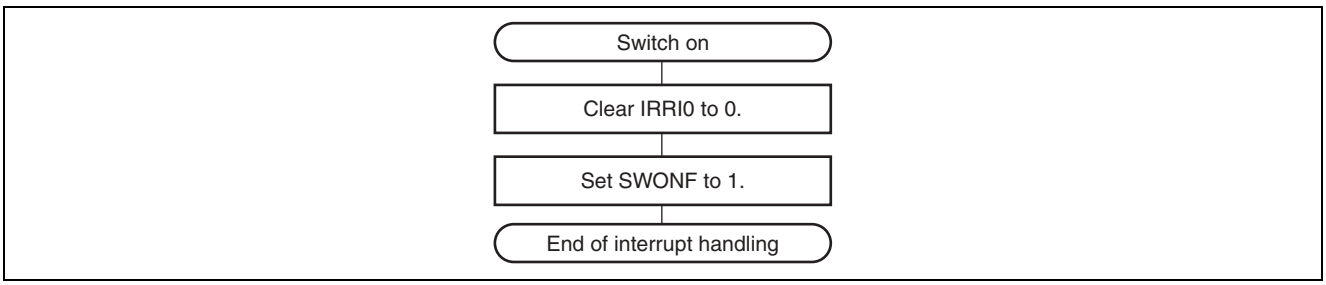
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. IRQ0 interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Watchdog Timer'                                                                                                    */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Watchdog Timer                                                                                                    */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TCSRW       *(volatile unsigned char *)0xFFB2       /* Timer Control/Status Register W          */
#define     TCSRW_BIT   (*(struct BIT *)0xFFB2)                 /* Timer Control/Status Register W          */
#define     B6WI        TCSRW_BIT.b7                            /* Bit-6 Write Disable                      */
#define     TCWE        TCSRW_BIT.b6                            /* Timer Counter W Write Enable             */
#define     B4WI        TCSRW_BIT.b5                            /* Bit-4 Write Disable                      */
#define     TCSRWE      TCSRW_BIT.b4                            /* Timer Control/Status Register W          */
                                                                /*                              Write Enable */
#define     B2WI        TCSRW_BIT.b3                            /* Bit-2 Write Disable                      */
#define     WDON        TCSRW_BIT.b2                            /* Watchdog Timer ON                        */
#define     B0WI        TCSRW_BIT.b1                            /* Bit-0 Write Disable                      */
#define     WRST        TCSRW_BIT.b0                            /* Watchdog Timer Reset                     */
```

```
#define     TCW         *(volatile unsigned char *)0xFFB3       /* Timer Counter W                          */
#define     PDR9_BIT    (*(struct BIT *)0xFFDC)                 /* Port Data Register 9                     */
#define     P92         PDR9_BIT.b2                             /* Port Data Register 9 bit2                */
#define     IEGR1_BIT   (*(struct BIT *)0xFFF2)                 /* Interrupt Edge Select Register 1         */
#define     IEG0        IEGR1_BIT.b0                            /* IEG0 Edge Select                         */
#define     IENR1_BIT   (*(struct BIT *)0xFFF3)                 /* Interrupt Enable Register 1              */
#define     IEN0        IENR1_BIT.b0                            /* IEN0 Interrupt Enable                    */
#define     IRR1_BIT    (*(struct BIT *)0xFFF6)                 /* Interrupt Request Register 1             */
#define     IRRI0       IRR1_BIT.b0                             /* IRRI0 Interrupt Request Register         */
#define     PMR2_BIT    (*(struct BIT *)0xFFC9)                 /* Port Mode Register 2                     */
#define     WDCKS       PMR2_BIT.b2                             /* Watchdog Timer Source Clock              */
#define     IRQ0        PMR2_BIT.b0                             /* P43/IRQ0 Select                          */

#pragma interrupt   (irq0int)
/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                      /* SP Set                                   */
void        main ( void );
void        irq0int ( void );

/************************************************************************************************************/
/*  RAM define                                                                                              */
/************************************************************************************************************/
unsigned int    counter_int;
unsigned char   USRF;                                           /* User Flag Area                           */

#define     USRF_BIT    (*(struct BIT *)&USRF)
#define     SWONF       USRF_BIT.b0
#define     LDONF       USRF_BIT.b1

/************************************************************************************************************/
/*  Vector Address                                                                                          */
/************************************************************************************************************/
#pragma section     V1                                          /* Vector Section Set                       */
void (*const VEC_TBL1[])(void) = {
    INIT                                                        /* 0x0000 Reset Vector                      */
};
#pragma section     V2                                          /* Vector Section Set                       */
void (*const VEC_TBL2[])(void) = {
    irq0int                                                     /* 0x0008 IRQ0 Interrupt Vector             */
};

#pragma section                                                 /* P                                        */
/************************************************************************************************************/
/*  Main Program                                                                                            */
/************************************************************************************************************/
void    main ( void )
{
    set_imask_ccr(1);                                           /* Interrupt Disable                        */

    SWONF = 0;                                                  /* Initialize SWONF                         */
    LDONF = 0;                                                  /* Initialize LDONF                         */

    P92 = 0;                                                    /* Initialize P92 Terminal Output Level     */

    TCSRW = 0x5A;                                               /* TCW And TCSRW Write Enable               */

    TCW = 0x10;                                                 /* Initialize TCW                           */
```

```
    IEG0 = 0;                                   /* Initialize IRQ0  Terminal Input Edge     */
    IRRI0 = 0;                                  /* Initialize IRQ0 Interrupt Request Flag   */
    WDCKS = 0;                                  /* Initialize IRQ0  Input Terminal          */

    TCSRW = 0xFE;                               /* Watchdog Timer On                        */

    IRQ0 = 1;
    IEN0 = 1;                                   /* IRQ0 Interrupt Enable                    */

    set_imask_ccr(0);                           /* Interrupt Enable                         */

    while(1){
        while(SWONF == 1){                      /* SWONF = 1 ?                              */
            ;
        }

        counter_int = 0;                        /* counter Clear                            */
        do{
            counter_int ++;                     /* counter Countup                          */
        }while(counter_int ! = 0);              /* counter_int = FFFF ?                     */

        if(LDONF == 1){
            P92 = 0;                            /* Turn Off LED                             */
            LDONF = 0;                          /* LDONF Clear                              */
        }else{
            P92 = 1;                            /* Turn On LED                              */
            LDONF = 1;                          /* LDONF set                                */
        }

        TCW = 0x10;                             /* Initialize TCW                           */
    }
}
/*******************************************************************************************************************/
/*  IRQ0 Interrupt                                                                                                 */
/*******************************************************************************************************************/
void    irq0int ( void )
{
    IRRI0 = 0;                                  /* Clear IRRI0                              */

    SWONF = 1;                                  /* Set SWONF                                */
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0008
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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