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M16C/65 Group

Delayed one-shot output

1. Abstract

The following are steps of outputting a pulse only once after a specified elapse since an external trigger is input.

Use the following peripheral function:

• One-shot timer mode of timer A

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Specification

After 1ms from the falling edge which inputs to TA0IN pin, TA10UT pin will output "H" for 50us.

(1) Set timer A0 in one-shot timer mode, and set timer A1 in one-shot timer mode with pulse output function.

(2) Set TA0 register to make timer A0 underflow period as 1ms. Set TA1 register to make timer A1 generate a pulse with 50us "H" interval.

Set the underflow of timer A0 as the counting start condition of timer A1.

Both timer A0 and timer A1 use fITIMAB as the count source.

(3) Connect a 20MHz oscillator to XIN.

(4) Using POFS1 bit in TAPOFS register, select the output polarity of the TA10UT pin.

4. Operation

(1) Setting the trigger select bit to "1" and setting the count start flag to "1" enables the counter of timer A0 to count.

(2) If an effective edge, selected by use of the external trigger select bit, is input to the TA0IN pin, the counter begins a down count. The counter of timer A0 performs a down count on count source f1TIMAB.

(3) As soon as the counter of timer A0 becomes "0000h", the counter reloads the content of the reload register and stops counting. At this time, the timer A0 interrupt request bit goes to "1".

(4) An underflow in timer A0 triggers the counter of timer A1 and causes it to begin counting. When timer A1 begins counting, the output level of the TA10UT pin goes to "H".

(5) As soon as the counter of timer A1 becomes "0000h", the output level of the TA10UT pin goes to "L", the counter reloads the content of the reload register, and stops counting. At this time, timer A1 interrupt request bit goes to "1".



Figure 1 shows the operation timing.

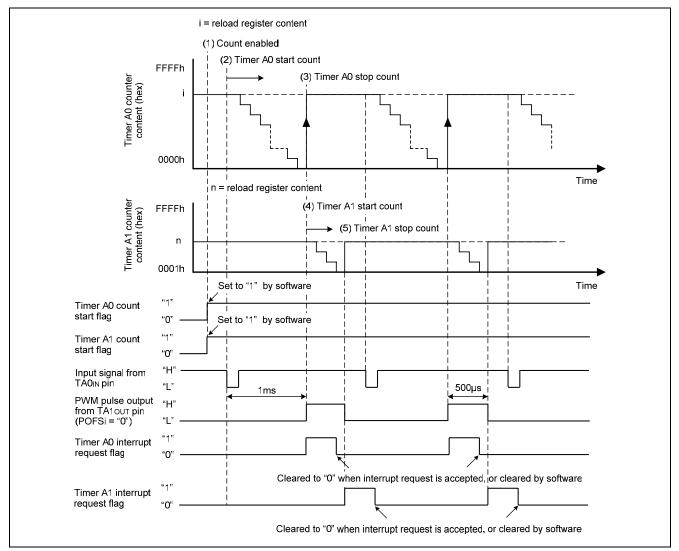


Figure 1. Operation timing of delayed one-shot output

Figure 2 shows the connection diagram.

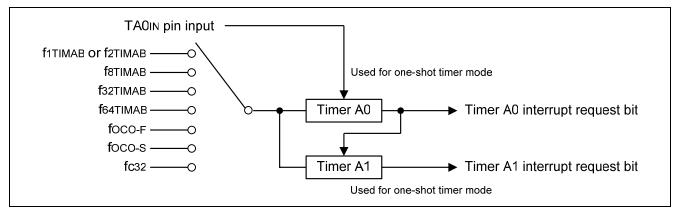


Figure 2. Connection diagram of delayed one-shot output



5. Set-up procedure

Table 1 shows Timer A count source, Figure 3 shows block diagram of Timer A count source in timer mode.

Table 1. Count Source Selection of Timer A

TCKDIVC0 register (Note 1)	TACSj	register	(Note 2)		TAiMR registe		Count source	Count source period	
TCDIV00	TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	ТСКО		f(Xin):20MHz f(Xcin):32.768kHz f(oco-F):about 20MHz f(oco-s):about 125kHz	
0	0	-	-	-	0	0	f1TIMAB/ f2TIMAB (Note 3)	50ns/100ns	
0	0	-	-	-	0	1	f8TIMAB	400ns	
0	0	-	-	-	1	0	f32TIMAB	1600ns	
0	0	-	-	-	1	1	fc32	976.56µs	
0	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	50ns/100ns	
0	1	0	0	1	-	-	f8TIMAB	400ns	
0	1	0	1	0	-	-	f32TIMAB	1600ns	
0	1	0	1	1	-	-	f64TIMAB	3200ns	
0	1	1	0	0	-	-	foco-F	about 50ns	
0	1	1	0	1	-	-	foco-s	about 8µs	
0	1	1	1	0	-	-	fC32	976.56µs	
1	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	about 50ns/100ns	
1	1	0	0	1	-	-	f8TIMAB	about 400ns	
1	1	0	1	0	-	-	f32TIMAB	about 1600ns	
1	1	0	1	1	-	-	f64TIMAB	about 3200ns	

Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection. Note 3: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.



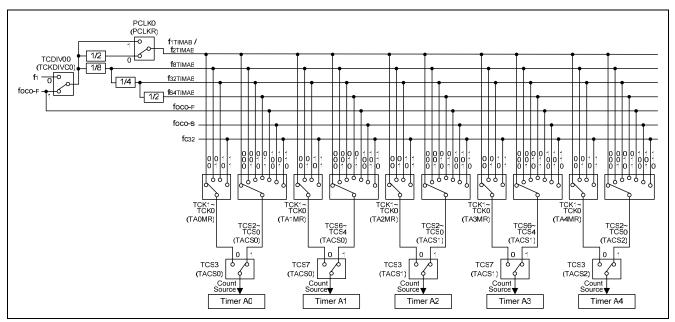
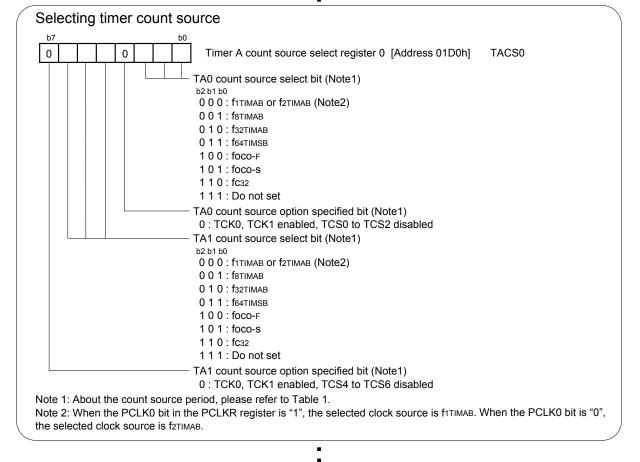


Figure 3. Count source of Timer A

							tting other registers associated with timer A. After changing the TCDIV00 bit, with timer A again.)
b7						bO	
0	0	0	0	X	0 0	2 0	Timer AB Division Control Register 0 [Address 01CBh] TCKDIVC0
							Clock select prior to timer AB division bit
							- Reserved bits
							Set to 0
							No register bits. If necessary, set to 0. Read as undefined value.
L			_				- Reserved bits Set to 0



•



Setting timer A0

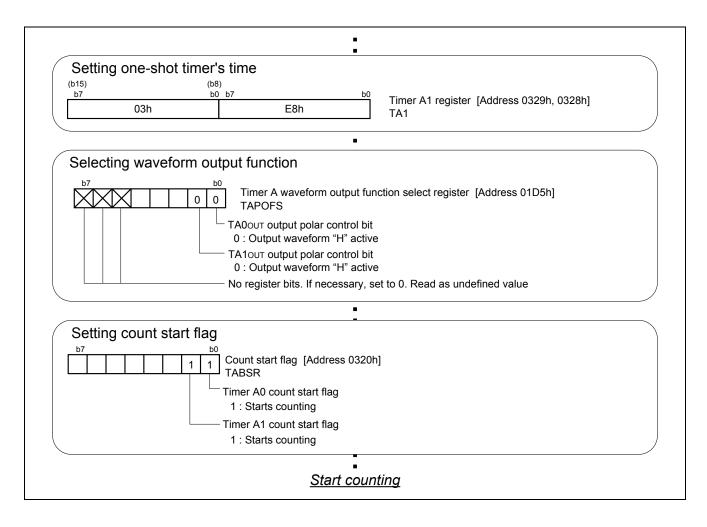
		Timer A0 mode register [Address 0336h] TA0MR
		- Selection of one-shot timer mode
		- Pulse output function select bit
		0 : Pulse is not output (TA0out pin is normal port pin)
		External trigger select bit
		0 : Falling edge of TA0ı∧ pin's input signal
		Trigger select bit 1 : Selected by event/trigger select register
		- 0 (Must always be "0" in one-shot timer mode)
		Count source select bit (Note1)
		^{b7 b6} О 0 : f1тімав or f2тімав (Note2)
		0 1 : f8тімав
		10: f32тімав
	ate 1. Valid when the TCC2 hit.	11: fc32
	ount source period, please refer	or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the to Table 1
(N		e PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0",

.



•					
Setting one-shot start flag					
(Set timer A0 to trigger timer A1)					
Dne-shot start flag [Address 0322h] ONSF					
Timer A0 event/trigger select bit ^{b7 b6} 0 0 : Input on ΤΑ0ιΝ is selected(Note)					
Note: Set the corresponding port direction register to "0"					
Satting and shot timer's time					
(Setting one-shot timer's time					
b7 b0 b7 b0 b7 b0 Timer A0 register [Address 0327h, 0326h]					
4Eh 20h TAO					
Setting timer A1					
·					
Selecting one-shot timer mode and functions					
0 0 1 0 1 1 0 Timer A1 mode register [Address 0337h] TA1MR Selection of one-shot timer mode Pulse output function select bit 1 Pulse is output (TA1out pin is pulse output pin) External trigger select bit Invalid when choosing timer's overflow Trigger select bit 1 Selected by event/trigger select register 0 (Must always be "0" in one-shot timer mode) Count source select bit (Note1) b7 b6 0 0					
0 1 : f8тімав 1 0 : f32тімав					
Note 1: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 1. Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.					
I Contraction of the second se					
Setting event/trigger select bit (Set timer A0 to trigger timer A1)					
b7 b0 Trigger select register [Address 0323h] TRGSR					
Timer A1 event/trigger select bit					
1 0 : TA0 overflow or underflow is selected					







6. Reference

Hardware manual

M16C/65 Group Hardware Manual

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