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SH7211 Group

Data Transfer to SCIF with DMAC

Introduction

This application note explains how to use the direct memory access controller (DMAC) and the serial communication interface with FIFO (SCIF), and is intended for reference to help in the design of user software.

Target Device

SH7211

Contents

1. Introduction

1.1 Specification

- Channel 0 and 1 are used for the DMAC and the SCIF, respectively.
- 32-byte character strings stored in the on-chip RAM are transferred to the transmit FIFO data register (SCFTDR) of the SCIF.
- The character strings transferred to the transmit FIFO data register (SCFTDR) are transmitted through asynchronous communications.
- The format of data to be transmitted is as follows: 8-bit data; no parity; one stop bit. The bit rate is set to 34800 bps.
- The SCIF transmit-FIFO-data-empty transfer request (on-chip peripheral module request) is used as the DMA transfer request.

1.2 Module Used

Direct memory access controller (DMAC channel 0)

Serial communication interface with FIFO (SCIF channel 1)

1.3 Applicable Conditions

• Microcontroller:	SH7211	
• Operating Frequency:	Internal clock	160 MHz
	Bus clock	40 MHz
	Peripheral clock	40 MHz
• C Compiler:	SuperH RISC engine family C/C++ compiler package Ver.9.11, from Renesas Technology	

2. Description of Sample Application

In this sample application, DMA transfer by the direct memory access controller (DMAC) transmits character string data stored in the on-chip RAM to the transmit FIFO data register of the serial communication interface with FIFO (SCIF), which then handles asynchronous communications.

2.1 Operational Overview of Used Modules

2.1.1 Direct Memory Access Controller (DMAC)

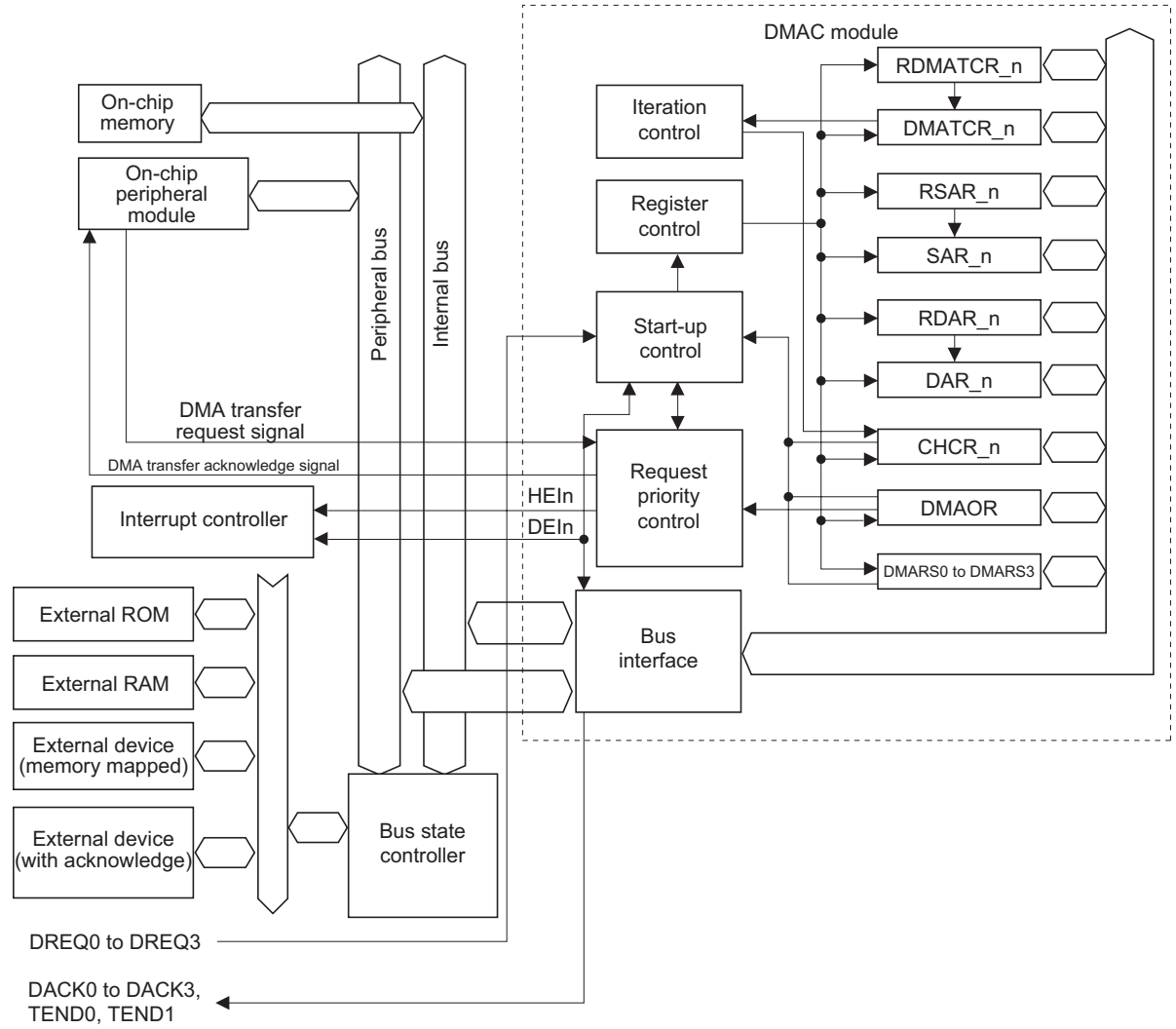
When a DMA transfer request is made, the DMAC starts to transfer data in order of priority of channels. Then, it continues the transfer operation until the transfer end condition is met. The DMAC has three transfer request modes: auto request, external request, and on-chip peripheral module request. The bus mode is selectable from burst mode and cycle stealing mode. For more details on the DMAC, refer to the section on the direct memory access controller (DMAC), in the SH7211 Group Hardware Manual.

Interrupt sources selected as sources for activating the DMAC are not input to the interrupt controller (INTC), but are masked. For details, refer to the section on the interrupt controller (INTC) in the SH7211 Group Hardware Manual.

An overview of the DMAC is provided in table 1. A block diagram of the DMAC is shown in figure 1.

Table 1 Overview of DMAC

Item	Description
Number of channels	8 (CH0 to CH7) Only 4 (CH0 to CH3) can receive external requests.
Address space	4 G bytes
Length of transfer data	Byte, word (2 bytes), longword (4 bytes), and 16 bytes (longword × 4)
Maximum transfer count	16,777,216 (24 bits) transfers
Address modes	Single address mode and dual address mode
Transfer requests	External requests, peripheral module requests, and auto requests (SCIF: 8 sources, IIC3: two sources, A/D converter: one source, MTU2: five sources, CMT: two sources)
Bus modes	Cycle stealing mode and burst mode
Priority level	Channel priority fixed mode and round-robin mode
Interrupt request	An interrupt request is issued to the CPU when half or all of a transfer process is completed.
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/transfer end signal	Active levels for DACK and TEND can be set independently



[Legend]

RDMATCR:	DMA reload transfer count register	CHCR:	DMA channel control register
DMATCR:	DMA transfer count register	DMAOR:	DMA operation register
RSAR:	DMA reload source address register	DMARS0 to DMARS3:	DMA extension resource selectors 0 to 3
SAR:	DMA source address register	HEIn:	DMA transfer half-end interrupt request to the CPU
RDAR:	DMA reload destination address register	DEIn:	DMA transfer end interrupt request to the CPU
DAR:	DMA destination address register	n:	0, 1, 2, 3, 4, 5, 6, 7

Figure 1 Block Diagram of the DMAC

2.1.2 Serial Communications Interface with FIFO (SCIF)

The SCIF supports asynchronous and synchronous communications. It incorporates 16-stage FIFO (First-In First-Out) registers, enabling fast and effective continuous communication. For details on the SCIF, refer to the section on serial communication interface with FIFO (SCIF), in the SH7211 Group Hardware Manual.

An overview of the SCIF is provided in table 2. In addition, overviews of asynchronous and synchronous serial communications are provided in tables 3 and 4, respectively.

Figure 2 shows a block diagram of the SCIF.

Table 2 Overview of SCIF

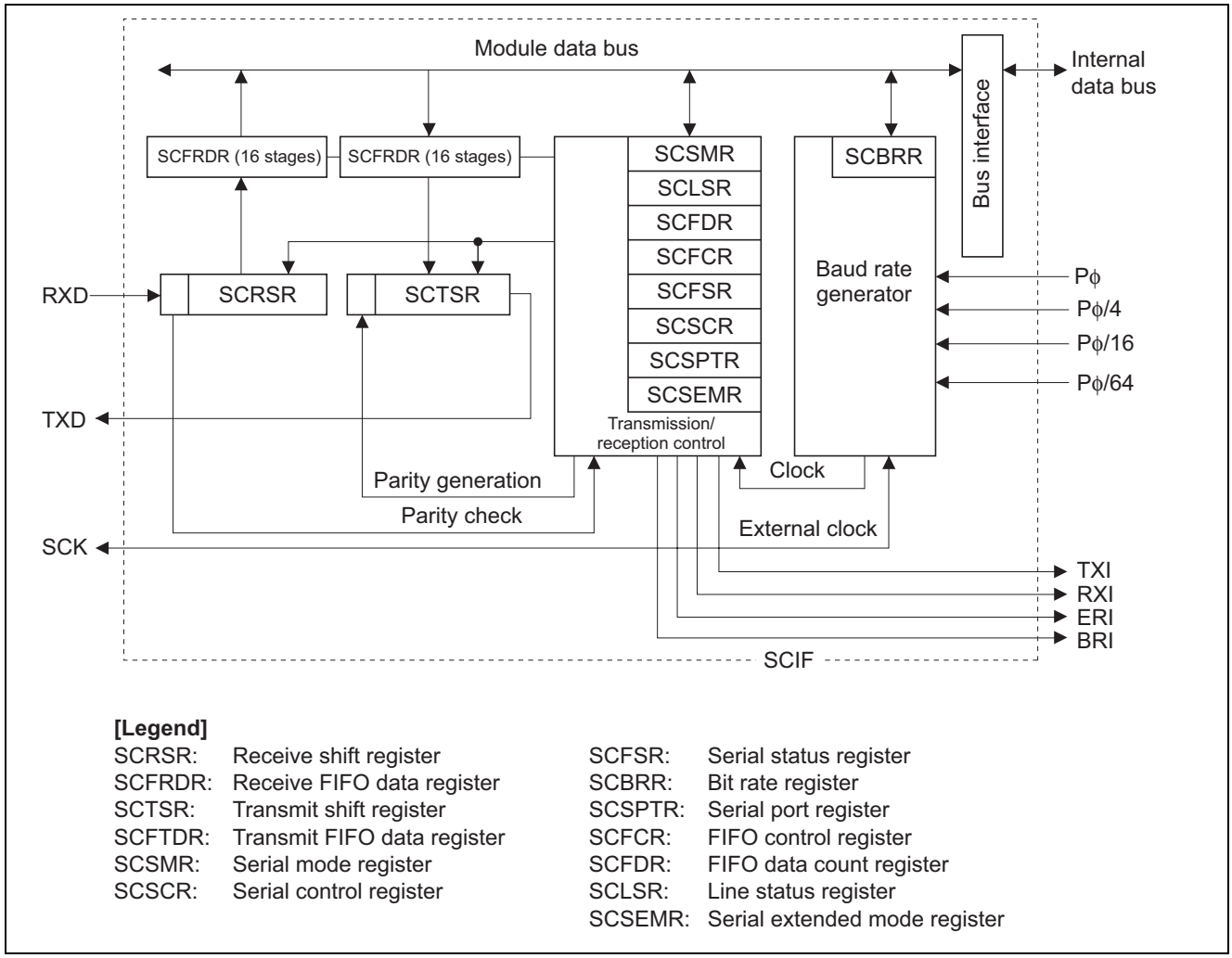
Item	Description
Communications mode	Asynchronous serial, synchronous serial Full duplex
Clock source	Baud rate generator (internal clock), or SCK pin (external clock)
Interrupt	Transmit-FIFO-data-empty interrupt, break interrupt, receive-FIFO-data-full interrupt, and receive-error interrupt
Others	Capable of operating in low power consumption mode Receive error counts detectable Timeout error detectable (in asynchronous mode)

Table 3 Overview of Asynchronous Serial Communication

Item	Description
Data length	7 or 8 bits
Stop bit length	1 or 2 bits
Parity	Even, odd parity, or no parity
Receive error detection	Parity error, framing error, and overrun error
Brake detection	A break is detected when a framing error is followed by at least one frame at the space level (0 or low level). A break can also be detected by reading the RXD level directly from the serial port register when a framing error occurs.

Table 4 Overview of Synchronous Serial Communication

Item	Description
Data length	8 bits
Receive error detection	Overrun error



[Legend]

SCRSR:	Receive shift register	SCFSR:	Serial status register
SCFRDR:	Receive FIFO data register	SCBRR:	Bit rate register
SCTSR:	Transmit shift register	SCSPTR:	Serial port register
SCFTDR:	Transmit FIFO data register	SCFCR:	FIFO control register
SCSMR:	Serial mode register	SCFDR:	FIFO data count register
SCSCR:	Serial control register	SCLSR:	Line status register
		SCSEMR:	Serial extended mode register

Figure 2 Block Diagram of SCIF

2.2 Operation of the Sample Program

In the sample program, transmit-FIFO-data-empty transfer requests from the SCIF (on-chip peripheral module requests) activate DMAC channel 0 to transfer data from the on-chip RAM to the transmit FIFO data register (SCFTDR) of SCIF channel 1. The data written to the SCFTDR of SCIF channel 1 are transmitted through asynchronous serial communications (UART mode). The settings of the DMAC and the SCIF are listed in tables 5 and 6, respectively. In addition, the timing of operations by the sample program is shown in figure 3.

Table 5 Settings of DMAC

DMA transfer condition	SCIF transmit data empty (SCIF_TXI1)
Channel	CH0
Length of transfer data	Byte
Transfer counts	32 transfers
Address mode	Dual address mode
Transfer request	On-chip module request (SCIF_TXI1)
Bus mode	Cycle stealing mode*
Priority level	Channel priority fixed mode
Interrupt request	An interrupt request to the CPU is made at the end of a data transfer
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/transfer end signal	Active levels for DACK and TEND can be set independently

Note When TXI of the SCIF is selected for the DMA transfer request source, cycle stealing mode must be used. For details, refer to the section on the DMA transfer requests in the SH7211 Group Hardware Manual.

Table 6 Settings of SCIF

Operating mode	Asynchronous
Channel	CH1
Data length	8-bits
Parity	Parity bits not added or checked
Length of stop bit	One
Clock source	Pϕ clock (40 MHz)
Transmit interrupt	Enable transmit FIFO data empty interrupts (TXI)
Error interrupt	Disabled
Transmission/reception mode	Transmission enabled
Baud rate	38400 bit/s

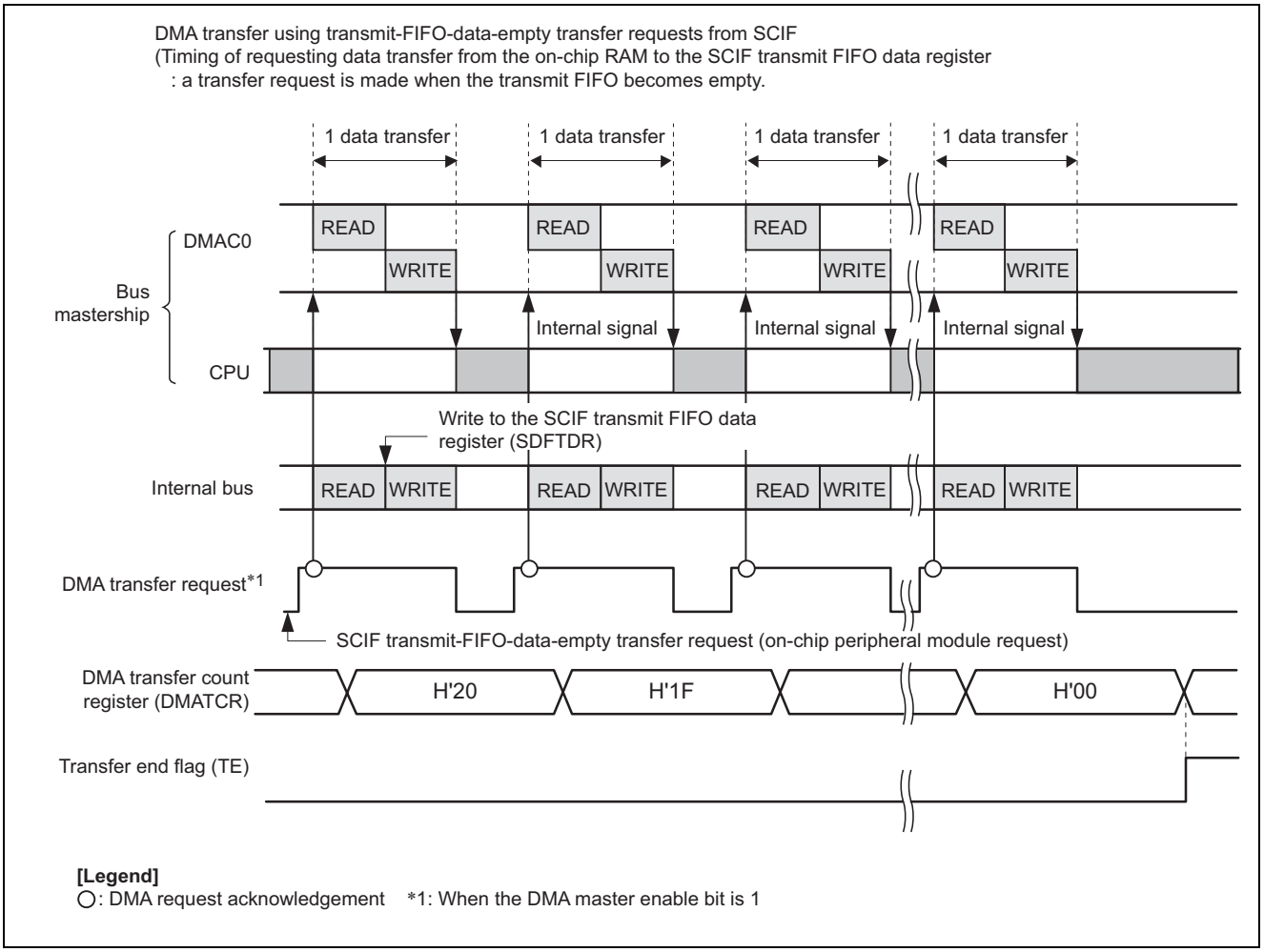


Figure 3 Timing of Operations by the Sample Program

2.3 Procedure for Setting Used Modules

This section describes the procedure for specifying initial settings for transferring data from the on-chip RAM to on-chip peripheral modules by using the DMAC.

By default, the on-chip peripheral modules of this MCU are configured to operate in module standby mode. When using any of these modules, be sure to release them from module standby mode before making the initial settings. Figure 4 shows a flowchart of the sample program. Figure 5 shows a flowchart of release from module standby mode for the DMAC and SCIF. Figures 6 and 7 illustrate flowcharts of initializing the DMAC and the SCIF, respectively. In addition, figure 8 illustrates a flowchart of DMA transfer end processing.

For details on registers, refer to the SH7211 Group Hardware Manual.

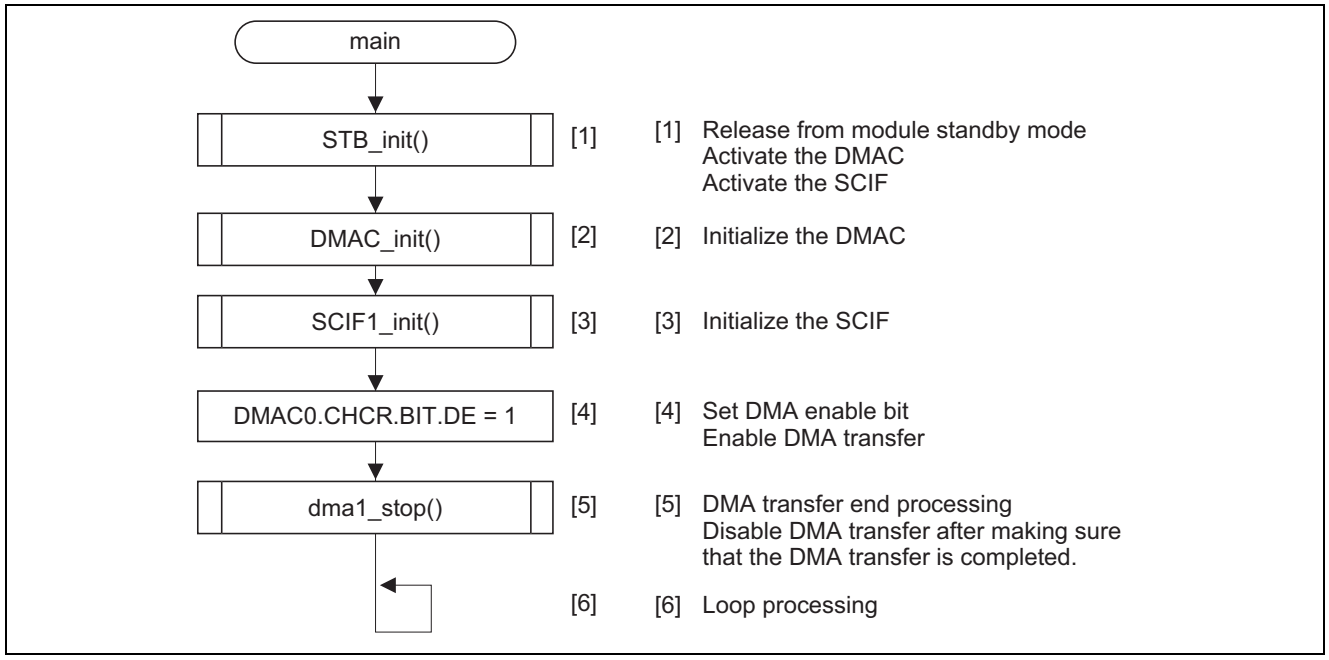


Figure 4 Flowchart of the Sample Program

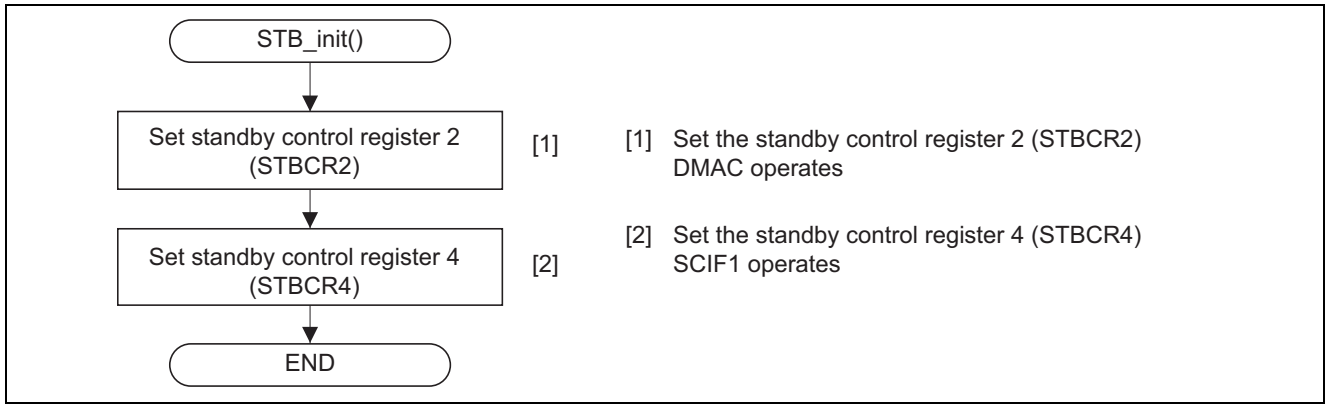


Figure 5 Flowchart of Release from Module Standby Mode for the DMAC and SCIF

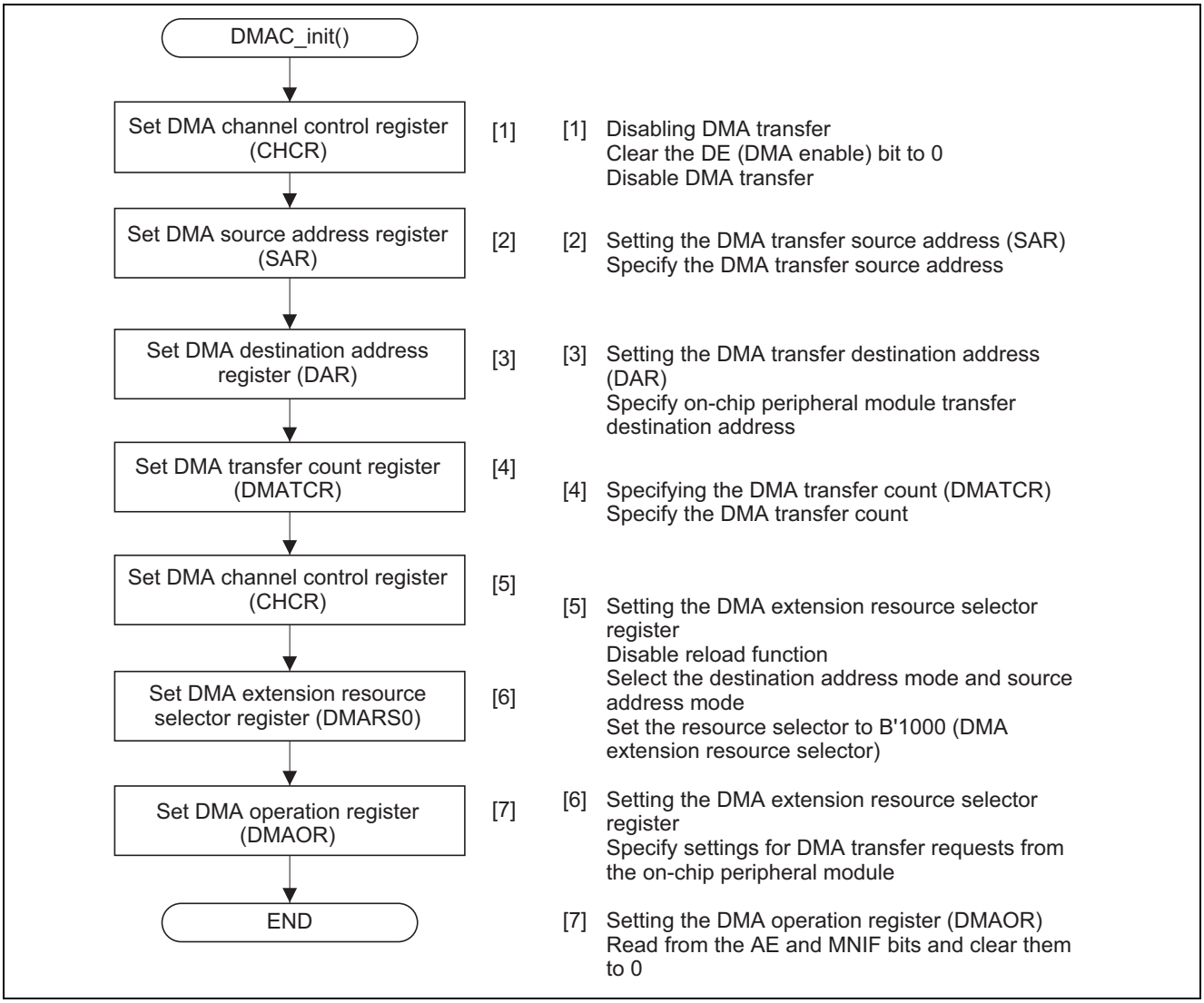
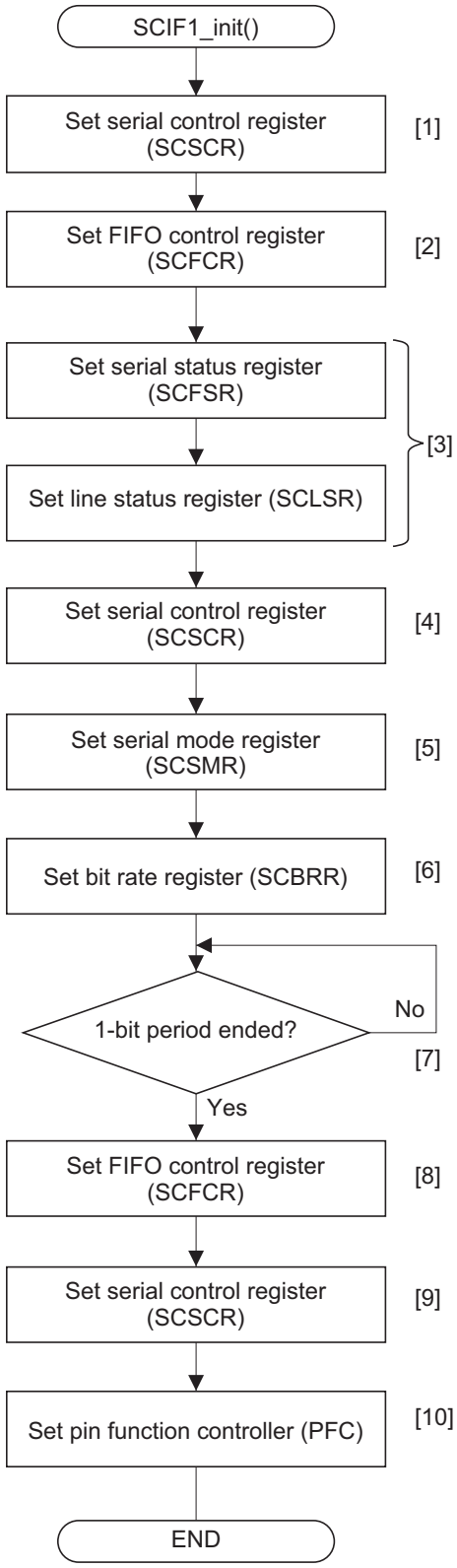


Figure 6 Flowchart of DMAC Initialization



[1] Setting the serial control register (SCSCR)
Disable transmission/reception

[2] Setting the FIFO control register (SCFCR)
Set the TFRST and RFRST bits to 1

[3] Setting the serial status register (SCFSR)
Clear the flags ER, DR, BRK, and SCLSR to 0 after reading from them
Reset the flags

[4] Setting serial control register (SCSCR)
Select pϕ clock (the TIE, RIE, TE and RE bits are 0)

[5] Setting the serial mode register (SCSMR)
Specify the transmission format

[6] Setting the bit rate register (SCBRR)
Specify the bit rate (38400bit/s)
Note: When an external clock is used, it is not necessary to set this register

[7] Insert 1-bit wait cycle

[8] Setting the FIFO control register (SCFCR)
Specify the transmit FIFO data number trigger
Clear the TFRST and RFRST bits to 0

[9] Setting the serial control register (SCSCR)
Set the TE and TIE bits to 1

[10] Setting the port A control register H3 (PACRH3)
Set PA25MD to B'101 to specify the settings for TXD1 output

Figure 7 Flowchart of SCIF Initialization

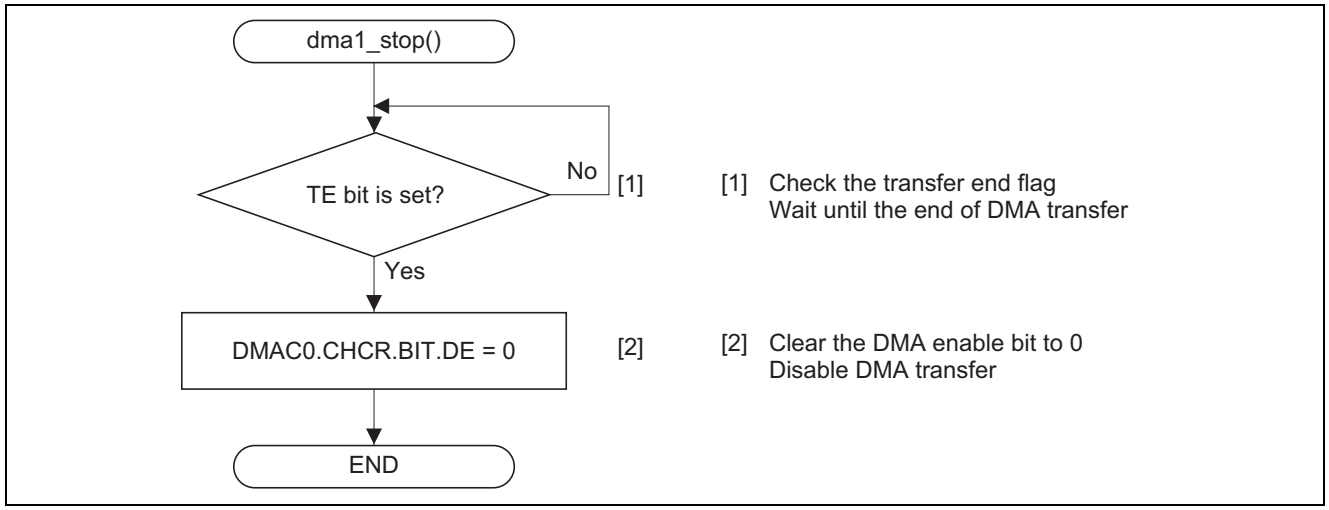


Figure 8 Flowchart of DMA Transfer End Processing

2.4 Register Settings for the Sample Program and Processing Procedure

In the sample program, character string data stored in the on-chip RAM are transferred to the transmit FIFO data register (SCFTDR) on SCIF channel 1 through DMA transfer, and then the SCIF transmits the data in asynchronous mode (UART mode).

2.4.1 1 Clock Pulse Generator (CPG)

The settings of the clock pulse generator for the sample program are listed in table 7.

Table 7 Settings of Clock Pulse Generator

Register Name	Address	Setting Value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'1303	CKOEN = "B'1": Output clocks STC[1:0] = "B'00": PLL circuit multiplication ratio × 1 IFC[2:0] = "B'000": Internal clock × 1 PFC[2:0] = "B'011": Peripheral clock × 1/4

2.4.2 Standby Control Registers

The settings of the standby control registers for the sample program are listed in table 8.

Table 8 Settings of Standby Control Registers

Register Name	Address	Setting Value	Description
Standby control register 2 (STBCR2)	H'FFFE0018	H'00	MSTP8 = "B'0": DMAC operates
Standby control register 4 (STBCR4)	H'FFFE040C	H'B6	MSTP46 = "B'0": SCIF1 operates

2.4.3 Pin Function Controller (PFC)

The settings of the pin function control register for the sample program are listed in table 9.

Table 9 Settings of Pin Function Control Register

Register Name	Address	Setting Value	Description
Port A control register H3 (PACRH3)	H'FFFE380A	H'0050	PA25MD[2:0] = "B'101": TXD1 output

2.4.4 Direct Memory Access Controller (DMAC)

The settings of the DMAC registers for the sample program are listed in table 10.

Table 10 Settings of DMAC Registers

Register Name	Address	Setting Value	Description
DAM source address register_0 (SAR_0)	H'FFFE1000	Address at which character string data are stored	Transfer Source Start Address The start address in the on-chip RAM, at which the character string is stored
DAM destination address register_0 (DAR_0)	H'FFFE1004	H'FFFE 880C	Transfer Destination Start Address SCIF transmit FIFO data register_1 (SCFTDR_1) address
DMA transfer count register_0 (DMATCR_0)	H'FFFE1008	D'32	DMA transfer count: Number of character string data
DMA channel control register_0 (CHCR_0)	H'FFFE100C	H'0000 0000	Before DMA initialization DE = "B'0": Disable DMA transfer
		H'0000 1800	DMA initialization TC = "B'0": Transfer data once per transfer request RLD = "B'0": Disable reload function (OFF) DM[1:0] = "B'00": Fix the destination address SM[1:0] = "B'01": Increment the source address RS[3:0] = "B'1000": DAM extension resource selector TB = "B'0": Cycle stealing mode TS[1:0] = "B'00": Transfer data in byte units IE = "B'0": Disable interrupt requests DE = "B'0": Disable DMA transfer
		H'0000 1805	When enabling DMA transfer IE = "B'1": Enable interrupt requests DE = "B'1": Enable DMA transfer
		H'0000 1804	When disabling DMA transfer DE = "B'0": Disable DMA transfer
DMA extension resource selector register (DMARS_0)	H'FFFE1300	H'0085	MID = "B'100001" RID = "B'01" Set to SCIF_1 transmit-FIFO-data-empty transfer request
DMA operation register (DMAOR)	H'FFFE1200	H'0000 0001	DME = "B'1": Enable DMA transfer on all the channels

2.4.5 Serial Communication Interface with FIFO

The settings of the SCIF registers for the sample program are listed in table 11.

Table 11 Settings of SCIF Registers

Register Name	Address	Setting Value	Description
Serial mode register_1 (SCSMR_1)	H'FFFE8800	H'0000	C/A = "B'0": Asynchronous mode CHR = "B'0": 8-bit data PE = "B'0": Parity bit not added or checked STOP = "B'0": 1 stop bit SCKS[1:0] = "B'00": Pϕ clock
Bit rate register_1 (SCBRR_1)	H'FFFE8804	D'32	Bit rate: 38400 (bits/s)*1
Serial control register_1 (SCSCR_1)	H'FFFE8808	H'0000	When setting TIE = "B'0": Disable transmit-FIFO-data-empty interrupt (TXI) request RIE = "B'0": Disable receive-FIFO-data-full interrupt (RXI) request, receive-error interrupt (ERI) request, and break interrupt (BRI) request TE = "B'0": Disable transmission RE = "B'0": Disable reception CKE[1:0] = "B'00": Internal clock/SCK pin used for input pin
		H'00C0	When enabling transmission TIE = "B'1": Enable transmission-FIFO-data-empty interrupt (TXI) request TE = "B'1": Enable transmission
FIFO control register_1 (SCFCR_1)	H'FFFE8818	H'0060	Initialization TFRST = "B'1": Enable resetting data for transmission in the transmit FIFO data register RFRST = "B'1": Enable resetting received data in the receive FIFO data register
		H'0000	When setting TFRST = "B'0": Disable resetting data for transmission in the transmit FIFO data register RFRST = "B'0": Disable resetting receive data in the receive FIFO data register RTRG[1:0] = "B'00": 1 Number of received data TTRG[1:0] = "B'00": 8 (8) Number of data for transmission

Note: 1. For specifying the bit rate, refer to examples of setting SCBRR in the SH7211 Group Hardware Manual.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
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