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SH7211 Group

Data Transfer between On-chip RAM Areas with DMAC (Burst Mode)

Introduction

This application note describes the operation of the DMAC, and is intended for reference to help in the design of user software.

Target Device

SH7211

Contents

1. Introduction

1.1 Specification

- DMAC channel 0 is used.
- Auto-request mode is used as the interrupt source for activating DMA transfer.
- Cycle-stealing mode is used as the bus mode.

1.2 Used Module

Direct memory access controller (DMAC channel 0)

1.3 Applicable Conditions

- Microcontroller: SH7211
- Operating Frequency: Internal clock 160 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
- C Compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01, from Renesas Technology

2. Description of Sample Application

In this sample application, the direct memory access controller (DMAC) is set to auto request mode to transfer 512-Kbtyte data stored in the on-chip RAM to another address.

2.1 Operation of Modules Used

When a DMA transfer request is made, the DMAC starts to transfer data in accordance with the priority order of channels, and continues the transfer operation until the transfer end condition is met. Transfer requests for the DMAC are of three kinds: auto requests, external requests, and on-chip peripheral module requests. The bus mode is selectable as burst mode or cycle-stealing mode.

For details on the DMAC, refer to the section on the direct memory access controller in the SH7211 Group Hardware Manual.

An overview of the DMAC is given in table 1. Examples of DMA transfer in cycle-stealing mode and burst mode are shown in figures 1 and 2, respectively. In addition, a block diagram of the DMAC is shown in figure 3.

Table 1 Overview of DMAC

Item	Description
Number of channels	8 (CH0 to CH7) Only 4 (CH0 to CH3) can receive external requests.
Address space	4 Gbytes
Length of transfer data	Byte, word (2 bytes), longword (4 bytes), and 16 bytes (longword × 4)
Maximum transfer count	16,777,216 (24 bits) transfers
Address mode	Single address mode and dual address mode
Transfer request	External request, on-chip peripheral module request, and auto request (SCIF: 8 sources, IIC3: two sources, A/D converter: one source, MTU2: five sources, CMT: two sources)
Bus mode	Cycle-stealing mode (normal mode and intermittent mode) and burst mode
Priority level	Channel priority fixed mode and round-robin mode
Interrupt request	An interrupt request to the CPU is made when half or all of a transfer process is completed.
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/transfer end signal	Active levels for DACK and TEND can be set independently

In the normal mode of cycle stealing, bus mastership is given to another bus master after each DMA transfer of one transfer unit (byte, word, longword, or 16-byte unit). When a subsequent transfer request occurs, bus mastership is obtained from the other bus master and transfer proceeds for one transfer unit. When that transfer ends, the bus mastership is passed to another bus master. This is repeated until the transfer end condition is satisfied.
The cycle-stealing normal mode can be used in transfer across any interval, regardless of the requesting source, source, and destination of the transfer.

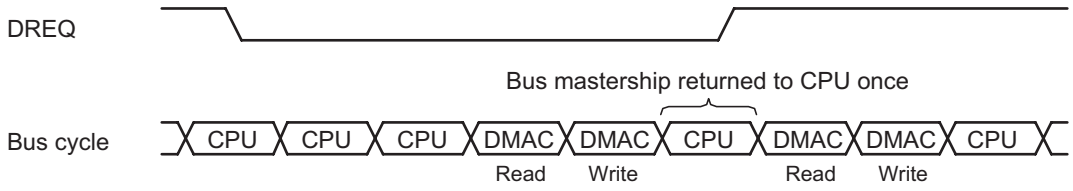


Figure 1 DMA Transfer Example in Cycle-Stealing Normal Mode (Dual Address, DREQ Low Level Detection)

In burst mode, once the DMAC has obtained bus mastership, it continues to perform transfer without releasing the bus until the transfer end condition is satisfied. In external mode, however, when the DREQ signal is being level-detected and changes to the non-active level, even if the tranfer end condition has not been satisfied, bus mastership is passed to another bus master on completion of the DMA transfer request for which the request has already been accepted.

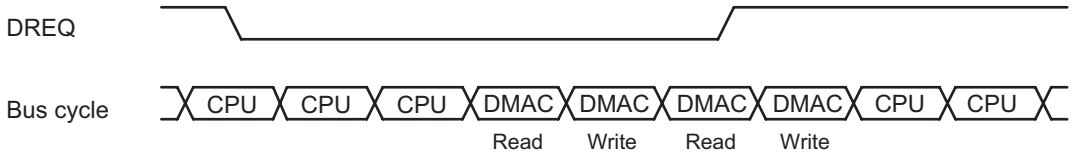
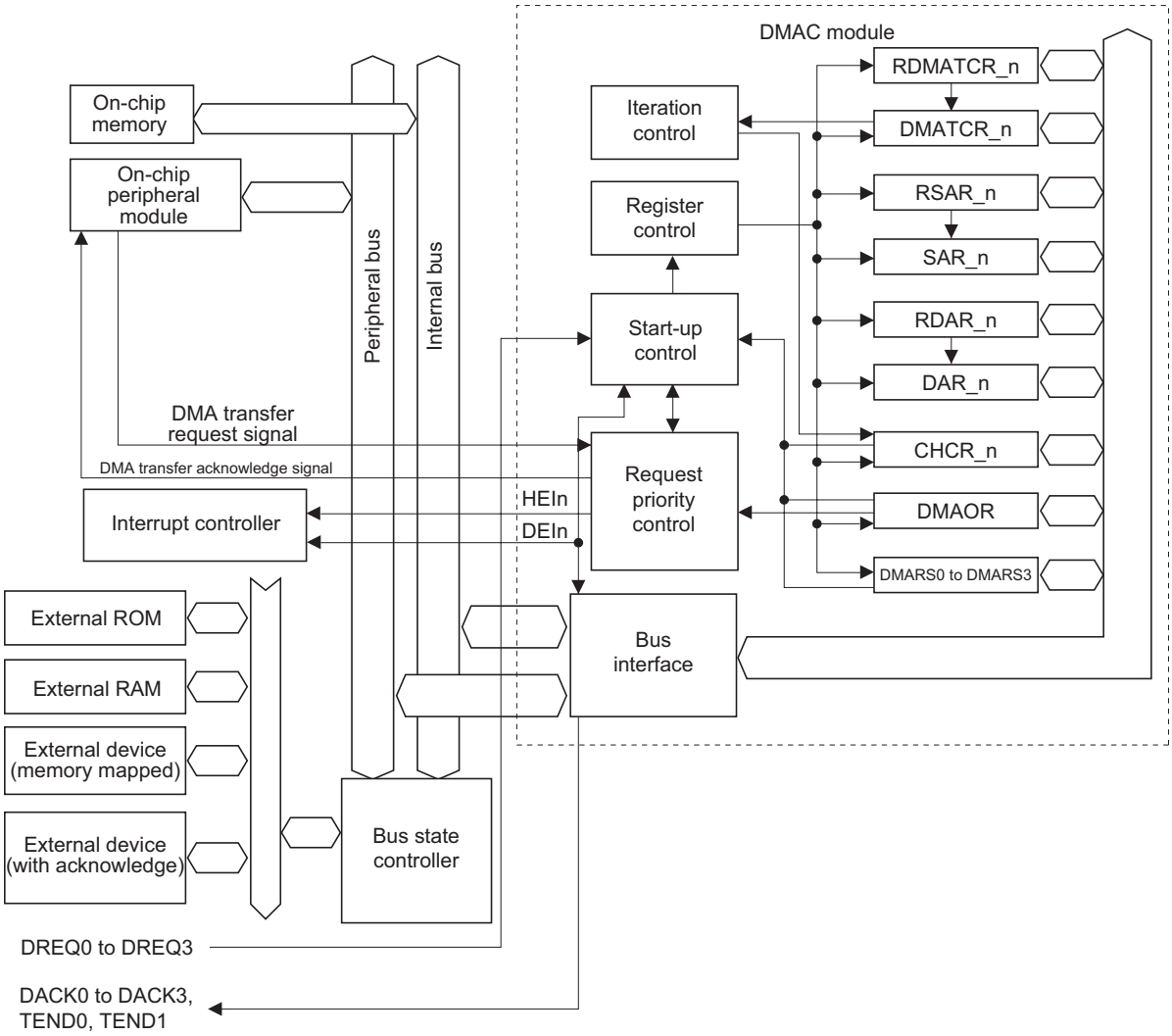


Figure 2 DMA Transfer Example in Burst Mode (Dual Address, DREQ Low Level Detection)



[Legend]

RDMATCR:	DMA reload transfer count register	CHCR:	DMA channel control register
DMATCR:	DMA transfer count register	DMAOR:	DMA operation register
RSAR:	DMA reload source address register	DMARS0 to DMARS3:	DMA extension resource selectors 0 to 3
SAR:	DMA source address register	HEIn:	DMA transfer half-end interrupt request to the CPU
RDAR:	DMA reload destination address register	DEIn:	DMA transfer end interrupt request to the CPU
DAR:	DMA destination address register	n:	0, 1, 2, 3, 4, 5, 6, 7

Figure 3 Block Diagram of DMAC

2.2 Operational Description of Sample Program

The settings of the DMAC for the sample program are listed in table 4. Also, the operation of the sample program is illustrated in figure 4.

Table 4 Settings of DMAC

DMA transfer condition	Auto request mode
Channel	CH0
Length of transfer data	4 bytes
Maximum transfer count	128 transfers (128 × data length of 4 bytes = 512-byte data)
Address mode	Dual address mode
Bus mode	Cycle-stealing mode
Priority level	Channel priority level fixed mode
Interrupt request	Disable an interrupt request to the CPU at the end of a transfer

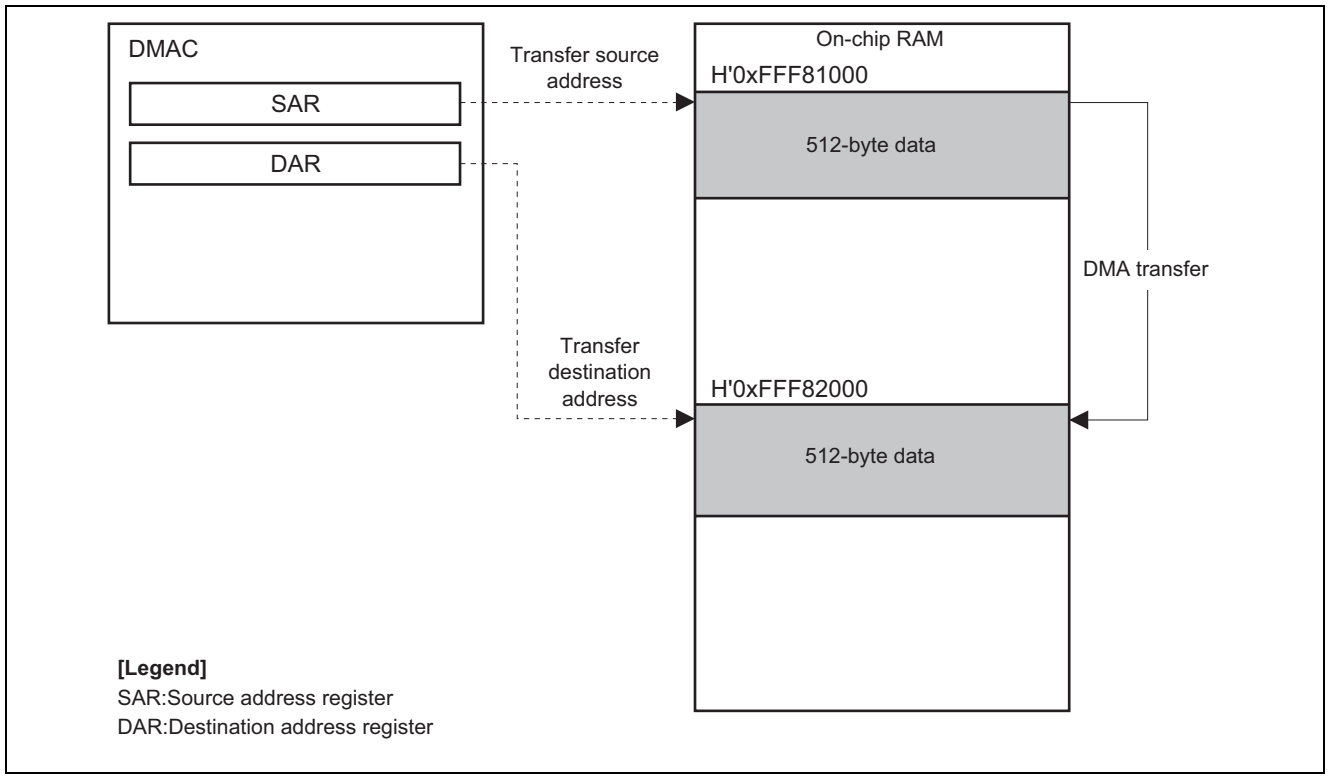


Figure 4 Operation of Sample Program

2.3 Procedure for Setting Modules

This section describes the procedure for making initial settings when the DMAC is to be used to transfer data between locations within the on-chip RAM. Auto request mode is used for the transfer requests.

By default, the on-chip peripheral modules of this MCU are in module standby mode. Whenever any of these modules is to be used, be sure to take it out of module standby mode before making the initial settings. In this sample application, processing to delete the end of DMA transfer is handled by interrupts.

Flowcharts of the sample program and DMAC initialization are shown in figure 5 and figure 6, respectively. In addition, a flowchart of DMA transfer end interrupt function is shown in figure 7.

For details on registers, refer to the SH7211 Group Hardware Manual.

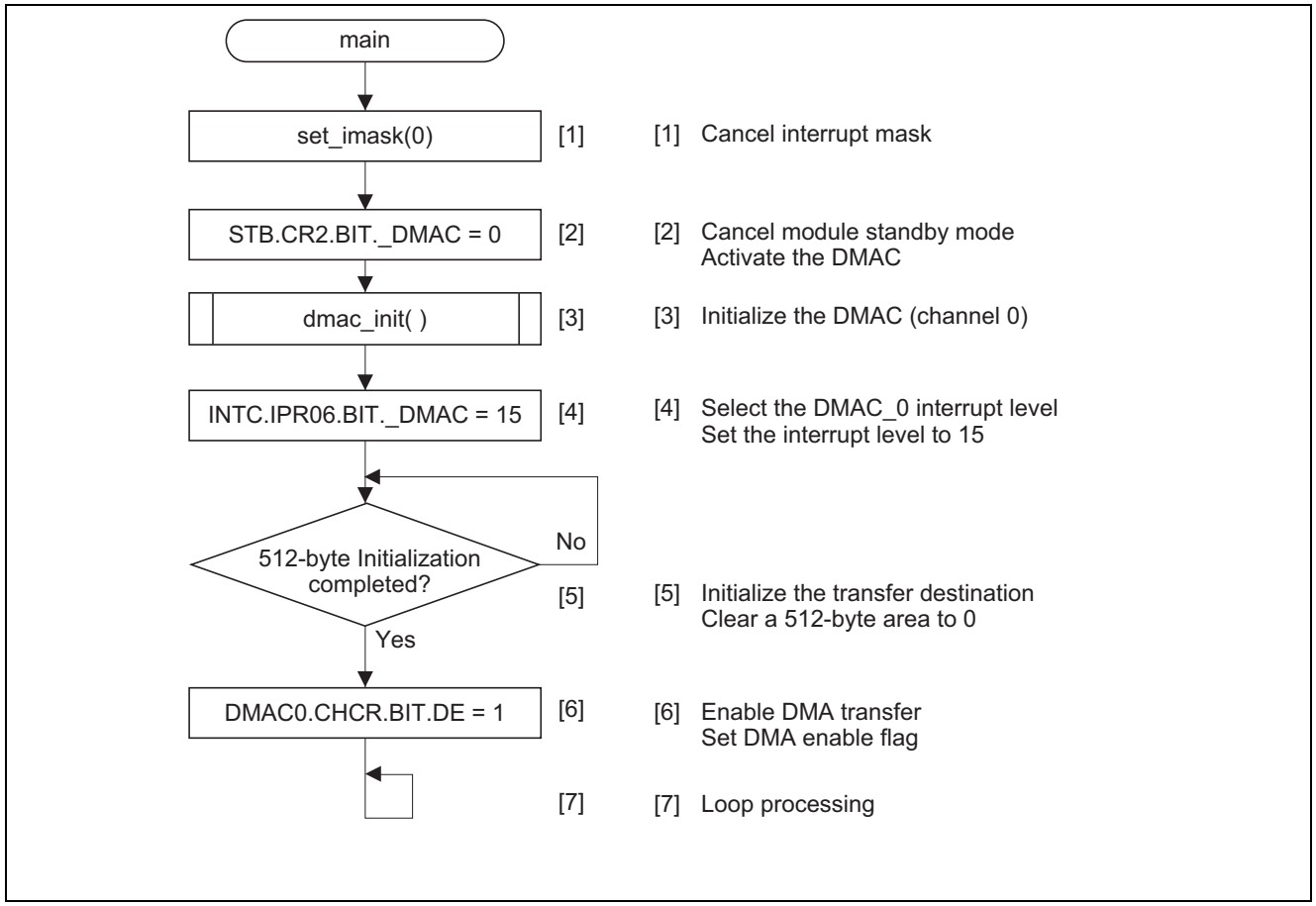


Figure 5 Flowchart of Sample Program

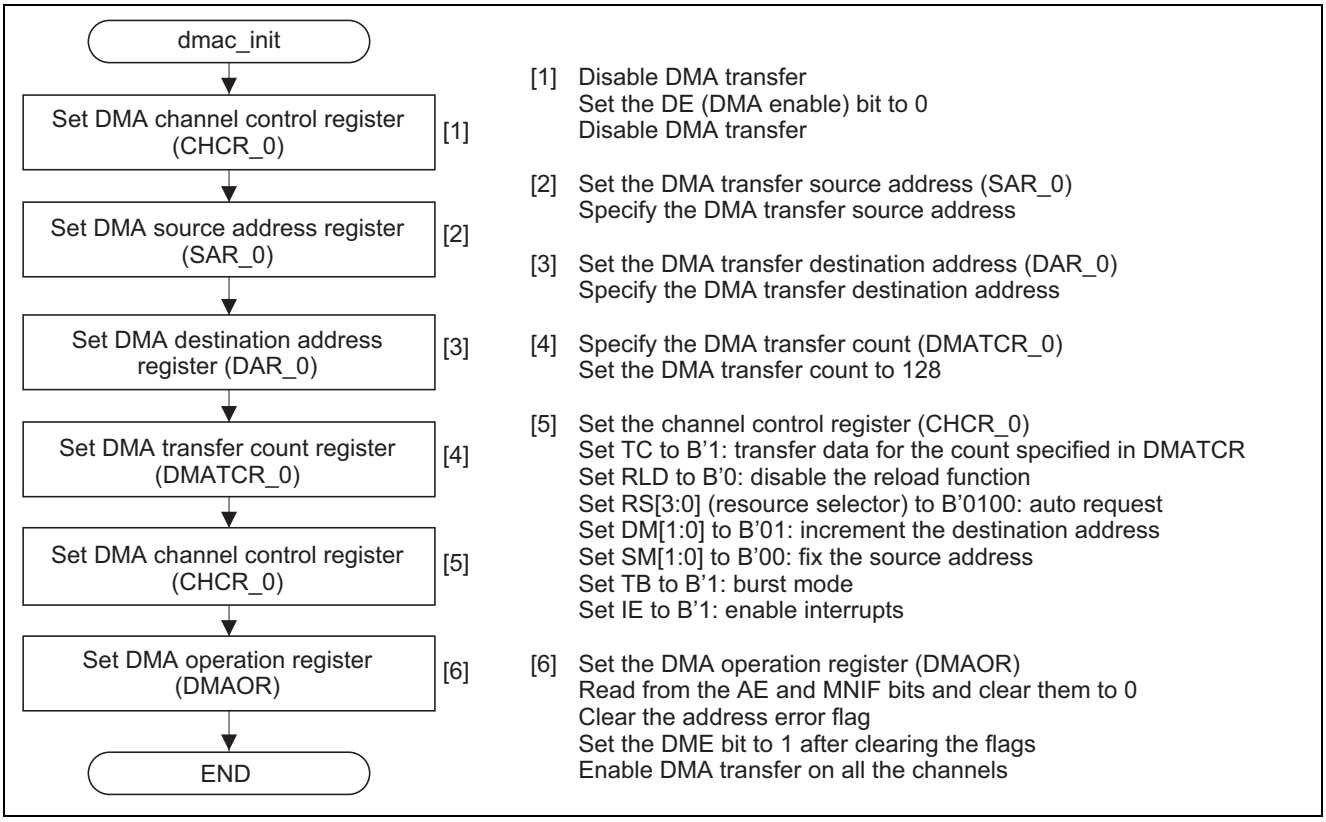


Figure 6 Flowchart of Initializing DMAC

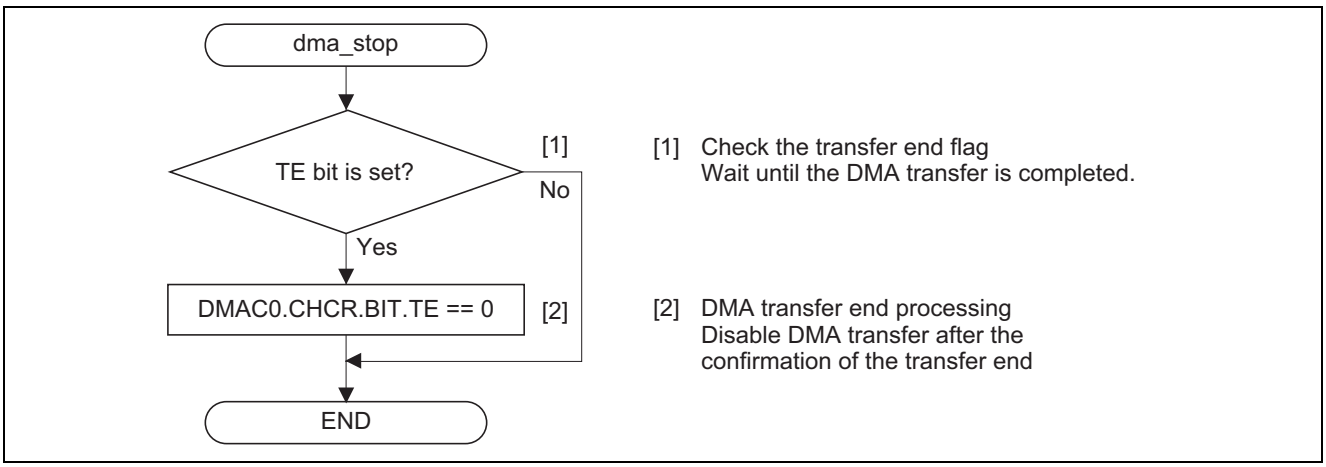


Figure 7 Flowchart of DMA Transfer End Interrupt Function

2.4 Register Settings for Sample Program

2.4.1 Clock Pulse Generator (CPG)

The settings of the clock pulse generator for the sample program are described in table 5.

Table 5 Settings of Clock Pulse Generator

Register Name	Address	Setting Value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'1303	CKOEN = "B'1": output clocks STC[1:0] = "B'00": frequency multiplication ratio of PLL circuit × 1 IFC[2:0] = "B'000": internal clock × 1 PFC[2:0] = "B'011": peripheral clock × 1/4

2.4.2 Standby Control Register

The settings of the standby control register for the sample program are described in table 6.

Table 6 Settings of Standby Control Register

Register Name	Address	Setting Value	Description
Standby control register 2 (STBCR2)	H'FFFE0018	H'00	MSTP8 = "B'0": the DMAC operates

2.4.3 Interrupt Controller (INTC)

The settings of the INTC for this sample program are described in table 7

Table 7 Settings of Interrupt Controller

Register Name	Address	Setting Value	Description
Interrupt priority register 06 (IPR06)	H'FFFE0C00	H'F000	Sets the DMAC0 interrupt level to 15

2.4.4 Direct Memory Access Controller (DMAC)

The settings of DMAC registers for the sample program are described in table 8.

Table 8 Settings of DMAC Registers

Register Name	Address	Setting Value	Description
DMA source address register 0 (SAR)	H'FFFE1000	H'FFF81000	Transfer source start address
DMA destination address register 0 (DAR)	H'FFFE1004	H'FFF82000	Transfer destination start address
DMA transfer count register 0 (DMATCR)	H'FFFE1008	D'128	DMA transfer count: 128 transfers
DMA channel control register 0 (CHCR)	H'FFFE100C	H'0000 0000	Before DMA initialization DE = "B'0": disables DMA transfer
		H'8000 4434	DMA initialization TC = "B'1": transfers data for the count specified in DMATCR for each transfer request DM[1:0] = "B'01": increments the destination address SM[1:0] = "B'00": fixes the source address RS[3:0] = "B'0100": auto request TB = "B'1": burst mode TS[1:0] = "B'10": longword (4 bytes) unit IE = "B'1": enables interrupt requests DE = "B'0": disables DMA transfer
		H'8000 4431	When enabling DMA transfer DE = "B'1": enables DMA transfer
		H'8000 4430	When disabling DMA transfer DE = "B'0": disables DMA transfer
DMA operation register (DMAOR)	H'FFFE1200	H'0000 0001	DME = "B'1": enables DMA transfer on all the channels

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7211 Group Hardware Manual
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