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# H8/300H Tiny Series

## Counting Interrupts Generated by Timer Z 16-Bit Free-Running Function

### Introduction

The free-running counter function of timer Z is used to count timer Z interrupts. The processing ends when the number of timer Z interrupts reaches 50.

### Target Device

H8/3687

### Contents

## 1. Specifications

1. The free-running counter function of timer Z is used to count timer Z interrupts. The processing ends when the number of timer Z interrupts reaches 50.
2. If the timer counter (TCNT0) overflows, a timer Z overflow interrupt request is issued.
3. An 8-bit counter that is placed in RAM is decremented in the timer Z interrupt processing. When the number of timer interrupts reaches 50, the timer Z interrupt is disabled and the processing ends.
4. A timer Z interrupt is specified to be generated every 32.768 ms where the timer counter (TCNT0) overflow occurs.

## 2. Description of Functions

1. In this sample task, the timer Z free-running counter function is used to count the number of timer Z interrupts. Figure 2.1 is a block diagram of timer Z free-running counter function. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer control register 0 (TCR0) selects the input clock for TCNT0 and the condition of clearing TCNT0. In this sample task, input clock is specified as ϕ/8, the counter value is incremented on the rising edge of the clock, and clearing of TCNT0 is disabled.
- Timer status register 0 (TSR0) indicates the timer Z status. In this sample task, the overflow flag (OVF) is set to 1 when TCNT0 overflows.
- Timer interrupt enable register (TIER0) enables or disables various interrupt requests. In this sample task, interrupts generated by TCNT0 overflow is enabled and other interrupts are disabled.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable counter that is incremented by an internal or external clock input. In this sample task, the TCNT0 counter increases on the rising edge of ϕ/8 and clearing of TCNT0 is disabled.
- Timer start register (TSTR) starts or stops TCNT0 and TCNT1 operations. In this sample task, TCNT0 is set to start counting and TCNT1 is set to stop counting.
- Timer mode register (TMDR) selects whether TCNT0 and TCNT1 operate in synchronization. In this sample task, TCNT0 operates independently of TCNT1.

The TCNT0 overflow cycle in this sample task is calculated by the following equation:

$$\text{TCNT0 overflow cycle} = \frac{1}{\text{System clock}/\ 8} \times 65536 = 32.768 \text{ ms}$$

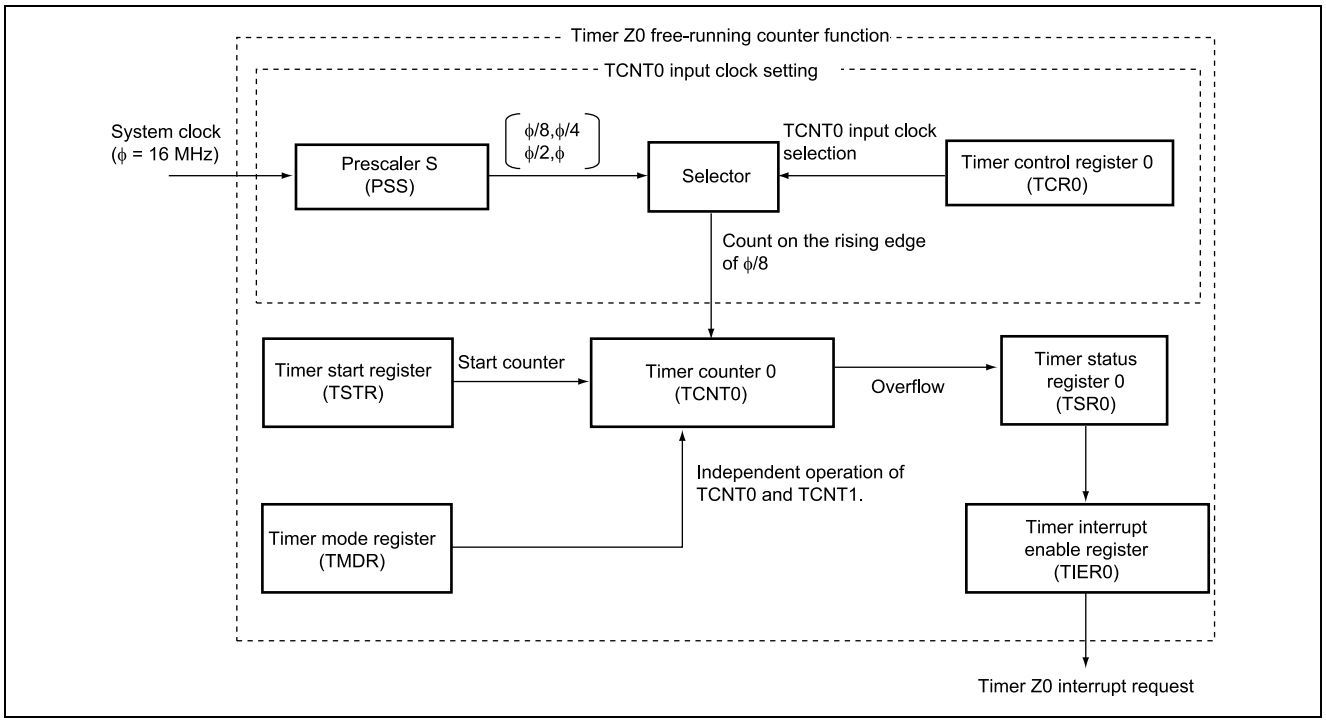



**Figure 2.1 Block Diagram of Timer Z0 Free-Running Counter Function**

2. Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the number of interrupts is counted by the timer Z's free-running counter function.

**Table 2.1 Function Allocation**

| Function | Description |
|---|---|
| PSS | 13-bit counter with system clock input |
| TCR0 | Specifies the input clock for TCNT0. |
| TSR0 | Controls the TCNT0 overflow flag. |
| TIER0 | Enables interrupt requests by TCNT0 overflow. |
| TCNT0 | 16-bit counter that is incremented on the rising edge of ϕ/8 clock. |
| TSTR | Starts or stops counting by TCNT0. |
| TMDR | Specifies TCNT0 to operate independently of TCNT1. |
| counter | 8-bit counter that counts the number of timer Z interrupts up to 50. |

## 3. Description of Operation

Operation of this sample task is described in figure 3.1. The hardware and software processing is applied as shown in figure 3.1 to count the number of interrupts by using the free-running counter function of timer Z.

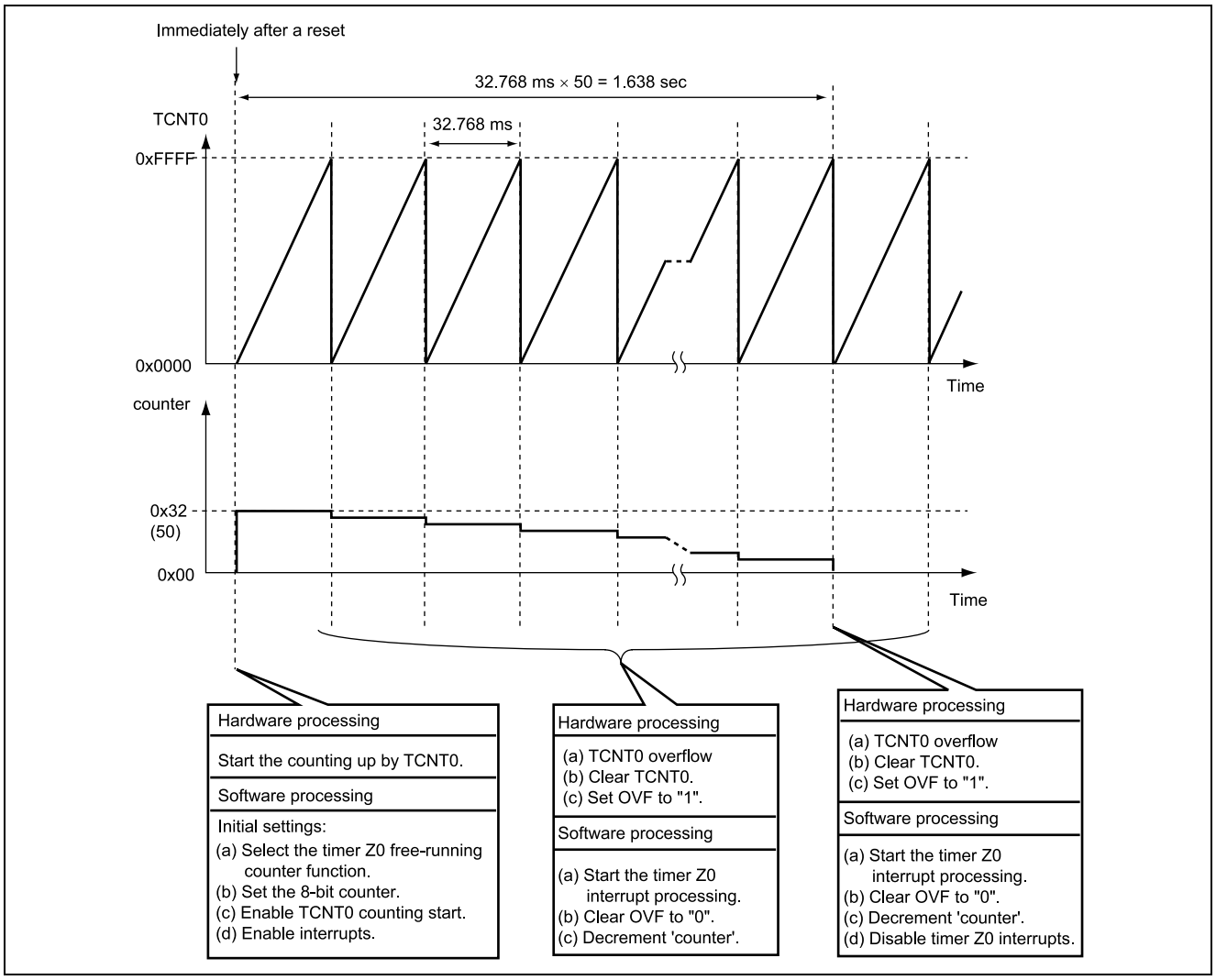



**Figure 3.1 Principle of Operation**

# 4. Description of Software

## 4.1 Modules

Table 4.1 describes the module used in this sample task.

**Table 4.1 Description of Modules**

| Module Name | Label Name | Function |
|---|---|---|
| Main routine | main | Selects the timer Z0 free-running counter function, starts counting by TCNT0, and provides settings for interrupts. |
| Interrupt count | tz0int | Timer Z0 interrupt processing<br>Decrements the 8-bit counter in RAM and disables timer Z0 interrupts when the counter reaches 0x00. |

## 4.2 Arguments

This sample task uses no arguments.

## 4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCR0 Timer control register 0 Address: 0xF700

| Bit | Bit Name | Setting | Function |
|---|---|---|---|
| 7 | CCLR2 | CCLR2 = 0 | Counter clear 2 to 0 |
| 6 | CCLR1 | CCLR1 = 0 | CCLR2 = 0, CCLR1 = 0, CCLR0 = 0: Disables clearing of TCNT0. |
| 5 | CCLR0 | CCLR0 = 0 | |
| 4 | CKEG1 | CKEG1 = 0 | Clock edge 1 to 0 |
| 3 | CKEG0 | CKEG0 = 0 | CKEG1 = 0, CKEG = 0: Counts on the rising edge of the clock. |
| 2 | TPSC2 | TPSC2 = 0 | Clock select 2 to 0 |
| 1 | TPSC1 | TPSC1 = 1 | TPSC2 = 0, TPSC1 = 1, TPSC0 = 1: Counts by an internal clock $\phi$/8. |
| 0 | TPSC0 | TPSC0 = 1 | |

- TSR0 Timer status register 0 Address: 0xF703

| Bit | Bit Name | Setting | Function |
|---|---|---|---|
| 4 | OVF | 0 | Overflow flag<br>OVF = 0: Indicates that TCNT0 overflow has not occurred.<br>OVF = 1: Indicates that TCNT0 overflow has occurred. |

- TIER0 Timer interrupt enable register 0 Address: 0xF704

| Bit | Bit Name | Setting | Function |
|---|---|---|---|
| 4 | OVIE | 1 | Timer overflow interrupt enable<br>OVIE = 0: Disables interrupts by the OVF flag in TSR0.<br>OVIE = 1: Enables interrupts by the OVF flag in TSR0. |

- TCNT0 Timer counter 0 Address: 0xF706
  Function: An 8-bit up-counter that is incremented by clock input of system clock/8.
  Setting: 0x0000

- TSTR Timer start register Address: 0xF720

| Bit | Bit Name | Setting | Function |
|---|---|---|---|
| 0 | STR0 | 0 | Channel 0 counter start<br>STR0 = 0: Stops counting by TCNT0.<br>STR0 = 1: Starts counting by TCNT0. |

- TMDR Timer mode register Address: 0xF721

| Bit | Bit Name | Setting | Function |
|---|---|---|---|
| 0 | SYNC | 0 | Timer synchronization<br>SYNC = 0: TCNT0 operates independently of TCNT1.<br>SYNC = 1: TCNT0 operates synchronously with TCNT1. |

## 4.4 Description of RAM

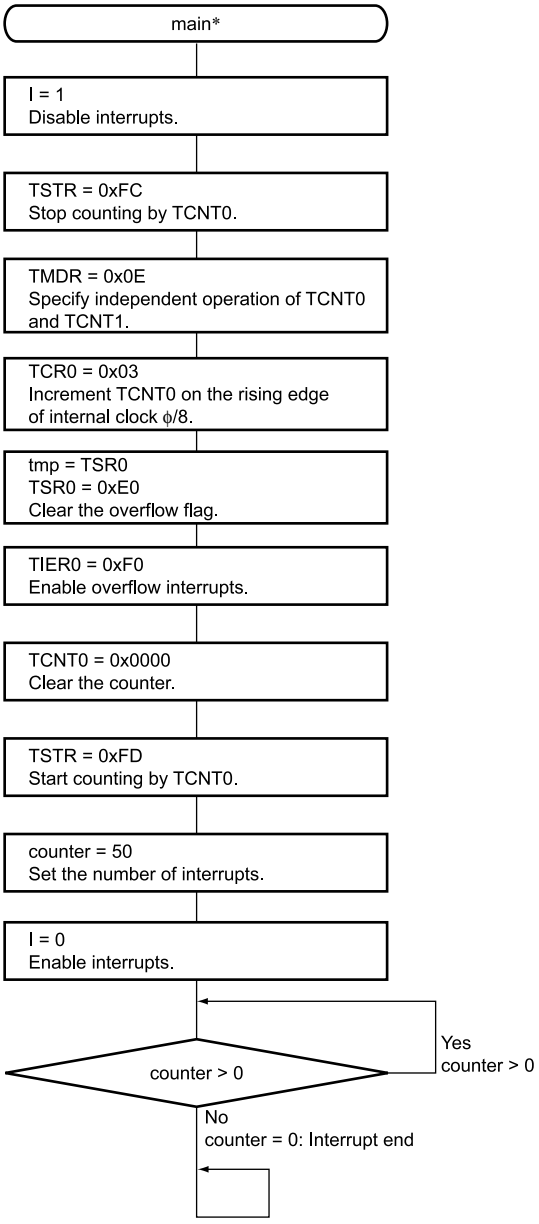
Table 4.2 describes the RAM used in this sample task.

**Table 4.2 Description of RAM**

| Label Name | Function | Size | Used in |
|---|---|---|---|
| counter | An 8-bit counter that counts the number of timer Z interrupts up to 50 | 1 byte | Main routine<br>Interrupt count |

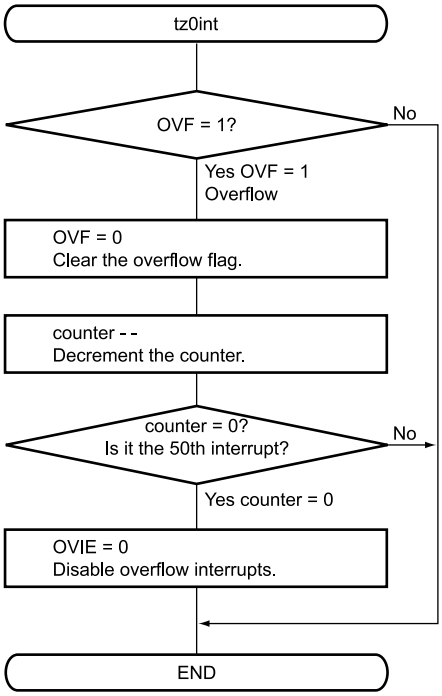
## 5. Flowchart

1. Main routine




Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Interrupt count



## 6. Program List

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Interrupt Counting by 16bit Free Running Function'                                                                */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer Z 16bit Free Running Timer                                                                                 */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                  /* Timer control register_0               */
#define        TSR0           *(volatile unsigned char *)0xF703                  /* Timer status register_0                */
#define        TSR0_BIT       (*(struct BIT *)0xF703)                            /* Timer status register_0                */
#define        OVF            TSR0_BIT.b4                                        /* Overflow Flag                          */
#define        TIER0          *(volatile unsigned char *)0xF704                  /* Timer interrupt enable register0       */
#define        TIER0_BIT      (*(struct BIT *)0xF704)                            /* Timer interrupt enable register0       */
#define        OVIE           TIER0_BIT.b4                                       /* Overflow Interrupt Enable              */
#define        TCNT0          *(volatile unsigned short *)0xF706                 /* Timer counter_0                        */
#define        TSTR           *(volatile unsigned char *)0xF720                  /* Timer start register                   */
#define        TMDR           *(volatile unsigned char *)0xF721                  /* Timer mode register                    */

#pragma interrupt   (tz0int)
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                       /* SP Set                                 */
void main ( void );
void tz0int ( void );
```

```
/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned char  counter;                                        /* 8bit Counter                                 */

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                  /* VECTOR SECTOIN SET                           */
void (*const VEC_TBL1[])(void) = {                                      /* 0x00 - 0x0f                                  */
     INIT                                                               /* 00 Reset                                     */
};
#pragma section     V2                                                  /* VECTOR SECTOIN SET                           */
void (*const VEC_TBL2[])(void) = {
     tz0int                                                             /* 34 Timer Z0 Interrupt                        */
};

#pragma section                                                         /* P                                            */

/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                                  /* Interrupt Disable                            */

     TSTR = 0xFC;                                                       /* TCNT0 count stop                             */
     TMDR = 0x0E;                                                       /* TCNT0,TCNT1 Single Mode                      */
     TCR0 = 0x03;                                                       /* Rising edge, phi/8                           */
     tmp = TSR0;
     TSR0 = 0xE0;                                                       /* Interrupt Flag Clear                         */
     TIER0 = 0xF0;                                                      /* OVF Interrupt Enable                         */
     TCNT0 = 0x0000;                                                    /* Clear TCNT0                                  */
     TSTR = 0xFD;                                                       /* TCNT0 count start                            */
     counter = 50;

     set_imask_ccr(0);                                                  /* Interrupt Enable                             */
     while(counter > 0);

     while(1);
}

/************************************************************************************************************************/
/*   Timer Z0 Interrupt                                                                                                 */
/************************************************************************************************************************/
void tz0int ( void )
{
     unsigned char tmp;

     if(OVF == 1){                                                      /* Overflow ?                                   */
          OVF = 0;                                                      /* Clear Overflow Flag                          */
          counter--;                                                    /* counter decrement                            */
          if(counter == 0x00){
               OVIE = 0;                                                /* Overflow Interrupt Disable                   */
          }
     }
}
```

**Link address specifications**

| Section Name | Address |
|---|---|
| CV1 | 0x0000 |
| CV2 | 0x0034 |
| P | 0x0100 |
| B | 0xFB80 |

## Revision Record

| | | Description | |
|---|---|---|---|
| Rev. | Date | Page | Summary |
| 1.00 | Sep.29.03 | — | First edition issued |
| | | | |
| | | | |
| | | | |
| | | | |

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