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H8/300H Tiny Series

Counting 32-Bit Data using Timer Z Cascaded Connection

Introduction

Timer counters 0 and 1 (TCNT0 and TCNT1) of timer Z are connected in cascade to operate as a 32-bit free-running counter.

Target Device

H8/3687

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1. Specifications

1. Timer counters 0 and 1 (TCNT0 and TCNT1) of timer Z are connected in cascade to operate as a 32-bit free-running counter. Figure 1.1 shows the MPU connection for cascade operation.
2. When TCNT1 overflows, the FTIOA1 pin toggles its output, which is then input to the FTIOA0 pin. On receiving the toggle output through the FTIOA0 pin, the TCNT0 counter value is incremented.
3. The TCNT0 is initialized to 0x0000 when it reaches 0xFFFF and starts counting again.

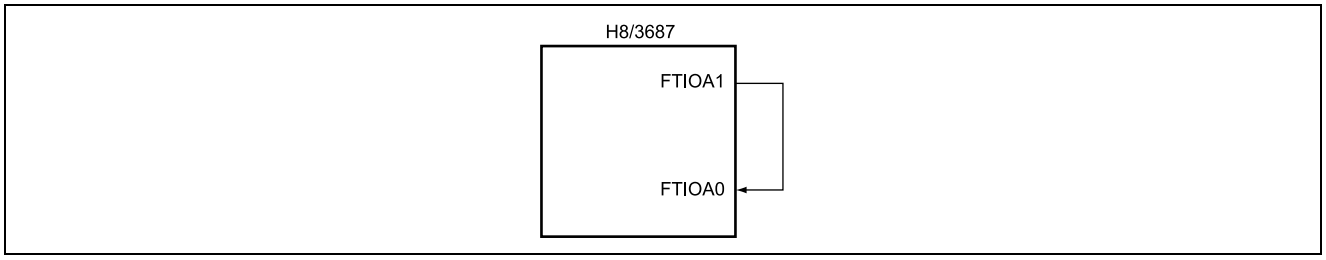


Figure 1.1 MPU Connection for Timer Z Cascade Operation

2. Description of Functions

1. In this sample task, timer Z timer counter 0 (TCNT0) and timer counter 1 (TCNT1) are connected in cascade to form a 32-bit free-running counter. Figure 2.1 is a block diagram of timer Z. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer control register 0 (TCR0) selects TCNT0 input clock and clearing method. In this sample task, the TCNT0 is incremented at the rising and falling edges of an external clock, and the TCNT0 is specified not to be cleared.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable upward counter that is incremented by the internal clock or external clock input. In this sample task, TCNT0 is incremented at the rising and falling edges of an external clock.
- Time control register 1 (TCR1) selects the TCNT1 input clock and clearing method. In this sample task, the TCNT1 is incremented at the rising edge of ϕ and is specified not to be cleared.
- Timer I/O control register A1 (TIORA1) controls GRA1 and GRB1. In this sample task, GRA1 is used as an output-compare register and the output on the FTIOA1 pin is toggled on a compare-match with GRA1.
- Timer counter 1 (TCNT1) is a 16-bit readable/writable upward counter that is incremented by the internal clock or external clock input. In this sample task, TCNT1 is incremented at the rising edge of ϕ.
- General register A1 (GRA1) is a 16-bit readable/writable register. The value of GRA1 is always compared with that of TCNT1. In this sample task, the GRA1 is set to 0x0000.
- Timer start register (TSTR) starts or stops the TCNT0 and TCNT1 operation. In this sample task, TCNT0 and TCNT1 are specified to perform counting.
- Timer mode register (TMDR) selects synchronous or independent operation of TCNT0 and TCNT1. In this sample task, independent operation is selected.
- Timer function control register (TFCR) specifies various operation modes and selects the output level. In this sample task, an external clock input is enabled and channels 0 and 1 are specified for normal operation.
- Timer output master enable register (TOER) enables or disables channels 0 and 1 outputs. In this sample task, the FTIOA0 output is disabled and the FTIOA1 output is enabled.
- Input-capture/output-compare A0 pin (FTIOA0) is specified as an input-capture input pin and the TCNT0 is incremented at the rising and falling edges.
- Input-capture/output-compare A1 pin (FTIOA1) is specified as an output-compare output pin and its output is toggled when TCNT1 matches GRA1.

$$\text{TCNT1 overflow cycle} = \frac{1}{\text{System clock/1}} \times 65536 = 4.096 \text{ ms}$$

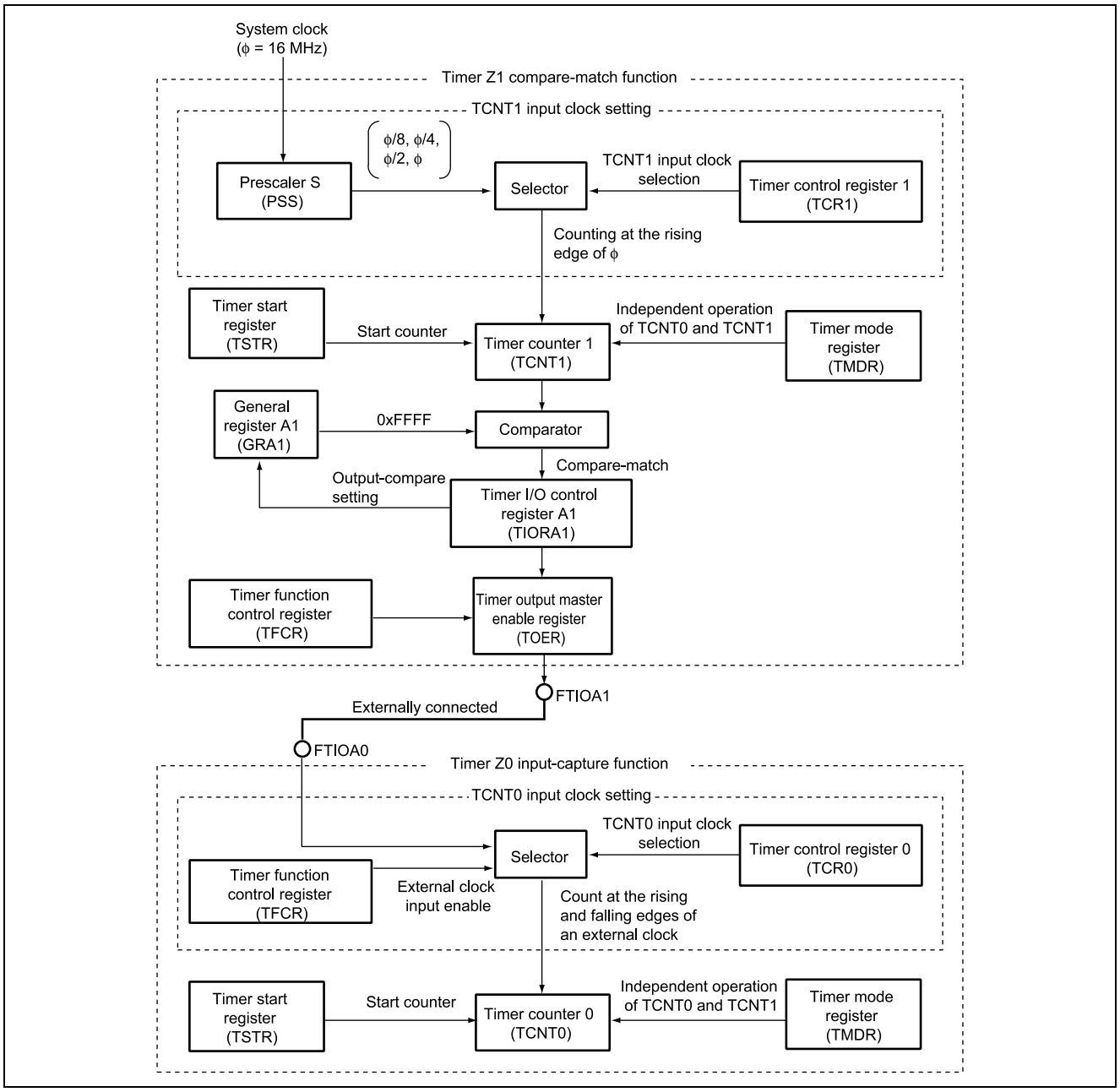


Figure 2.1 Block Diagram of the 32-bit Counter Using Timer Z Cascaded Connection

2. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so that a 32-bit counter is implemented by cascade connection of timer Z.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCR0	Specifies an input clock for the 32-bit counter.
TCNT0	Upper 16 bits of the 32-bit counter
TCR1	Specifies the TCNT1 to be incremented at both edges of the FTIIOB0 pin
TIORA1	Configures the FTIOA1 pin.
TCNT1	Lower 16 bits of the 32-bit counter
GRA1	Compared with TCNT1 to check whether or not an overflow has occurred (0xFFFF -> 0x0000).
TSTR	Starts counting by TCNT0 and TCNT1.
TMDR	Specifies TCNT0 to operate independently of TCNT1
TFCR	Sets the external clock input, and specifies channels 0 and 1 for normal operation.
TOER	Disables the FTIOA0 pin output and enables the FTIOA1 pin output
TFIOA0 pin	A carry from the lower 16 bits is input.
TFIOA1 pin	Toggles the output when the lower 16 bits overflow (when TCNT1 matches GRA1).

3. Description of Operation

Figure 3.1 illustrates the operation of this sample task. The hardware and software processing are applied as shown in figure 3.1 to implement a 32-bit counter by the cascade connection of timer Z.

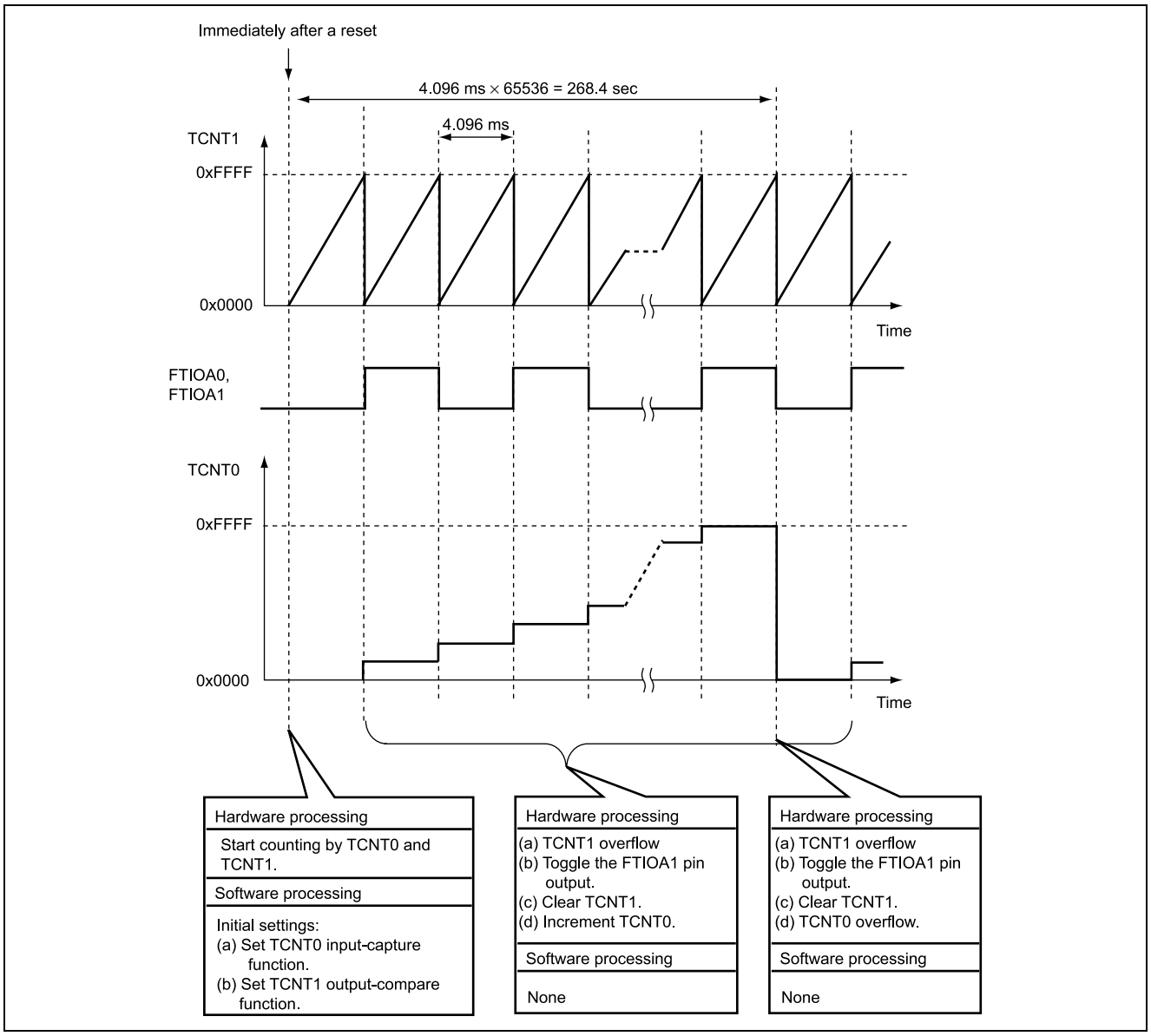


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Module

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of the Module

Module Name	Label Name	Function
Main routine	main	Sets the timer Z0 input-capture function and timer Z1 compare-match function, and starts counters.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCR0 Timer control register 0 Address: 0xF700

Bit	Bit Name	Setting	Function
7	CCLR2	CCLR2 = x	Counter clear 2 to 0
6	CCLR1	CCLR1 = 0	CCLR2 = x, CCLR1 = 0, CCLR0 = 0: Disables clearing of TCNT0.
5	CCLR0	CCLR0 = 0	(x: Don't care)
4	CKEG1	CKEG1 = 1	Clock edge 1 to 0
3	CKEG0	CKEG0 = x	CKEG1 = 1, CKEG0 = x: Counts at the rising and falling edges of the clock. (x: Don't care)
2	TPSC2	TPSC2 = 1	Timer prescaler 2 to 0
1	TPSC1	TPSC1 = x	TPSC2 = 1, TPSC1 = x, TPSC0 = x:
0	TPSC0	TPSC0 = x	Counts by an external clock input from the FTIOA0 pin. (x: Don't care)

- TIORA0 Timer I/O control register A0 Address: 0xF701

Bit	Bit Name	Setting	Function
2	IOA2	IOA2 = 0	I/O control A2 to A0
1	IOA1	IOA1 = 0	IOA2 = 0, IOA1 = 0, IOA0 = 0:
0	IOA0	IOA0 = 0	Specifies the GRA0 as an output-compare register and disables the FTIOA0 pin output by compare-matches.

- TCNT0 Timer counter 0 Address: 0xF706
  Function: A 16-bit upward counter that is incremented at the rising and falling edges of an external clock.
  Setting: 0x0000

- TCR1 Timer control register 1 Address: 0xF710

Bit	Bit Name	Setting	Function
7	CCLR2	CCLR2 = x	Counter clear 2 to 0
6	CCLR1	CCLR1 = 0	CCLR2 = x, CCLR1 = 0, CCLR0 = 0: Disables clearing of TCNT0.
5	CCLR0	CCLR0 = 0	(x: Don't care)
4	CKEG1	CKEG1 = 0	Clock edge 1 to 0
3	CKEG0	CKEG0 = 0	CKEG1 = 0, CKEG0 = 0: Counts at the rising edge of the clock.
2	TPSC2	TPSC2 = 0	Timer prescaler 2 to 0
1	TPSC1	TPSC1 = 0	TPSC2 = 0, TPSC1 = 0, TPSC0 = 0: Counts by ϕ.
0	TPSC0	TPSC0 = 0	

- TIORA1 Timer I/O control register A1 Address: 0xF711

Bit	Bit Name	Setting	Function
2	IOA2	IOA2 = 0	I/O control A2 to A0
1	IOA1	IOA1 = 1	IOA2 = 0, IOA1 = 1, IOA0 = 1:
0	IOA0	IOA0 = 1	Specifies the GRA1 as an output-compare register and the FTIOA1 pin output be toggled on a compare-match with GRA1.

- TCNT1 Timer counter 1 Address: 0xF716
  Function: A 16-bit upward counter that is incremented at the rising edge of ϕ.
  Setting: 0x0000

- GRA1 General register A1 Address: 0xF718
  Function: A compare-match is generated when the GRA1 value matches the TCNT1 counter value.
  Setting: 0xFFFF

- TSTR Timer start register Address: 0xF720

Bit	Bit Name	Setting	Function
1	STR1	0	Channel 1 counter start STR1 = 0: Stops counting by TCNT1. STR1 = 1: Starts counting by TCNT1.
0	STR0	0	Channel 0 counter start STR0 = 0: Stops counting by TCNT0. STR0 = 1: Starts counting by TCNT0.

- TMDR Timer mode register Address: 0xF721

Bit	Bit Name	Setting	Function
0	SYNC	0	Timer synchronization SYNC = 0: TCNT0 operates independently of TCNT1. SYNC = 1: TCNT0 operates synchronously with TCNT1.

- TFCR Timer function control register Address: 0xF723

Bit	Bit Name	Setting	Function
6	STCLK	1	External clock input select STCLK = 0: Disables an external clock input. STCLK = 1: Enables an external clock input
1	CMD1	CMD1 = 0	Combination mode 1 to 0
0	CMD0	CMD0 = 0	CMD1 = 0, CMDk0 = 0: Channels 0 and 1 operate in normal operation mode.

- TOER Timer output master enable register Address: 0xF724

Bit	Bit Name	Setting	Function
4	EA1	0	Master enable A1 EA1 = 0: Enables the FTIOA1 pin output. EA1 = 1: Disables the FTIOA1 pin output.
0	EA0	1	Master enable A0 EA0 = 0: Enables the FTIOA0 pin output. EA0 = 1: Disables the FTIOA0 pin output.

- PCR6 Port control register 6 Address: 0xFFE9

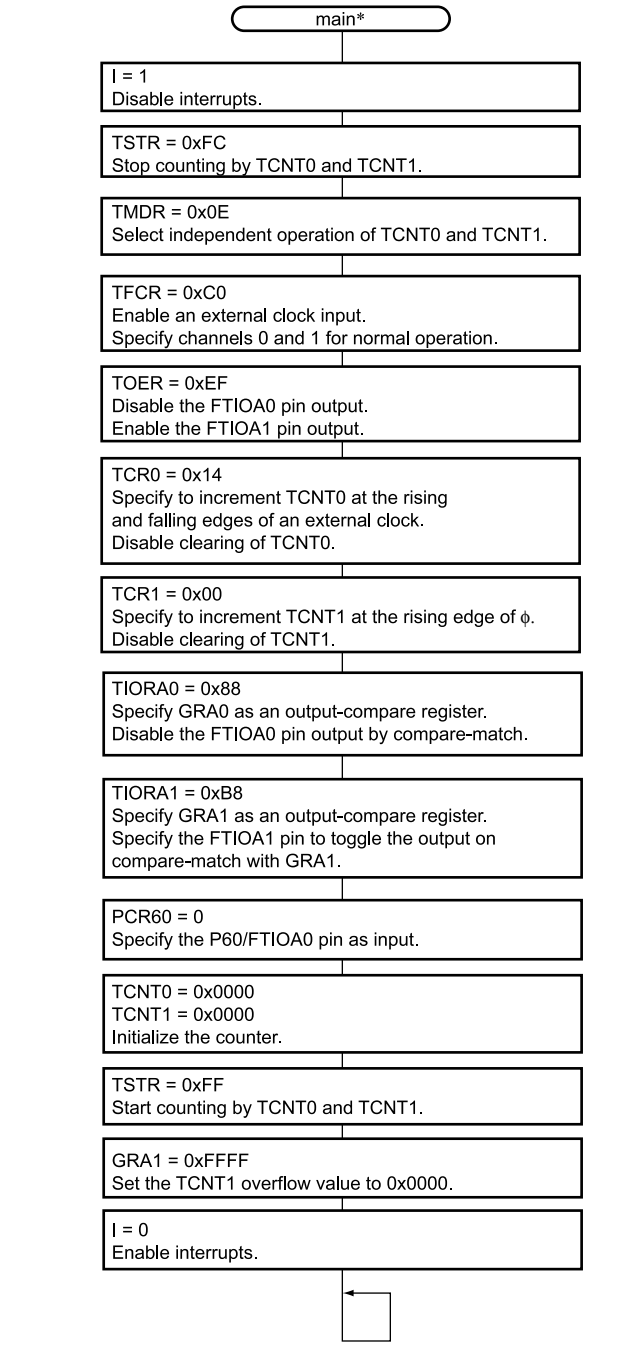
Bit	Bit Name	Setting	Function
0	PCR60	0	Port control register 60 PCR60 = 0: Specifies the P60/FTIOA0 pin as an input. PCR60 = 1: Specifies the P60/FTIOA0 pin as an output.

4.4 Description of RAM

This sample task does not use RAM.

5. Flowchart

Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   '32 bit Free runninng counter '                                                                                    */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer Z Output Compare                                                                                           */
/*   : Timer Z 16bit External clock count                                                                               */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                  /* Timer control register_0                */
#define        TIORA0         *(volatile unsigned char *)0xF701                  /* Timer I/O Control Register A_0          */
#define        TCNT0          *(volatile unsigned short *)0xF706                 /* Timer counter_0                         */
#define        TCR1           *(volatile unsigned char *)0xF710                  /* Timer control register_1                */
#define        TIORA1         *(volatile unsigned char *)0xF711                  /* Timer I/O Control Register A_1          */
#define        TCNT1          *(volatile unsigned short *)0xF716                 /* Timer counter_1                         */
#define        GRA1           *(volatile unsigned short *)0xF718                 /* General register A_1                    */
#define        TSTR           *(volatile unsigned char *)0xF720                  /* Timer start register                    */
#define        TMDR           *(volatile unsigned char *)0xF721                  /* Timer mode register                     */
#define        TFCR           *(volatile unsigned char *)0xF723                  /* Timer function control register         */
#define        TOER           *(volatile unsigned char *)0xF724                  /* Timer output master enable register     */
#define        TOCR           *(volatile unsigned char *)0xF725                  /* Timer output control register           */
#define        PCR6           *(volatile unsigned char *)0xFFE9                  /* Port Control Register 6                 */
#define        PCR6_BIT       (*(struct BIT *)0xFFE9                             /* Port Control Register 6                 */
#define        PCR60          PCR6_BIT.b0                                        /* Port Control Register 60                */

/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                      /* SP Set                                  */
void main ( void );
```

```
/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                  /* VECTOR SECTOIN SET                       */
void (*const VEC_TBL1[])(void) = {                                      /* 0x00 - 0x0f                              */
     INIT                                                               /* 00 Reset                                 */
};

#pragma section                                                         /* P                                        */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     set_imask_ccr(1);                                                  /* Interrupt Disable                        */

     TSTR = 0xFC;                                                       /* TCNT0,TCNT1 count stop                   */
     TMDR = 0x0E;                                                       /* TCNT0,TCNT1 Single Mode                  */
     TFCR = 0xC0;                                                       /* Chanel 0,1 is Normal Mode                */
     TOER = 0xEF;                                                       /* FTIOB0 Output Enable                     */
     TCR0 = 0x14;                                                       /* Both edges, FTIOA0 Clock count           */
     TCR1 = 0x00;                                                       /* Rising edge, phi Clock count             */
     TIORA0 = 0x88;                                                     /* Not output by GRA0 compare match         */
     TIORA1 = 0x8B;                                                     /* Toggle output by GRA1                    */
                                                                        /* compare match                            */
     PCR60 = 0;                                                         /* P60 input / FTIOA0 input pin             */
     TCNT0 = 0x0000;                                                    /* Clear TCNT0                              */
     TCNT1 = 0x0000;                                                    /* Clear TCNT1                              */
     TSTR = 0xFF;                                                       /* TCNT0,TCNT1 count start                  */
     GRA1 = 0x0000;                                                     /* Set Overflow value                       */

     set_imask_ccr(0);                                                  /* Interrupt Enable                         */

     while(1);
}
```

Link address specifications

Section Name	Address
CV1	0x0000
P	0x0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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