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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series

Connecting a Pressure Sensor

Introduction

A pressure sensor is connected to an analog input pin, and the results of pressure measurements (unit: kPa abs) are displayed on 7-segment LEDs.

Target Device

H8/36014

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1. Specifications

1. Figure 1.1 shows the hardware configuration of an example of pressure sensor connection. As shown in the figure, the sensor is connected to analog input pin 0 (pin AN0).
2. A/D conversion of the AN0 pin input is performed, then the A/D conversion result is displayed on seven-segment LEDs connected to an I/O port.
3. The seven-segment LED displays show the 10-bit data of the A/D conversion result in decimal fraction.
4. The A/D conversion is performed every 0.49152 seconds.

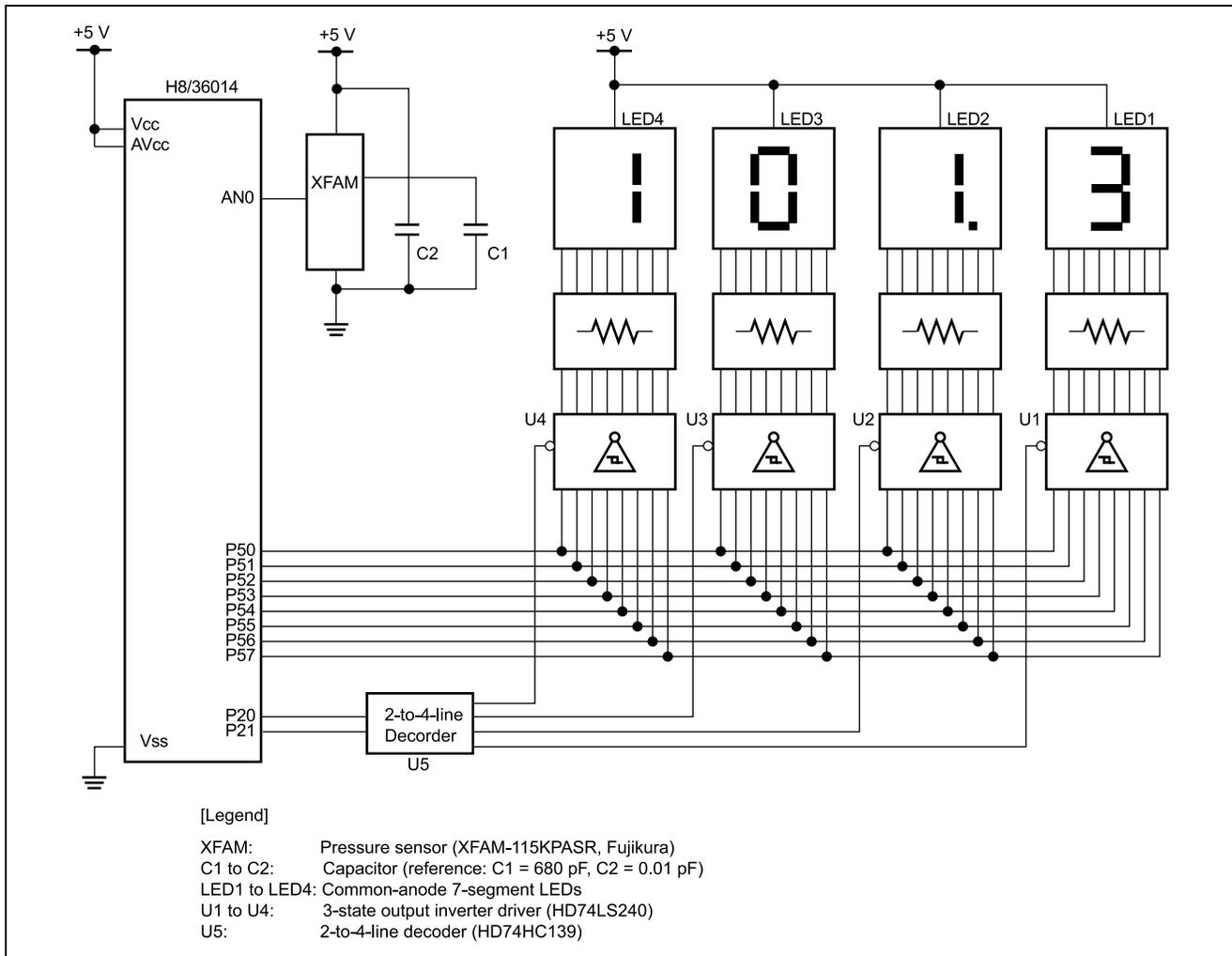


Figure 1.1 Hardware Configuration

5. In this sample task, the H8/36014 operating voltage (Vcc) and analog power supply voltage (AVcc) are 5.0 V, and the OSC clock frequency is 16 MHz.

6. The semiconductor-type pressure sensor used in this sample task is a single-chip integrated absolute pressure model manufactured by Fujikura (model no.: XFAM-115KPASR). Sensor specifications are shown below.
- A. Table 1.1 shows the specifications of this sensor.

Table 1.1 Specifications of Semiconductor-type Pressure Sensor

Item	Value	Units
Working conditions and recommended operating conditions		
Pressure type	absolute pressure	—
Rated pressure	115	kPa abs
Measurable pressure range	15 to 115	kPa abs
Pressure media	non-corrosive gas	—
Power supply voltage	5±0.25	VDC
Absolute maximum ratings		
Maximum load pressure	2 times the rated pressure	—
Maximum applied voltage	8	VDC
Operating temperature	−40 to 125	°C
Storage temperature	−40 to 125	°C
Operating humidity	30 to 80 (no condensation)	%RH
Electric performance (power supply voltage Vcc = 5.0 VDC, temperature Ta = 25°C)		
Current consumption	10 or less	mA
Output impedance	10 or less	Ω
Source current	0.2 or less	mA
Sink current	2 or less	mA
Response time	2 (ref. value)	msec
Output span voltage	4.5	V
Offset voltage*	0.2±0.1125	V
Full-scale voltage*	4.7±0.1125	V
Overall accuracy	±2.5	%FS/0 to 85°C

Note: * Varies with power supply voltage fluctuations. For details refer to figure 1.3.

B. Figure 1.2 shows a connection diagram.

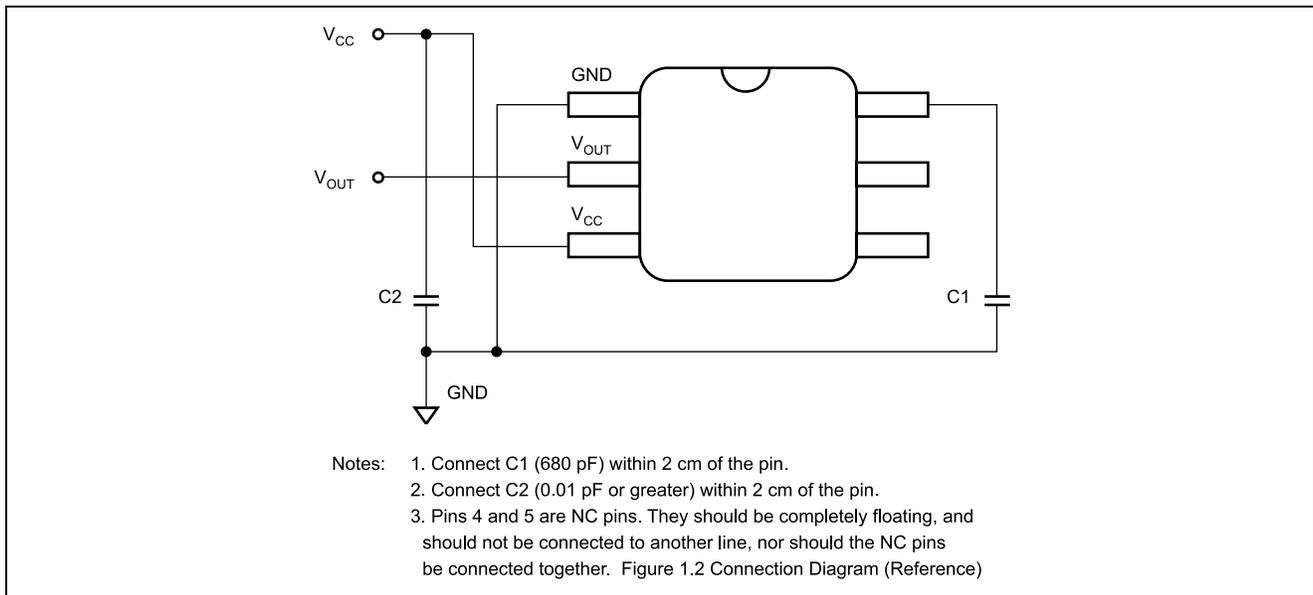


Figure 1.2 Connection Diagram (Reference)

C. Output characteristics are shown in figure 1.3. The full-scale voltage and the scale of the output voltage vary in proportion to the power supply voltage.

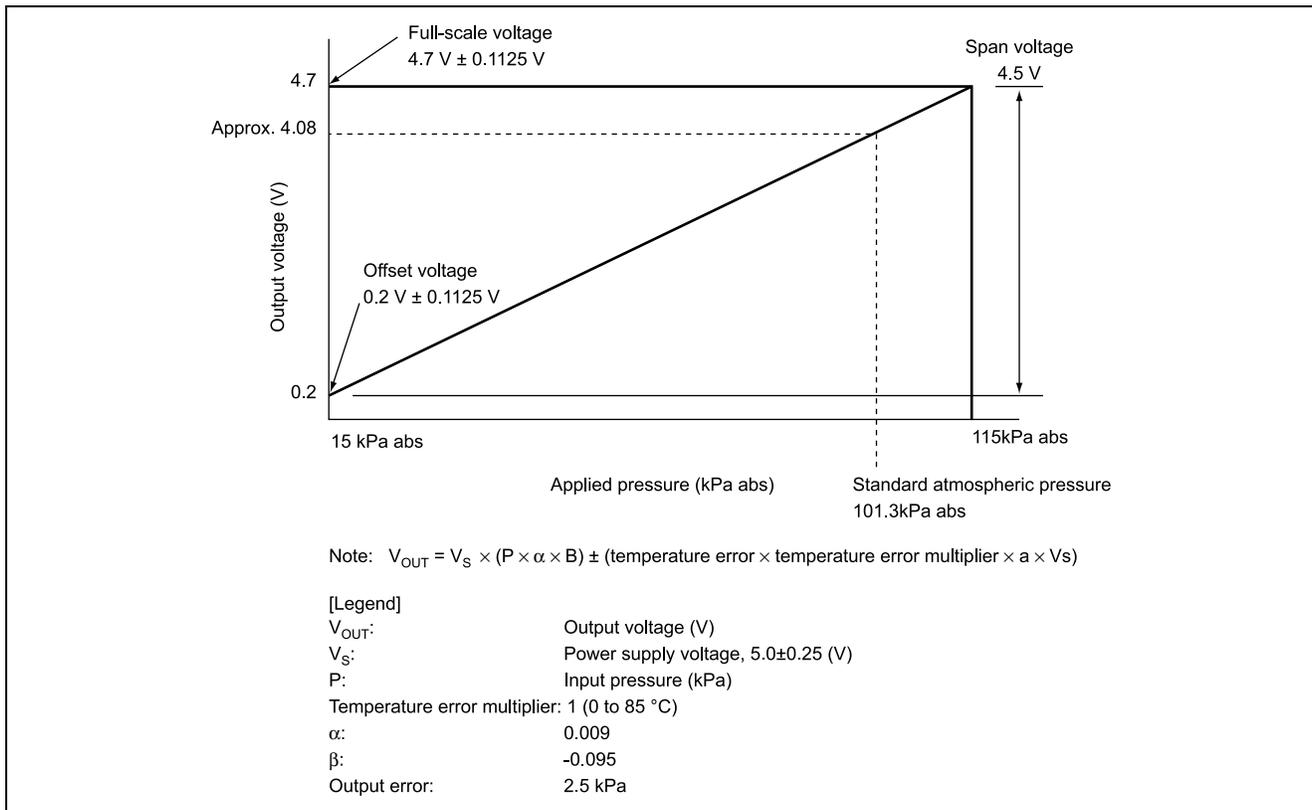


Figure 1.3 Output Characteristics (Reference)

7. Operation of this sample task is as follows:
 - A. The output voltage of 4.08 V, which is obtained under the standard atmospheric pressure with a power supply voltage of 5 V, is converted to 101.3 kPa abs.
 - B. The 7-segment LED display is "101.3" under the above conditions.

8. In this sample task, display on the 7-segment LED is handled by attaching port outputs from the microcontroller to the inputs to the tri-state-output inverter drivers (HD74LS240), the outputs from which are in turn connected to the cathodes of the 7-segment LEDs. The same eight port-output pins are used to control the display on each of the four 7-segment LEDs. The enable pins of the tri-state inverter driver control switching between the 7-segment displays. The signals used to switch between the displays are generated by a 2-to-4-line decoder (HD74HC139), which is controlled by two port-pin outputs. Figure 1.4 shows how the 7-segment LEDs are controlled.

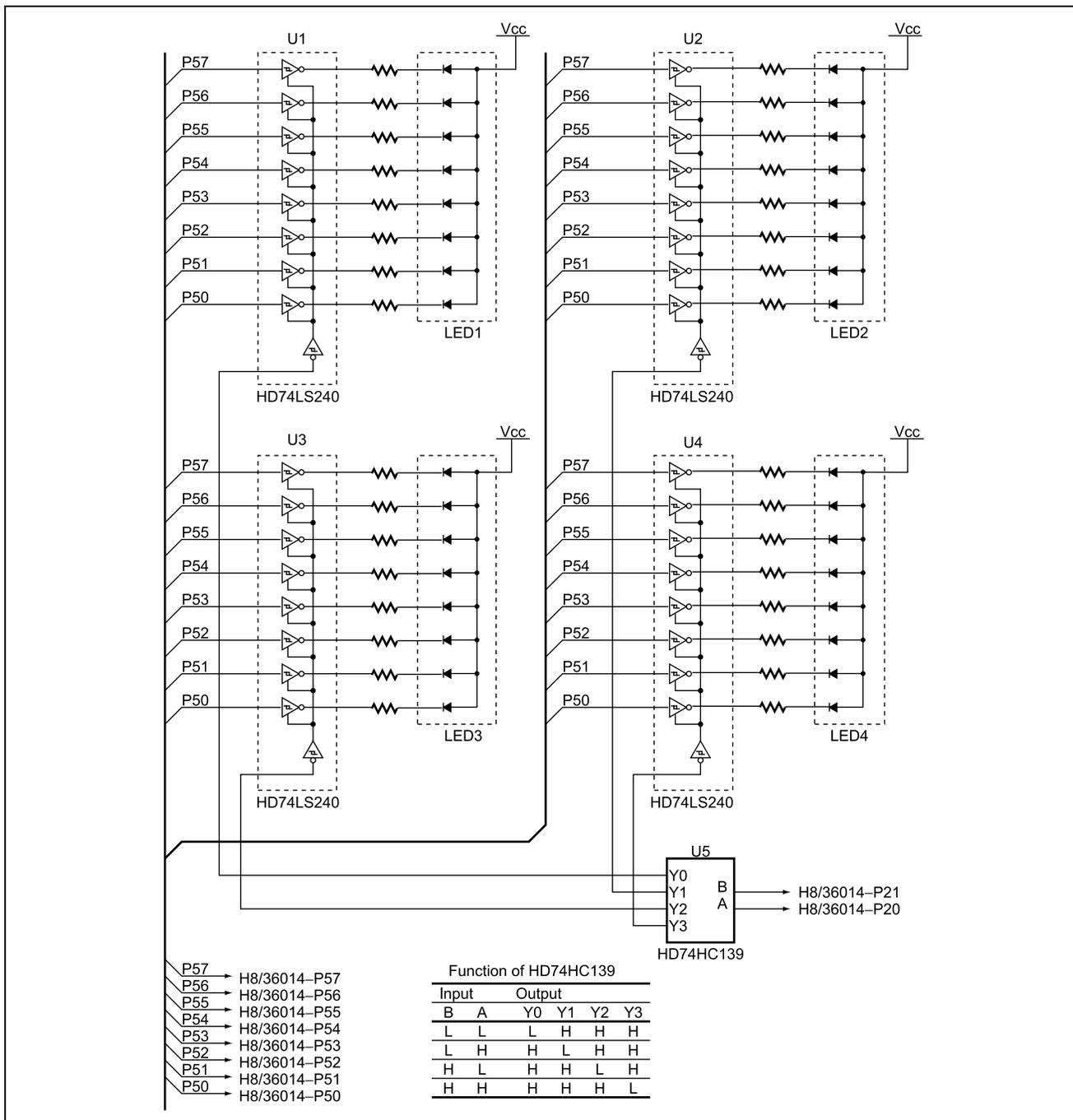


Figure 1.4 Control of Seven-Segment LEDs

9. In this sample task, the results of A/D conversion are displayed in decimal-fraction format (unit: kPa abs) on the 7-segment LEDs. Figure 1.5 shows how this is done.

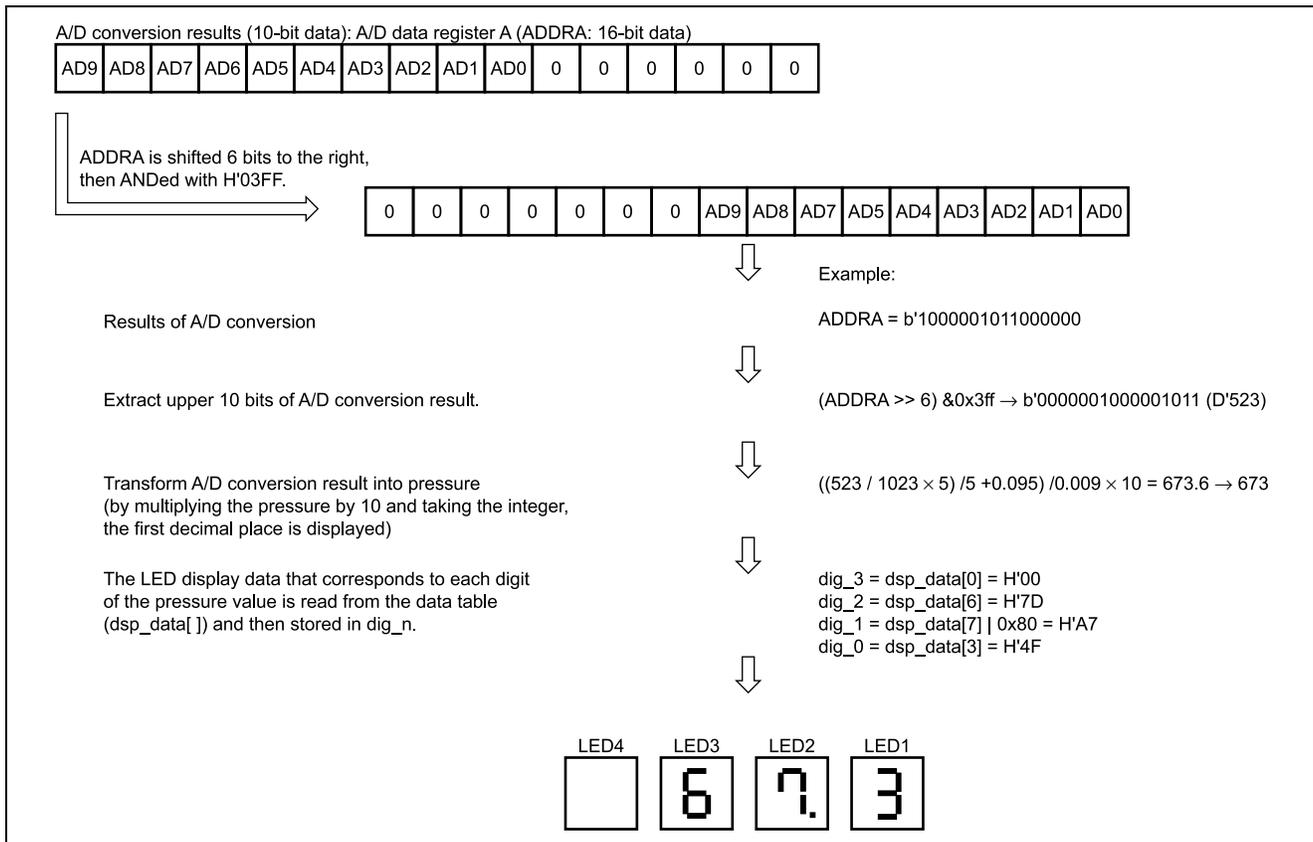


Figure 1.5 Acceleration value is displayed on the LEDs.

2. Description of Functions

1. Figure 2.1 is a block diagram of the H8/36014 functions used in this sample task; table 2.1 shows function allocations.

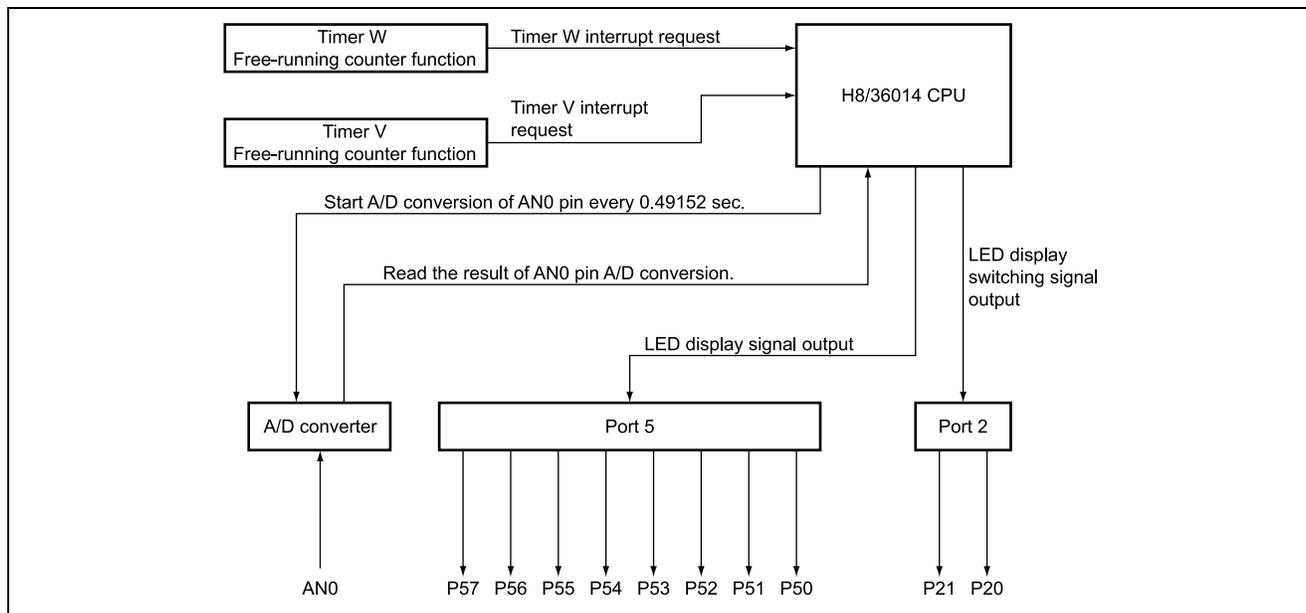


Figure 2.1 Block Diagram of Functions

Table 2.1 Function Allocation

Function Used	Function Allocation
Timer W	The timer W's free-running counter function is used to perform A/D conversion of the signal on the analog input pin 0 (AN0). The A/D conversion period is detected in terms of the timer W's overflow cycle of 32.768 ms.
Timer V	Timer V's free-running function is used to control switching of the 7-segment LED display. Each of the four 7-segment LEDs is lit in sequence at an interval of 2.048 ms, which is the time taken for timer V to overflow. This obtains dynamic illumination from the LEDs.
A/D converter	This unit A/D-converts the output voltage from the pressure sensor connected to analog input pin 0 (AN0) of the A/D converter.
Port 2	The active 7-segment LED display is switched by the P20 and P21 output pins of port 2. These pins are connected to the input/output pins of the 2-to-4-line decoder.
Port 5	The data for display on the currently active 7-segment LED is placed on the P50 to P57 output pins of port 5. The 10 bits of data produced by A/D conversion of the value on the AN0 pin are converted to 4-digit decimal fraction display data for output to the LEDs.

2. A diagram of the connection of the seven-segment LEDs used is shown in figure 2.2. As shown in the figure, by outputting "high" from port 5, the corresponding LED segments are lit. The relation between the port 5 outputs and the LED display data appears in table 2.2.

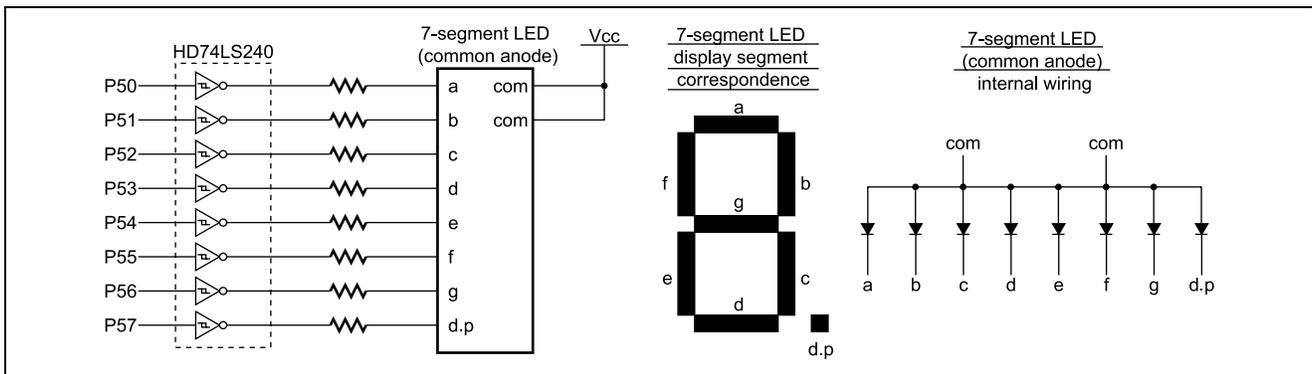
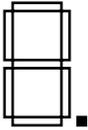
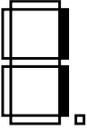
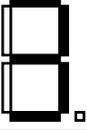
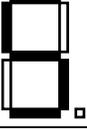
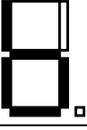
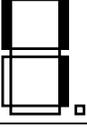
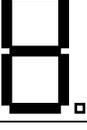
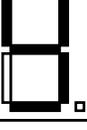


Figure 2.2 7-Segment LED Connection and Internal Wiring

Table 2.2 Relation between Port 5 Outputs and 7-Segment LED Display Data

LED Display	Port 5 Output Data								LED Display	Port 5 Output Data							
	P57	P56	P55	P54	P53	P52	P51	P50		P57	P56	P55	P54	P53	P52	P51	P50
	0	0	1	1	1	1	1	1		1	0	0	0	0	0	0	0
	0	0	0	0	0	1	1	0									
	0	1	0	1	1	0	1	1									
	0	1	0	0	1	1	1	1									
	0	1	1	0	0	1	1	0									
	0	1	1	0	1	1	0	1									
	0	1	1	1	1	1	0	1									
	0	0	1	0	0	1	1	1									
	0	1	1	1	1	1	1	1									
	0	1	1	0	1	1	1	1									

Note: For the first integer digit, display data is ORed with that for a decimal point.

3. Principles of Operation

- Figure 3.1 shows the principle of operation in the use of timer W and A/D conversion carried out on the AN0 pin. The A/D conversion interrupt is not used in this sample task. Instead, the time to start A/D conversion (0.49152 s) and completion of A/D conversion are detected by polling of the timer W overflow flag in the tmrw routine.

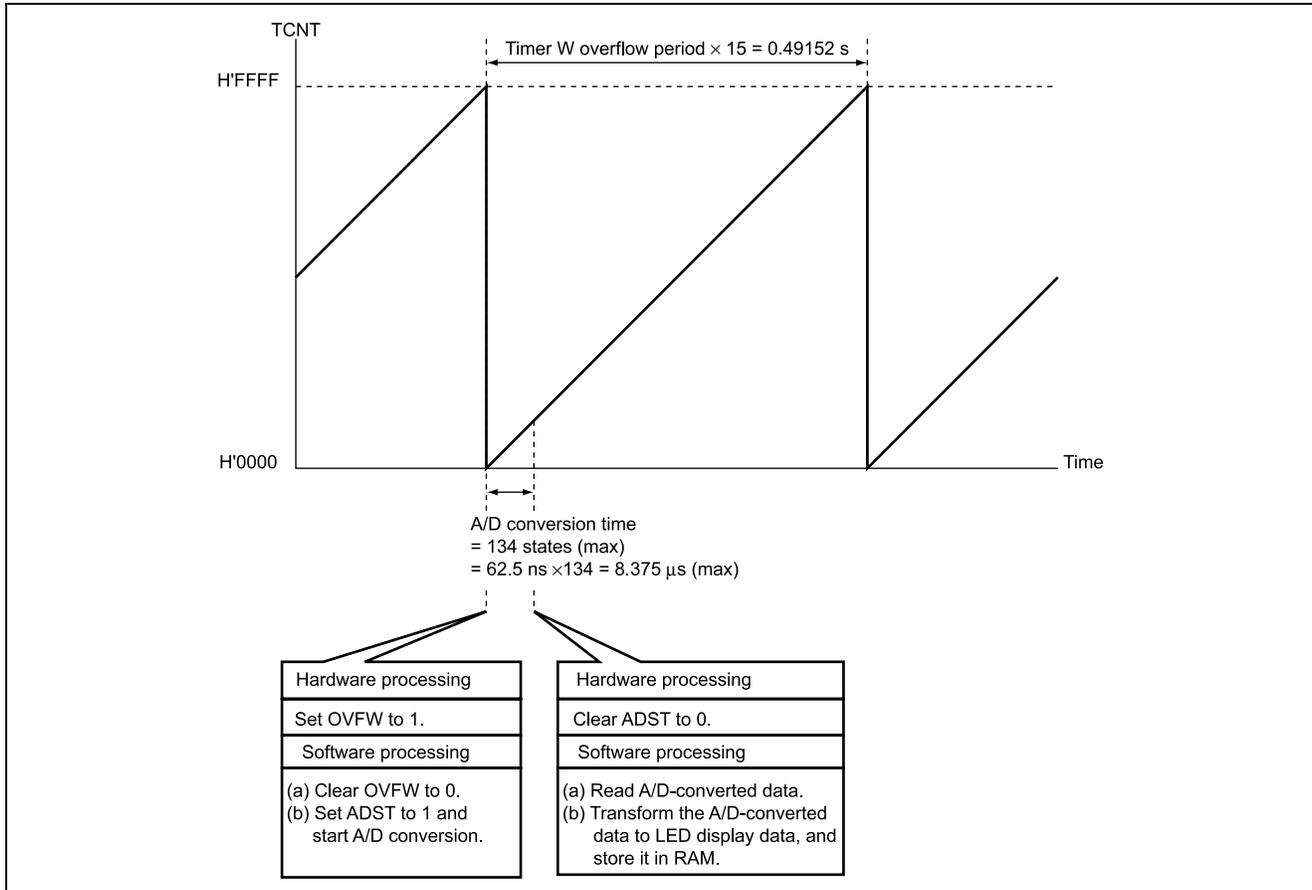


Figure 3.1 Principle of Operation of A/D Conversion of AN0-Pin Signal Using Timer W

2. The principle applied in controlling the 7-segment displays is explained below. Figure 3.2 depicts the situation where "67.3" is being displayed on LED4 to LED1. As the figure shows, the next display in sequence of LED1 to LED4 is lit up each time a timer-V overflow period elapses, creating a dynamic display on the 7-segment LED.

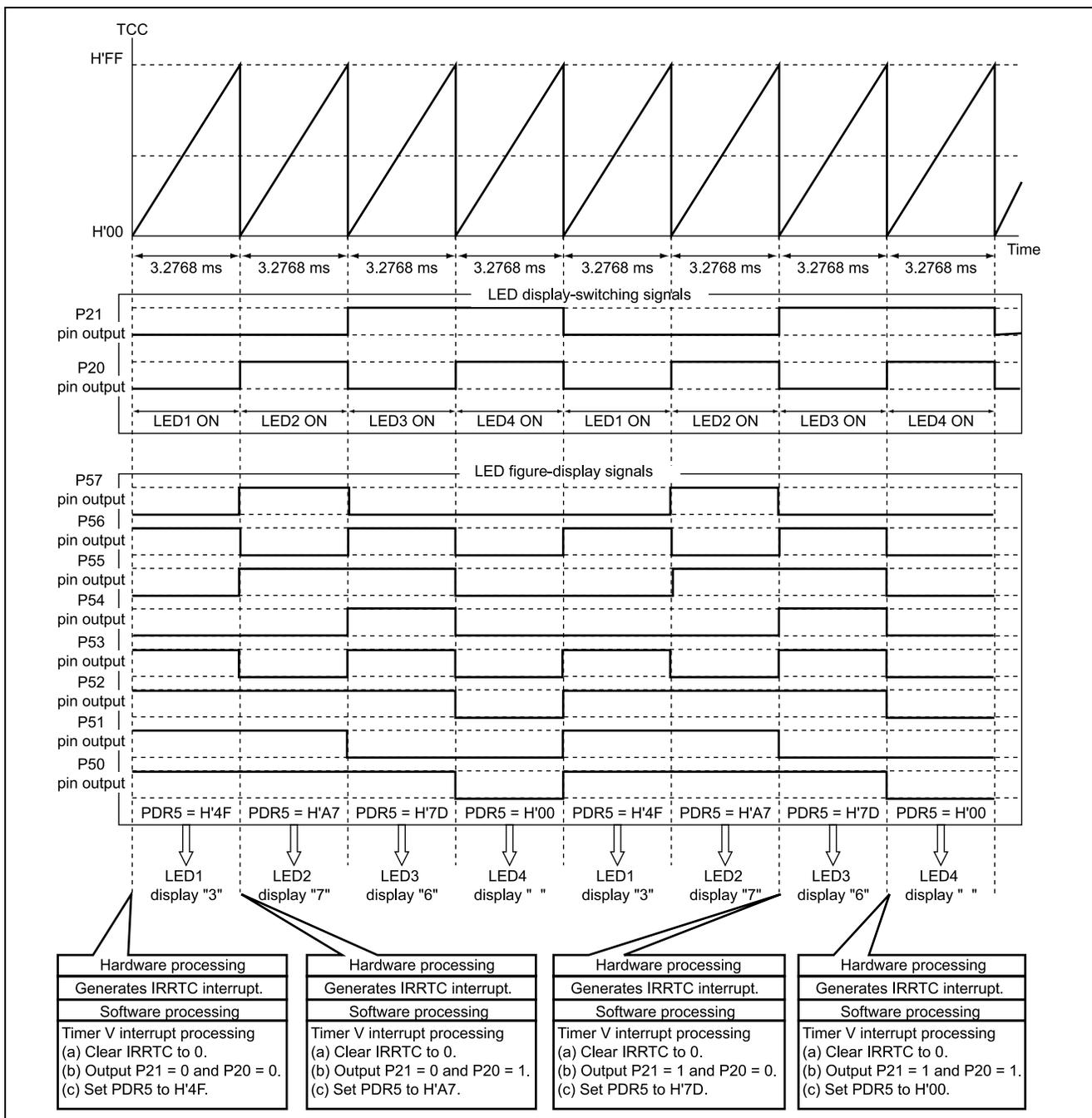


Figure 3.2 Principle of Operation for the 7-Segment LED Display Control

4. Description of Software

4.1 Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	Main	Makes initial settings and enables interrupts.
Timer W interrupt processing routine	Tmrw	Clears the interrupt flags, transforms A/D-converted data into LED-display data, and stores the result in RAM.
Timer V interrupt processing routine	Tmrv	Clears the interrupt flags and controls output of LED-display data and switching of display from LED to LED.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 4.2.

Table 4.2 Description of Internal Registers

Register Name	Function	Address	Setting
TCRV0	Timer control register V0 Selects TCNTV input clock, sets condition for clearing of TCNTV, and controls the individual timer V interrupt requests.	H'FFA0	H'03 (initial setting)
CMIEB	Compare Match Interrupt Enable B: When CMIEB = 0, interrupt requests on setting of the CMFB bit in TCSRv are disabled.	Bit 7	0
CMIEA	Compare Match Interrupt Enable A: When CMIEA = 0, interrupt requests on setting of the CMFA bit in TCSRv are disabled.	Bit 6	0
OVIE	Timer Overflow Interrupt Enable: When OVIE = 0, interrupt requests on setting of the OVF bit in TCSRv are disabled. When OVIE = 1, interrupt requests on setting of the OVF bit in TCSRv are enabled.	Bit 5	0/1
CCLR1	Counter Clear 1 and 0:	Bit 4	0
CCLR0	Sets the conditions for clearing of TCNTV. When CCLR1 = 0 and CCLR0 = 0 are both set, clearing of TCNTV is disabled.	Bit 3	0
CKS2	Clock Select 2 to 0:	Bit 2	0
CKS1	In combination with the ICKS0 bit of TCRV1, selects the clock	Bit 1	1
CKS0	signal for input to TCNTV and the condition to be counted. With CKS2 = 0, CKS1 = 1, CKS0 = 1 and ICKS0=1, counting by TCNTV is of the falling edges of the internal clock $\phi/128$.	Bit 0	1

Register Name	Function	Address	Setting
TCSR _V	Timer Control/Status Register V: Holds the overflow and compare-match status flags for timer V and controls output in response to a match.	H'FFA1	H'10
CMFB	Compare Match Flag B: When the values of TCNTV and TCORB match, CMFB is set to 1.	Bit 7	0
CMFA	Compare Match Flag A: When the values of TCNTV and TCORA match, CMFA is set to 1.	Bit 6	0
OVF	Timer Overflow Flag: When the value of TCNTV overflows, OVF is set to 1. This bit is cleared by reading it while it is set and then writing a 0 to it.	Bit 5	0
OS3	Output Select Bits 3 and 2:	Bit 3	0
OS2	Selects the output level on the TMOV pin in response to a match for compare-match B. When OS3 = 0 and OS2 = 0: No change	Bit 2	0
OS1	Output Select Bits 1 and 0:	Bit 1	0
OS0	Selects the output level on the TMOV pin in response to a match for compare-match A. When OS = 0 and OS0 = 0: No change	Bit 0	0
TCRV1	Timer Control Register V1: Selects the input edge of the TRGV pin, enables TRGV input, and selects the TCNTV input clock.	H'FFA5	H'E3
TVEG1	TRGV Input Edge Selects 1 and 0:	Bit 4	0
TVEG0	Selects the input edge of the TRGV pin. In this case TVEG1 = 0 and TVEG0 = 0, so trigger input from the TRGV pin is disabled.	Bit 3	0
TRGE	TRGV Input Enable: Enables and disables incrementing of TCNTV count on the edge input selected by TVEG1 and TVEG0. In this case TRGE = 0, so counting by TCNTV is not affected by the input to the TRGV pin.	Bit 2	0
ICKS0	Internal Clock Select 0: Selects the clock input to TCNTV and condition counted, in combination with the CKS2 to CKS0 bits of TCRV0. In this case CKS2=0, CKS1=1, CKS0=1 and ICKS0=1, so counting by TCNTV is of the falling edges of the internal clock $\phi/128$.	Bit 0	1
TMRW	Timer mode register W: Selects general register functions and the timer output mode.	H'FF80	H'80
CTS	Counter start: When CTS=1, indicates TCNT has started counting. When CTS=0, indicates TCNT has stopped counting.	Bit 7	1

Register Name	Function	Address	Setting
TCRW	Timer control register W: Selects the input clock for the counter and sets counter clearing conditions and the level of timer output.	H'FF81	H'30
CKS2	Clock select:	Bit 6	0
CKS1	When CKS2 = 0, CKS1 = 1 and CKS0 = 1, specifies the TCNT	Bit 5	1
CKS0	input clock as the system clock divided by 8.	Bit 4	1
TIERW	Timer interrupt enable register W: Controls timer W interrupt requests.	H'FF82	H'00 (at initial setting)
OVIE	Timer overflow interrupt enable: When OVIE = 0, disables interrupt requests by OVF. When OVIE = 1, enables interrupt requests by OVF.	Bit 7	0/1
TSRW	Timer status register W Indicates interrupt request statuses.	H'FF83	H'00
OVF	Timer overflow: When OVF=0, indicates TCNT has not overflowed When OVF=1, indicates that TCNT has overflowed.	Bit 7	0
TCNT	Timer counter: 16-bit upward counter which takes as input the system clock divided by 8.	H'FF86	H'00
ADCSR	A/D control/status register: Consists of A/D converter control bits and conversion status bits	H'FFB8	H'00 (initial setting)
ADF	A/D End Flag: On completion of A/D conversion in single mode, ADF is set to 1. Clear this bit by writing 0 to it after reading it as 1.	Bit 7	0
ADIE	A/D Interrupt Enable: When ADIE = 0, A/D Conversion End interrupt requests by the ADF are disabled.	Bit 6	0
ADST	A/D Start: Initiates A/D conversion by setting this bit to 1. This is automatically cleared to 0 on completion of A/D conversion in single mode.	Bit 5	0/1
SCAN	Scan Mode: When SCAN = 0, A/D conversion is in the single mode.	Bit 4	0
CKS	Clock Select: When CKS = 0, the A/D conversion period = 134 cycles (max.).	Bit 3	0
CH2	Channel Select Bits 2 to 0:	Bit 2	0
CH1	Select the analog input channel.	Bit 1	0
CH0	CH2 = 0, CH1 = 0 and CH0 = 0 (when SCAN = 0) are set to select AN0.	Bit 0	0

Register Name	Function	Address	Setting
ADCR	A/D Control Register: Enables the start of A/D conversion in response to an external trigger.	H'FFB9	H'7E
TRGE	Trigger Enable: When TRGE = 0, starting A/D conversion in response to edge input on an external trigger pin (ADTRG) is disabled.	Bit 7	0
ADDRA	A/D data register A: Stores the results of A/D conversion of the signal on AN0.	H'FFB0	—
PCR2	Port control register 2: Provides pin-by-pin control of input/output selection for the pins of port 2 that have been set as general purpose I/O pins. When PCR2=H'03, pin P22 functions as a general-purpose input pin, while P21 and P20 function as general-purpose output pins.	H'FFE5	H'03
PDR2	Port data register 2: General I/O port data register for port 2	H'FFD5	H'F8
PMR5	Port mode register 5: Sets the port 5 pin functions	H'FFE1	H'00
POF7	P57 pin function switching: POF7 = 0 selects the general-purpose I/O port function for P57.	Bit 7	0
POF6	P56 pin function switching: POF6 = 0 selects the general-purpose I/O port function for P56.	Bit 6	0
WKP5	P55/ $\overline{WKP5}$ /ADTRG Pin Function Switching: WKP5 = 0 selects the general-purpose I/O port function for P55.	Bit 5	0
WKP4	P54/ $\overline{WKP4}$ Pin Function Switching: WKP4 = 0 selects the general-purpose I/O port function for P54.	Bit 4	0
WKP3	P53/ $\overline{WKP3}$ Pin Function Switching: WKP3 = 0 selects the general-purpose I/O port function for P53.	Bit 3	0
WKP2	P52/ $\overline{WKP2}$ Pin Function Switching: WKP2 = 0 selects the general-purpose I/O port function for P52.	Bit 2	0
WKP1	P51/ $\overline{WKP1}$ Pin Function Switching: WKP1 = 0 selects the general-purpose I/O port function for P51.	Bit 1	0
WKP0	P50/ $\overline{WKP0}$ Pin Function Switching: WKP0 = 0 selects the general-purpose I/O port function for P50.	Bit 0	0
PUCR5	Port pull-up control register 5: Provides pin-by-pin control of the pull-up MOSFET for the pins of port 5 that have been set as inputs. When PUCR5 = H'00, the pull-up MOSFETs of the P55 to P50 pins are turned off.	H'FFD1	H'00
PDR5	Port data register 5: General I/O port data register for port 5	H'FFD8	H'00
PCR5	Port control register 5: Provides pin-by-pin control of input/output selection for the pins of port 2 that have been set as general purpose I/O pins. When PCR5=H'FF, the pins P57 to P50 function as general-purpose output pins.	H'FFE8	H'FF

4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name	Function	Address	Used in
dig_0	Stores LED1 display data. (1 byte)	H'FB8C	main, tmrw
dig_1	Stores LED2 display data. (1 byte)	H'FB8D	main, tmrw
dig_2	Stores LED3 display data. (1 byte)	H'FB8E	main, tmrw
dig_3	Stores LED4 display data. (1 byte)	H'FB8F	main, tmrw
cnt	8-bit counter used in switching display from LED1 to LED4. (1 byte)	H'FB90	main, tmrw
counter_sub	8-bit counter used for adjustment of A/D data acquisition intervals. (1 byte)	H'FB91	main, tmrw
convdat1	Coefficient for voltage conversion $\times 100$ (4 bytes)	H'FB80	main, tmrw
itemp	Area for temporary storage of calculated results (2 bytes)	H'FB84	tmrw
ftemp	Area for temporary storage of calculated results (4 bytes)	H'FB86	tmrw
ptr	Stores pointer to dig_0 (2 bytes)	H'FB8A	tmrv

4.5 Description of data table

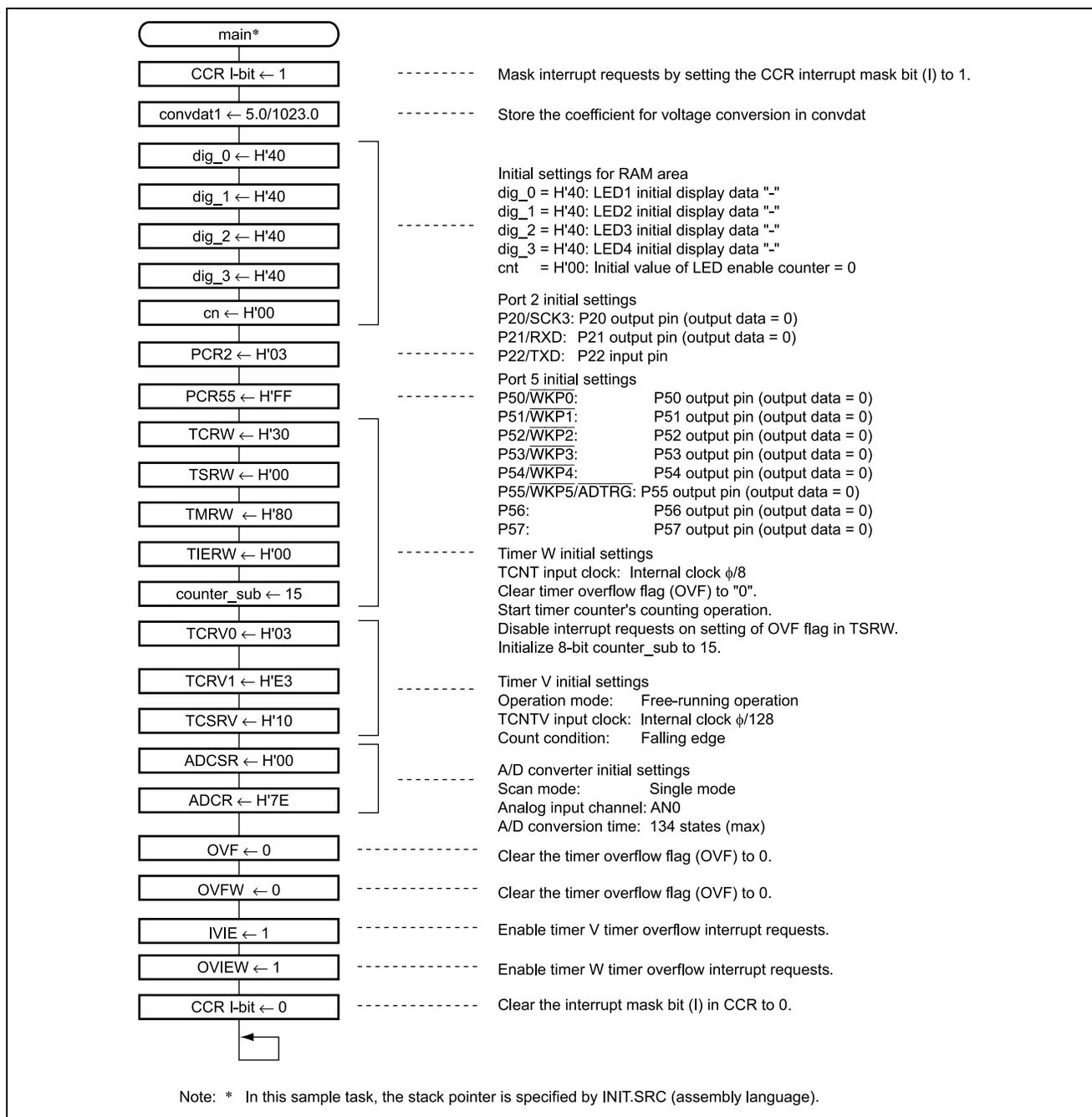
In this sample task, display data for the 7-segment LED displays are stored in the ROM as a 1-dimensional array (data table). Table 4.4 describes the data table of display data (dsp_data []).

Table 4.4 Description of 7-Segment LED Display Data Table (dsp_data[])

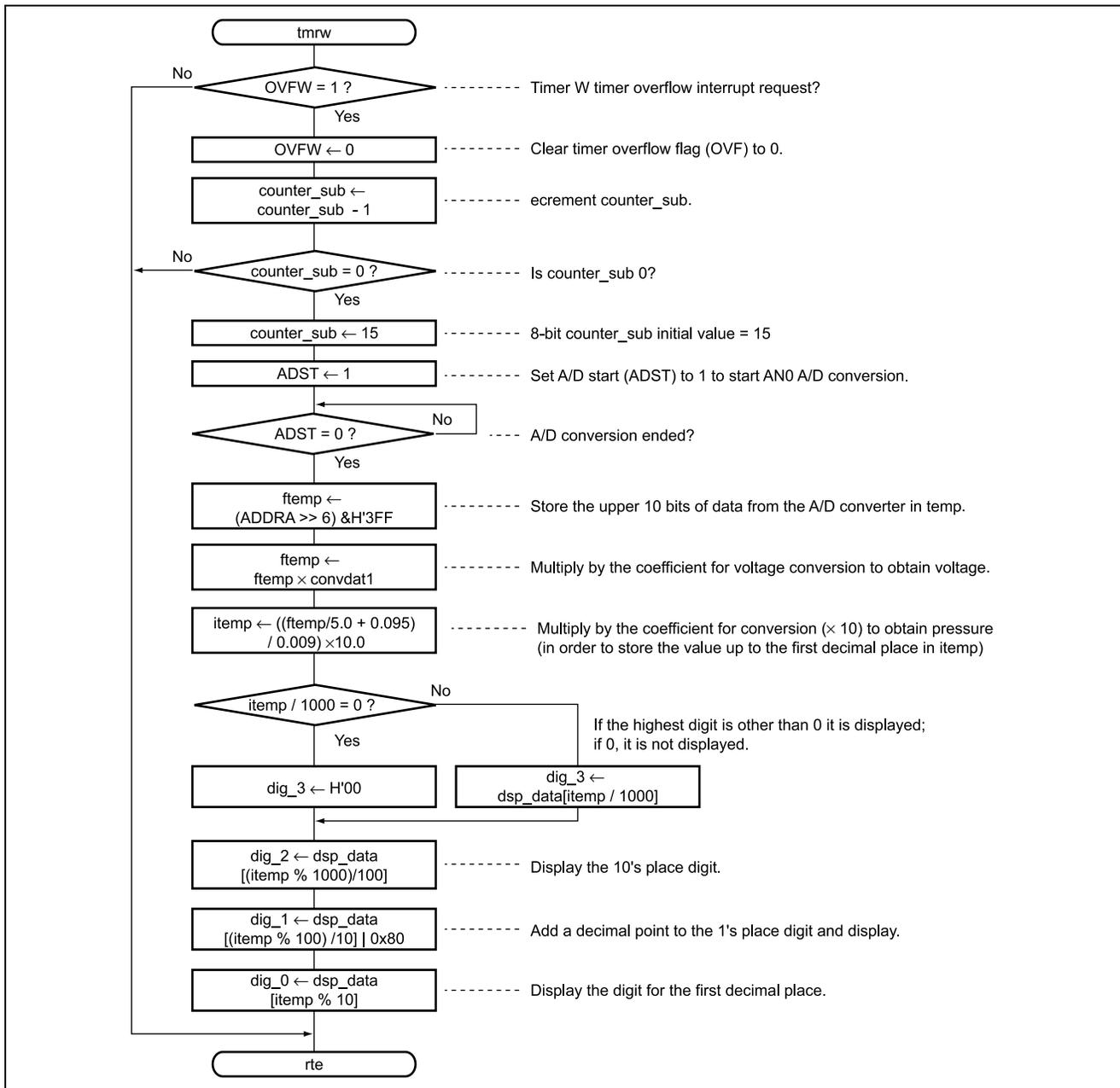
Array Name	Data	Data Description	Data Size	Address
dsp_data[0]	H'3F	Data output from port 5 to display "0" on an LED.	1 byte	H'0E06
dsp_data[1]	H'06	Data output from port 5 to display "1" on an LED.	1 byte	H'0E07
dsp_data[2]	H'5B	Data output from port 5 to display "2" on an LED.	1 byte	H'0E08
dsp_data[3]	H'4F	Data output from port 5 to display "3" on an LED.	1 byte	H'0E09
dsp_data[4]	H'66	Data output from port 5 to display "4" on an LED.	1 byte	H'0E0A
dsp_data[5]	H'6D	Data output from port 5 to display "5" on an LED.	1 byte	H'0E0B
dsp_data[6]	H'7D	Data output from port 5 to display "6" on an LED.	1 byte	H'0E0C
dsp_data[7]	H'27	Data output from port 5 to display "7" on an LED.	1 byte	H'0E0D
dsp_data[8]	H'7F	Data output from port 5 to display "8" on an LED.	1 byte	H'0E0E
dsp_data[9]	H'6F	Data output from port 5 to display "9" on an LED.	1 byte	H'0E0F

5. Flowchart

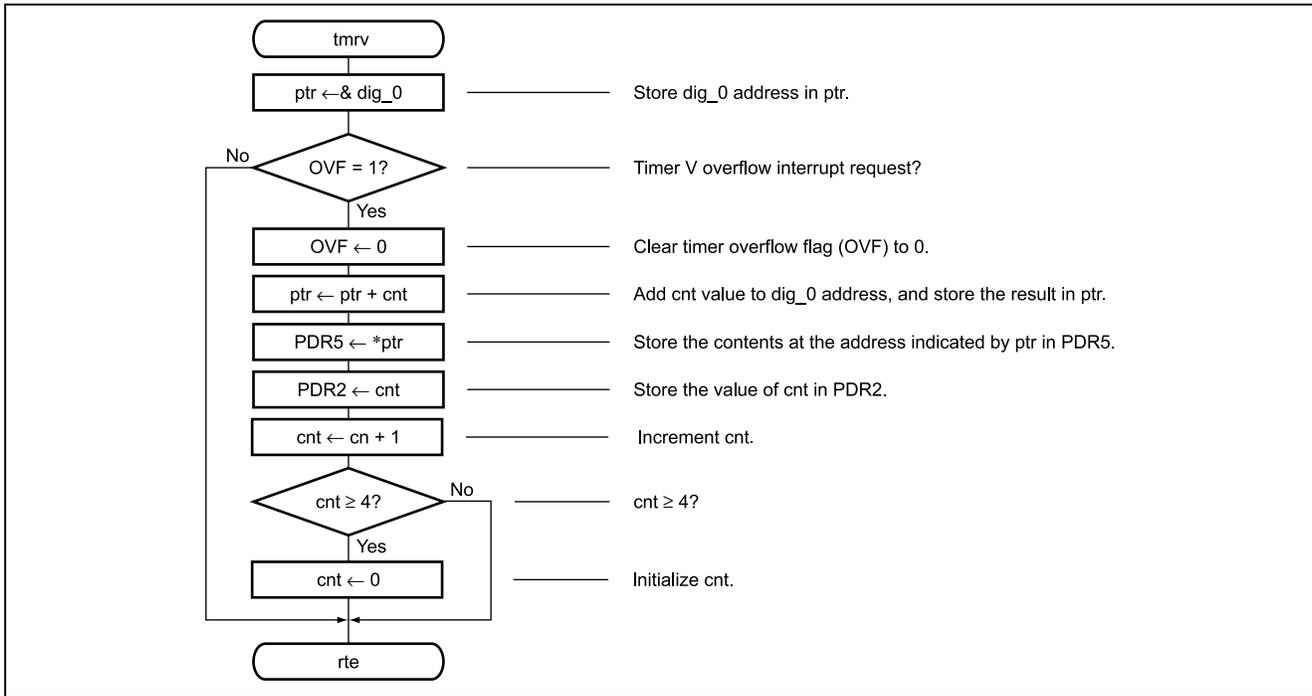
1. Main Routine (main)



2. Timer W Interrupt Processing Routine (tmrw)



3. Timer V Interrupt Processing Routine (tmrv)



6. Program Listing

INIT.SRC (program list)

```

.export  _INIT
.import  _main
;
.section P,CODE
_INIT:
mov.w   #'ff80,r7
ldc.b   #'10000000,ccr
jmp     @_main
;
.end

/* H8/300H tiny Series -H8/36014- Application note */
/* Application example */
/* Pressure measurement example */

#include <machine.h>

/* Symbol definition */
struct BIT {
    unsigned char b7:1; /* bit 7 */
    unsigned char b6:1; /* bit 6 */
    unsigned char b5:1; /* bit 5 */
    unsigned char b4:1; /* bit 4 */
    unsigned char b3:1; /* bit 3 */
    unsigned char b2:1; /* bit 2 */
    unsigned char b1:1; /* bit 1 */
    unsigned char b0:1; /* bit 0 */
};

#define PDR2      *(volatile unsigned char *)0xFFD5 /* Port data register 2 */
#define PCR2      *(volatile unsigned char *)0xFFE5 /* Port control register 2 */

#define PMR5      *(volatile unsigned char *)0xFFE1 /* Port mode register 5 */
#define PUCR5     *(volatile unsigned char *)0xFFD1 /* Port pull-up control register 5 */
#define PDR5      *(volatile unsigned char *)0xFFD8 /* Port data register 5 */
#define PCR5      *(volatile unsigned char *)0xFFE8 /* Port control register 5 */

#define TMRW      *(volatile unsigned char *)0xFF80 /* Timer mode register W */
#define TCRW      *(volatile unsigned char *)0xFF81 /* Timer control register W */
#define TCRW_BIT  (*(struct BIT *)0xFF81) /* Timer Control Register W */
#define TIERW     *(volatile unsigned char *)0xFF82 /* Timer interrupt enable register W */
#define TIERW_BIT (*(struct BIT *)0xFF82) /* Timer Interrupt Enable Register */
#define OVIEW     TIERW_BIT.b7 /* Timer Overflow Interrupt Enable W */
#define TSRW      *(volatile unsigned char *)0xFF83 /* Timer status register W */
#define TSRW_BIT  (*(struct BIT *)0xFF83) /* Timer Status Register W */
#define OVFW      TSRW_BIT.b7 /* Timer Over flow W */

#define TCRV0     *(volatile unsigned char *)0xFFA0 /* Timer control register V0 */
#define TCRV0_BIT (*(struct BIT *)0xFFA0)
#define OVIE      TCRV0_BIT.b5 /* Timer overflow interrupt enable */
#define TCSRW     *(volatile unsigned char *)0xFFA1 /* Timer control/status register V */
#define TCSRW_BIT (*(struct BIT *)0xFFA1)
#define OVF       TCSRW_BIT.b5 /* Timer overflow flag */
#define TCRV1     *(volatile unsigned char *)0xFFA5 /* Timer control register V1 */

```

```

#define ADCSR      *(volatile unsigned char *)0xFFB8          /* A/D control/status register      */
#define ADCSR_BIT  (*(struct BIT *)0xFFB8)
#define ADST       ADCSR_BIT.b5                             /* A/D start                        */
#define ADCR       *(volatile unsigned char *)0xFFB9          /* A/D control register             */
#define ADDR_A     *(volatile unsigned int *)0xFFB0           /* A/D data register A              */
#define ADDR_B     *(volatile unsigned int *)0xFFB2           /* A/D data register B              */
#define ADDR_C     *(volatile unsigned int *)0xFFB4           /* A/D data register C              */
#define ADDR_D     *(volatile unsigned int *)0xFFB6           /* A/D data register D              */

#pragma interrupt (tmrw)
#pragma interrupt (tmrv)

/* Function definition
extern void INIT(void);          /* Stack pointer set
void main(void);                /* main routine
void tmrw(void);                /* Timer W interrupt routine
void tmrv(void);                /* Timer V interrupt routine

/* Data table
const unsigned char dsp_data[10] =
{
0x3f,                            /* LED display data = "0"
    0x06,                            /* LED display data = "1"
    0x5b,                            /* LED display data = "2"
    0x4f,                            /* LED display data = "3"
    0x66,                            /* LED display data = "4"
    0x6d,                            /* LED display data = "5"
    0x7d,                            /* LED display data = "6"
    0x27,                            /* LED display data = "7"
    0x7f,                            /* LED display data = "8"
    0x6f,                            /* LED display data = "9"
};

/* RAM define
unsigned char dig_0;             /* Dig-0 LED display data store
unsigned char dig_1;             /* Dig-1 LED display data store
unsigned char dig_2;             /* Dig-2 LED display data store
unsigned char dig_3;             /* Dig-3 LED display data store
unsigned char cnt;               /* LED enable counter
unsigned char counter_sub;
float convdat1;                 /* Convert data (volt)
unsigned int itemp;
float ftemp;
unsigned char *ptr;             /* Pointer set

/* Vector address
#pragma section V1               /* Vector section set
void (*const VEC_TBL1[]) (void) = {
    INIT                          /* H'0000 Reset vector
};
#pragma section V2               /* Vector section set
void (*const VEC_TBL2[]) (void) = {
    tmrw                          /* H'002a Timer W interrupt vector
};
#pragma section V3               /* Vector section set
void (*const VEC_TBL3[]) (void) = {
    tmrv                          /* H'002c Timer V interrupt vector
};
#pragma section                  /* P

```

```

/*****
/* Main program */
*****/
void main(void)
{
set_imask_ccr(1); /* CCR I-bit = 1 */
convdat1 = 5.0 / 1023.0; /* Set convert constant 1 */

dig_0 = 0x40; /* Used RAM area initialize */
dig_1 = 0x40; /* Used RAM area initialize */
dig_2 = 0x40; /* Used RAM area initialize */
dig_3 = 0x40; /* Used RAM area initialize */
cnt = 0x00; /* Used RAM area initialize */

PCR2 = 0x03; /* Port 2 initialize */

PCR5 = 0xff; /* Port 5 initialize */

TCRW = 0x30; /* Timer W initialize */
TSRW = 0x00; /* Clock Select */
TMRW = 0x80; /* Clear OVF */
TIERW = 0x00; /* Timer Counter Count Start */
counter_sub = 15; /* OVF Interrupt Disable */
/* Initialize 8bit Counter_sub */

TCRV0 = 0x03; /* Timer V initialize */
TCRV1 = 0xe3; /* Internal clock select */
TCSRv = 0x10; /* Clear OVF to 0 */

ADCSR = 0x00; /* A/D converter initialize */
ADCR = 0x7e;

OVF = 0; /* Clear OVF to 0 */
OVFW = 0; /* Clear OVF to 0 */
OVIE = 1; /* Timer V OVF interrupt enable */
OVIEW = 1; /* Timer W OVF interrupt enable */

set_imask_ccr(0); /* CCR I-bit = 0 */

while(1);
}

```

```

/*****
/*   Timer W Interrupt
/*****
void tmrw(void)
{
if ( OVFW == 1 ) {
    OVFW = 0;
    counter_sub--;
    if ( counter_sub == 0x00 ){
        counter_sub = 15;
        ADST = 1;
        while(ADST == 1);
        ftemp = (ADDRA >> 6) & 0x3ff;

        ftemp = ftemp * convdat1;

        itemp = ((ftemp / 5.0 + 0.095) / 0.009) * 10.0;

        if (itemp/1000 == 0) {
            dig_3 = 0x00;
        } else {
            dig_3 = dsp_data[itemp / 1000];
        }
        if (itemp/100 == 0) {
            dig_2 = 0x00;
        } else {
            dig_2 = dsp_data[(itemp % 1000) / 100];
        }
        dig_1 = dsp_data[(itemp % 100) / 10] | 0x80;
        dig_0 = dsp_data[itemp % 10];
    }
}

/*****
/*   Timer V Interrupt
/*****
void tmrv(void)
{
    ptr = &dig_0;

    while(OVF == 1){
        OVF = 0;
        ptr += cnt;
        PDR5 = *ptr;
        PDR2 = cnt;
        cnt++;
        if (cnt >= 4){
            cnt = 0;
        }
    }
}

```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.29.03	—	First edition issued

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