Choosing a Crystal for VersaClock® 7 Devices

This application note describes the crystal specifications requirements of VersaClock 7 devices. A list of recommended crystals and their vendors is also provided.

Contents

1. Introduction

The VersaClock 7 RC310xx/RC210xx family relies on a crystal as the reference to the analog PLL. To achieve optimum performance for a given application, the selection of the crystal must consider the nature of the application as well as the specifications of the devices. For more details on the requirements for selecting a crystal for timing applications, see the Choosing the Right Crystal for Clocking Devices application note. This application note describes the requirements for selecting a crystal for the RC210xx and RC310xx family of devices.

2. VersaClock 7 External Crystal Characteristics

Table 1 shows the specifications for the external crystal characteristics of the VersaClock 7 family of devices. To ensure stable operation of the crystal oscillator circuitry of the device, choose a crystal with specifications that fall within the requirements of the device.

Table 1. External Crystal Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
-	Resonance Mode	-	Fundamental			-
f_{INXTAL} [1]	Crystal input frequency	Fundamental mode	8	-	80	MHz

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
ESR [1]	Equivalent Series Resistance	8MHz ≤ f_{INXTAL} ≤ 12MHz, C_L = 12pF	-	-	120	Ω
		12MHz ≤ f_{INXTAL} ≤ 28MHz, C_L = 12pF	-	-	80	
		28MHz ≤ f_{INXTAL} ≤ 54MHz, C_L = 12pF	-	-	50	
		54MHz ≤ f_{INXTAL} ≤ 80MHz, C_L = 8pF	-	-	50	
C_O [1]	Shunt Capacitance	-	-	7	-	pF
C_L [1]	Load Capacitance	-	6	8	12	
Drive [1]	Drive Level	-	-	-	100	µW
F_{TOL}	Frequency Tolerance	Center frequency at 25ºC	-	-	[2]	ppm
F_{STAB}	Frequency Stability	Over operating temperature range with respect to F_{TOL}.	-	-		
Aging	Per Year	-	-	-		

1. These parameters are required regardless of the crystal used.
2. These parameters are customer/application dependent. Common maximum values are F_{TOL} = ±20ppm, and Aging = ±5ppm/10years. These parameters can be adjusted to meet particular requirements.

3. Load Capacitance

For VersaClock 7, Renesas recommends using a crystal that has a nominal load capacitance between 6pF and 12pF. VersaClock 7 does not use external tuning capacitors, but instead uses an internal, adjustable load capacitance. The internal load capacitance can be adjusted in the programmed configuration file or via register writes to the device.

The total load capacitance can be modeled as seen in Figure 1, where C_{pcb1} and C_{pcb2} are the stray capacitance of the circuit board, C_{f1} and C_{f2} are the fixed capacitance internal to VersaClock 7 on each leg of the oscillator, and C_{d1} and C_{d2} are the internal tuning caps (digicaps) of the VersaClock 7 device. For all capacitances, C_{xx1} refers to capacitances on the XIN_REFIN pin and C_{xx2} refers to capacitances on the XOUT_REFINB pin.

The load capacitance (C_L) for the XIN pin is:

$$C_L = \frac{1}{\frac{1}{C_{totalXIN}} + \frac{1}{C_{totalXOUT}}}$$

where,

$$C_{totalXIN} = C_{f1} + C_{d1} + C_{pcb1}$$

$$C_{totalXOUT} = C_{f2} + C_{d2} + C_{pcb2}$$

The fixed internal capacitance for VersaClock 7 devices is, C_{f1} = C_{f2} = 5.5pF. The fixed capacitance is always present. For Renesas VersaClock 7 evaluation boards it is assumed that C_{pcb1} = C_{pcb2} = 1.7pF RCx1008B boards and C_{pcb1} = C_{pcb2} = 2.5pF RCx1012B boards. The circuit board stray capacitance values can be manually changed by setting the values of **xin_pcb_capacitance** and **xout_pcb_capacitance** in the RICBox GUI.

For VersaClock 7, the capacitance of the internal tuning capacitor for XIN can be controlled via the **TOP.XO.XO_CNFG.en_cap_x1** register and the capacitance of the internal tuning capacitor for XOUT can be controlled via the **TOP.XO.XO_CNFG.en_cap_x2** register. Note, the values of **TOP.XO.XO_CNFG.en_cap_x1** and **TOP.XO.XO_CNFG.en_cap_x2** are each a combination of the fixed capacitance and the internal tuning capacitance for each leg on the crystal.

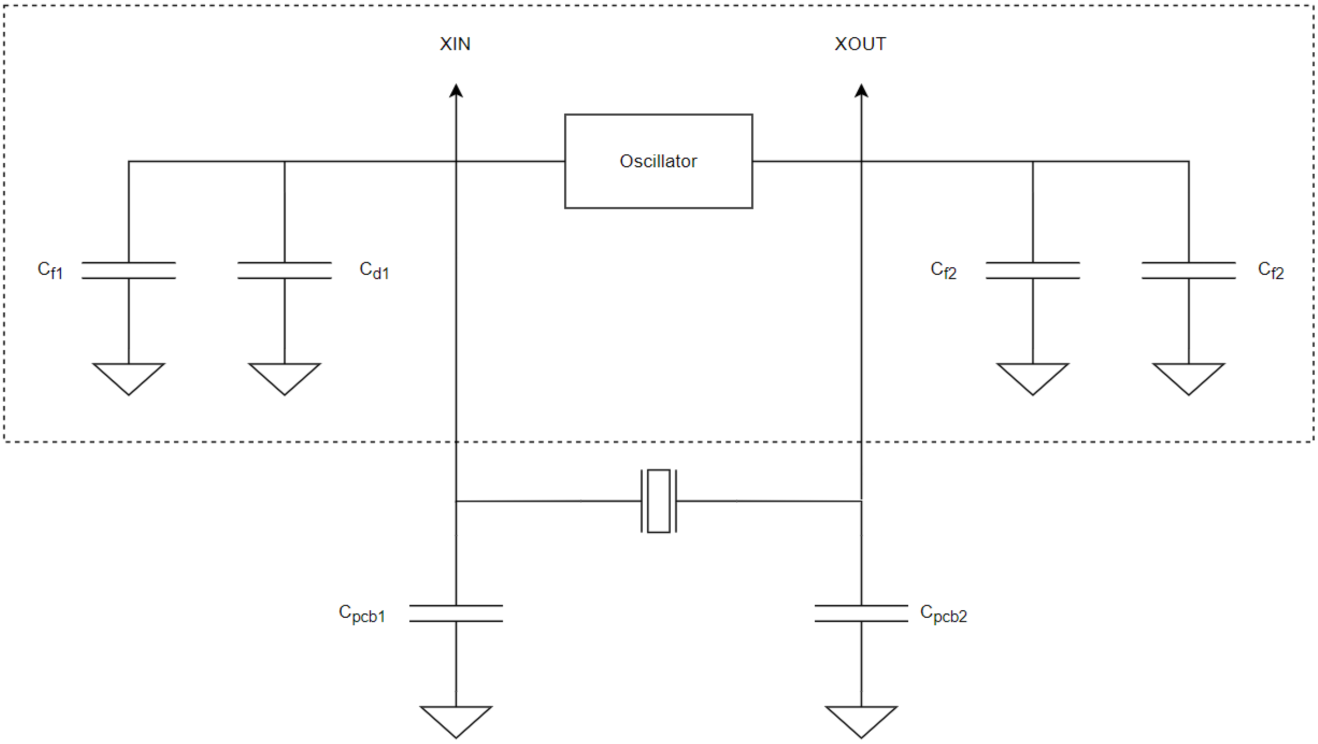

Figure 1: Crystal Capacitance

4. Equivalent Series Resistance

Equivalent series resistance (ESR) is the effective resistance component in series with the LC model of the crystal itself. ESR is determined by the crystal size, cut, frequency, and mode of vibration. ESR subtracts from the negative resistance in the oscillator. A small package with a very small crystal may have too high an ESR for the driver, making it harder to start and sustain oscillation. A large package can fit a larger crystal (at the same cut, mode, and frequency) and will have a lower ESR.

ESR is proportional to the motional resistance (R_M) of the crystal and the shunt capacitance (C_O). It is also inversely proportional to the load capacitance (C_L). The ESR can be calculated as follows:

$$ESR = R_M\left(1 + \frac{C_O}{C_L}\right)^2$$

ESR is commonly expressed as a maximum value in ohms and is significant for two reasons.

1. The loop gain needed for an oscillator to start up and maintain oscillation is proportional to the ESR.
2. The drive level of an oscillator is proportional to the ESR. Therefore, if the ESR is too large, the crystal can have trouble oscillating or it can lead to a drive level which exceeds the rating that accelerates aging.

For VersaClock 7 devices, the maximum ESR value that is recommended varies with crystal frequency and load capacitance (refer to Table 1).

5. Using a Crystal Oscillator (XO) with VersaClock 7

A crystal oscillator (XO) can be used in place of a crystal with VersaClock 7. To use a XO with VersaClock7, the XIN_REFIN input must be overdriven. The XIN_REFIN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V, and the slew rate must be ≥0.2V/ns. For 1.2V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 2. For LVCMOS drivers with > 1.2V swing, the amplitude must be reduced from full swing to at least 1.2V to prevent signal interference with the power rail. The sum of the driver output impedance and Rs must equal the transmission line impedance to prevent overshoot and undershoot.

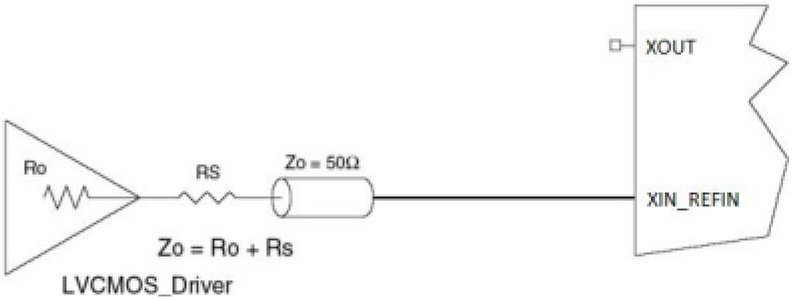

Figure 2. 1.2V LVCMOS Driver to XTAL Input Interface

Figure 3 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equal the transmission line impedance. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. We also need to scale the 3.3V LVCMOS swing to 1.2V (~1/3 of the swing). This yields R1 = 2 x R2 while R1 || R2 = 50Ω. Solving for a 50Ω ohm system gives R1 = 150Ω and R2 = 75Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Different scaling factors are required for 2.5V and 1.8V LVCMOS drivers.

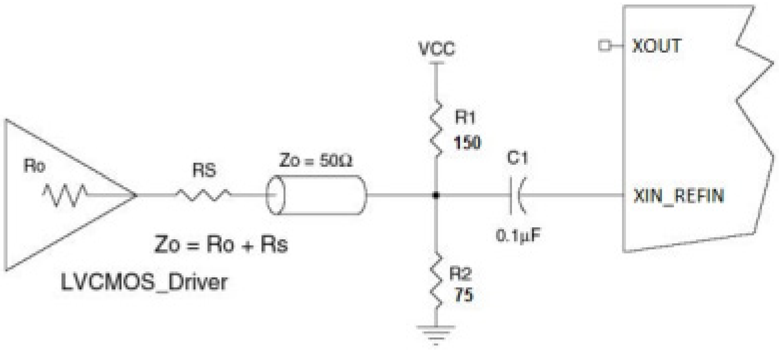

Figure 3. LVCMOS Driver to XTAL Input Interface

Figure 4 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN_REFIN input. Renesas recommends that all components in the schematics be placed in the layout. Though some components may not be used by the application, they can be used for debugging purposes.

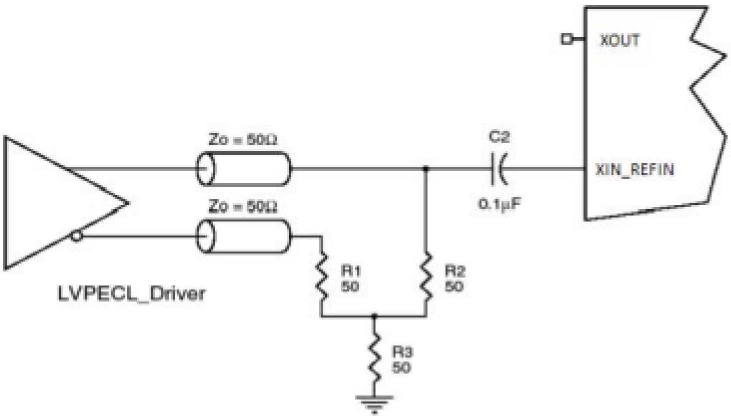

Figure 4. LVPECL Driver to XTAL Input Interface

6. Drive Level

Confirm that the crystal maximum specified drive level will accommodate the drive level of the VersaClock 7 product. For VersaClock 7 devices, the maximum recommended crystal drive level is 100µW. To prevent exceeding the drive level of the crystal, a series-damping resistor (R_S) can be added, but this series resistor will decrease the negative resistance and loop gain will increase phase noise. It is preferred to select a crystal that can tolerate the required drive strength. Adding an R_S, populated with a 0-ohm shunt allows the use of a series resistance if a suitable crystal cannot be sourced.

Exceeding the drive level on the crystal accelerates aging. Renesas recommends measuring the power dissipated in the crystal to ensure it is below the crystal maximum specification. For more information, see the Quartz Crystal Drive Level Application Note.

R_S should be a small surface mounted part (example 0201 or 0402) to minimize stray capacitance.

7. Operating Temperature

Operating a crystal outside of its specified operating temperature range may prematurely age the crystal (increased ppm frequency change over time) or may damage the housing. A crystal operating outside of its temperature range can result in higher jitter frequency offset caused by the temperature. Crystal performance is typically not guaranteed beyond its specified temperature range. The recommended operating temperature range for VersaClock 7 devices is -40°C to 85°C.

8. Frequency Tolerance

Select a manufacturing tolerance (maximum deviation from the specified resonant frequency at room temperature) and frequency shift over the operating temperature range (often called frequency stability) that is acceptable for the application. When tight frequency tolerances (< 10ppm) over the operating temperature range are a requirement, it may be necessary to use a TCXO (temperature compensated crystal oscillator) or OCXO (oven-controlled crystal oscillator) instead.

Note: For VersaClock 7 products, the crystal or crystal oscillator at XIN is the jitter reference. The preference is to use a crystal for low jitter instead of a generated clock signal.

9. Aging

Confirm that the crystal aging tolerance (ppm per year) meets the application requirement. Exceeding the drive level on the crystal, as well as shock, vibration and operating the crystal outside of its specified temperature range, accelerates aging. If the crystal will experience shock or vibration in its application, consider an oven-controlled SC-cut crystal that is more tolerant of vibration.

10. List of Acceptable Crystals

Table 2 provides a list of crystals that would be acceptable for applications using a VersaClock 7 device. The selection of the crystal frequency will depend on the application. For a clock synthesizer with outputs set at 100MHz, a 50MHz crystal would be recommended.

Table 2. Acceptable Crystals for VersaClock 7 Applications

Manufacturer	Part Number	Frequency (MHz)	ESR (Ω)	C_L (pF)	Drive Level Rating (µW)	Frequency Tolerance (ppm)	Frequency Stability (ppm)	Aging (ppm/year at 25°C)	Temp Range (°C)
Specification	**-**	**8–80**	**50** **(f>28MHz)**	**8–12**	**100**	**-**	**-**	**-**	**-40 to 85**
NDK	NX2016SA-80M	80	50	8	200	±15	±50	±3	-40 to 125
NDK	NX2016SA-50M	50	50	8	200	±15	±15	±3	-40 to 125
TXC [1]	8Y80072011	80	40	8	300	-5 to 12	-15 to 12	±1	-40 to 85
TXC [1]	8Y78172002	78.125	40	8	300	-5 to 12	-15 to 12	±1	-40 to 85
TXC [1]	8Y73072002	73	40	8	300	-5 to 12	-15 to 12	±1	-40 to 85
TXC [1]	8Y68072001	68	40	8	300	-5 to 12	-15 to 12	±1	-40 to 85
TXC [1]	8Y62572002	62.5	40	8	300	-5 to 12	-15 to 12	±1	-40 to 85
TXC [1]	8Y60072005	60	40	8	300	-5 to 12	-15 to 12	±1	-40 to 85
TXC [1]	7M54072002	54	50	8	100	±12	±15	±3	-40 to 85
TXC [1]	7M50070021	50	50	10	200	±15	±20	±3	-40 to 85
Abracon	ABM11W-50.0000MHZ-8-R50-D3Y-T3	50	50	8	100	±25	±30	±2	-40 to 85
Raltron	RH100-50.000-8-F-2030-EXT-TR	50	50	8	200	±20	±30	±2	-40 to 85
KYOCERA	CX3225SB54000	54	50	8	100	±10	±15	±1	-30 to 85
KYOCERA	CX2016SA50000	50	50	8	200	±15	±50	-	-40 to 125
ECS	ECS-500-8-37-AGN-TR	50	50	8	100	±25	±30	±5	-40 to 85
Taitien	XXDBPLNANF-40.000000	40	50	12	200	±10	±15	±3	-40 to 85
Taitien	XXCCCLNANF-49.152000	49.152	50	10	200	±20	±20	±3	-40 to 85
Taitien	XXCBPLNANF-50.000000	50	50	10	200	±10	±15	±3	-40 to 85

[1] Can be ordered directly from the vendor.

11. Revision History

Revision	Date	Description
1.03	Oct 13, 2025	▪ Added section Load Capacitance ▪ Added section Equivalent Series Resistance ▪ Added section Using a Crystal Oscillator (XO) with VersaClock 7 ▪ Added section Drive Level ▪ Added section Operating Temperature ▪ Added section Frequency Tolerance ▪ Added section Aging
1.02	May 26, 2023	Removed “A” from the referenced RC310xx and RC210xx part numbers.
1.01	May 24, 2023	Updated list of acceptable crystals in Table 2.
1.00	Nov 4, 2022	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2026 Renesas Electronics Corporation. All rights reserved.