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April 1st, 2010
Renesas Electronics Corporation

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H8/300L

Boot mode In-circuit Programming (Boot)

Introduction

The Renesas Flash Development Toolkit (FDT) is an onboard flash programming tool with user-friendly Graphical User Interface (GUI) for Renesas F-ZTAT (Flash Zero Turn Around Time) microcomputers. To shorten the development cycle, especially on re-programming time of the mounted flash micon, it becomes essential to incorporate onboard programming feature onto the target board. This application note describes the hardware requirements for the H8/38024 flash micon in boot mode using FDT.

Target Device

H8/300L Super Low Power (SLP) Series - H8/38024F

Contents

1. Overview

HD64F38024 micon has a 32-kbytes built-in flash memory. Onboard programming/erasing can be done in boot mode, in which the boot program built into the chip is started to erase or program of the entire flash memory.

Renesas Flash Development Toolkit (FDT) is an onboard programming GUI software, which connects the target board to the Host PC. This target board is mounted with HD64F38024 micon and built with onboard programming circuitry. The boot mode programming is achieved via SCI3 channel in asynchronous mode.

1.1 Boot Mode & Micro Kernel

Boot Mode conditions the internal FLASH circuitry and initiates an Auto Bootload sequence at RESET for programming/erasing the entire flash memory. Once the chip is set to boot mode, it will run a protected section of code known as the boot code. First, boot code negotiates a bit rate for an asynchronous serial connection (SCI3) with the host. Next, the boot code downloads the Micro Kernel (µKernel) at 9600 bps from the FDT software running on host PC.

µKernel in FDT is responsible for initialising the device, particularly to set up a valid stack pointer, enable flash memory and configure the required communication ports. It also downloads the FDT Main Kernel, which interfaces with the write, read, erase and blank check modules at 38400 bps for flash operations. The design of FDT is based on a split kernel approach.

In boot mode, µKernel uGen38024.cde is fixed at pre-defined baud rate of 38400 and clock frequency of 9.83 MHz, so no customisation of the µKernel is allowed.

2. Hardware Requirements

A simple onboard programming circuitry consists of the following three blocks: Crystal oscillator block, Boot mode's setting block and Serial communication block.

2.1 Crystal Oscillator Block

The clock circuitry comprises of a 9.8304 MHz quartz crystal for the main clock and a 32.768 kHz quartz crystal for the sub clock. This 9.8304 MHz crystal on the H8/38024F target board allows FDT to download programming data at a baud rate of 38400 bps with bit error rate of 0%.

n = 0 for ϕ = 9.8304/2 (MHz)
= 4.9152 (MHz)

$$N = \frac{OSC \times 10^6}{64 \times B \times 2^{2n}} - 1 \quad \text{.....[1]}$$

Given OSC = 9.8304 (MHz), B = 38400 (bps) and n = 0,
Hence, N = 3

$$Error = [\frac{\phi \times 10^6}{(N+1) \times 64 \times B \times 2^{2n-1}} - 1] \times 100\% \text{ .....[2]}$$

Hence, Error = 0 %.

Therefore, a baud rate of 38400 bps is chosen for a main clock of 9.8034 MHz.

2.1.1 Conditions

Stable VCC with decoupling capacitor of 0.1µF to GND

2.2 Boot Mode's Setting Block

To enter into boot mode, it requires the conditions of TEST = 0, P95 = 0 and P34 = 1. After /RES_N ends, HD64F38024 micon will be set to boot mode. The Reset Timing diagram is as follows:

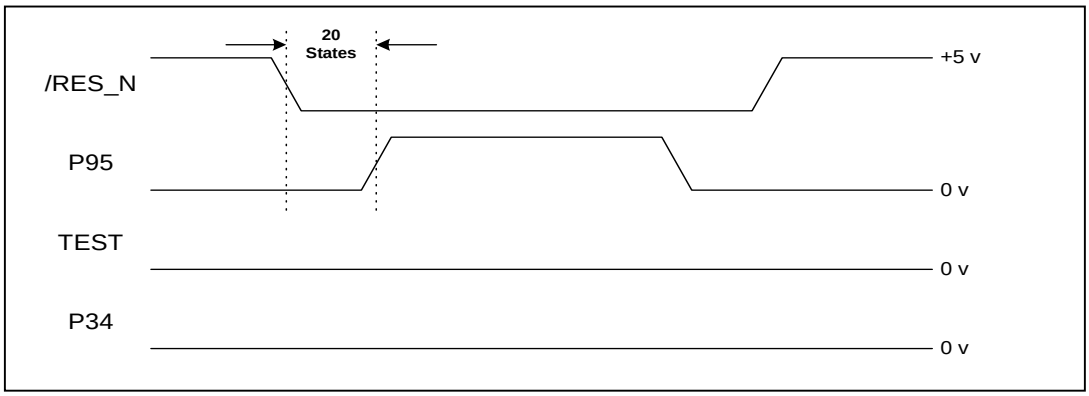


Figure 2.1 Reset Timing of Boot Mode

2.2.1 Conditions

P95 is set HIGH after /RES_N goes LOW for 20 states

2.3 Serial Communication Block

FDT links the Target board to the Host PC using the on-chip, three-wire serial communication channel [SCI3] on the H8/38024F micon. This requires a RS232 transceiver [eg. SP3232ECT] to translate the RS232 signals. The connection between the Target board and the Host PC is using serial cable with DB-9 connectors.

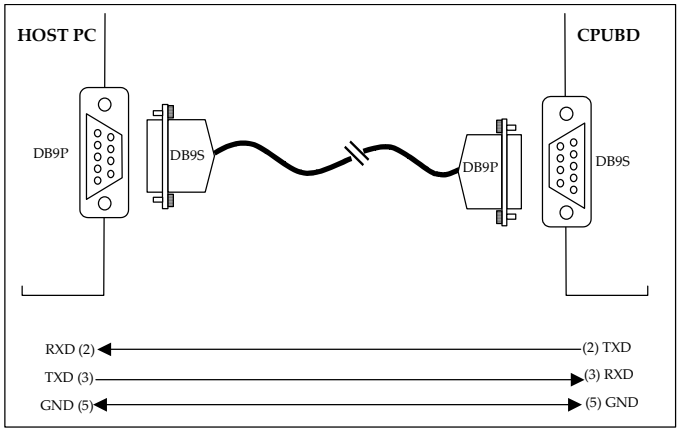


Figure 2.2 Serial Connection

3. Block Diagram of Onboard Flash Circuitry

The block diagram of an onboard flash circuitry for H8/38024F is shown in Fig 3.1. The detailed circuit diagram and BOM List can be found in Appendix A and Appendix B respectively.

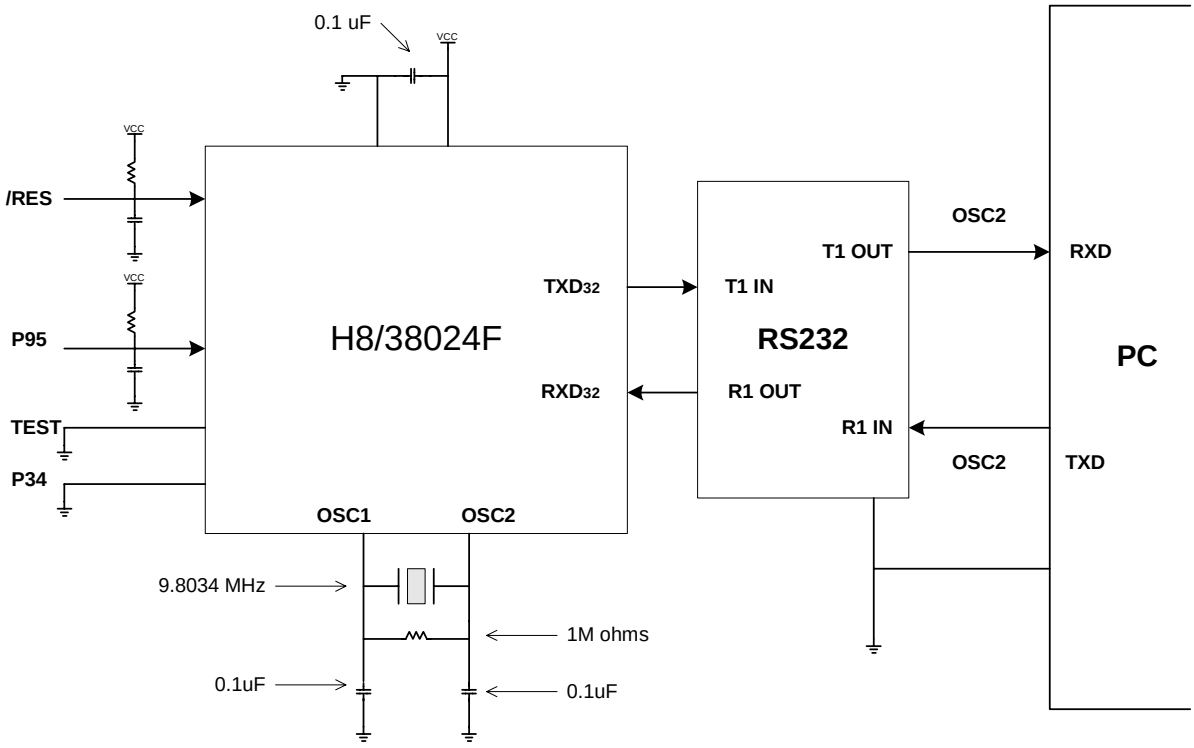


Figure 3.1 Block Diagram of Onboard Flash Circuitry

4. Basic Operation of FDT v2.2

4.1 Creating a New Workspace

Click on **Start** menu of Windows® and select **Program** -> **Renesas** -> **FLASH Development Toolkit 2.2** to open the Welcome to the FLASH Development Toolkit dialog box.

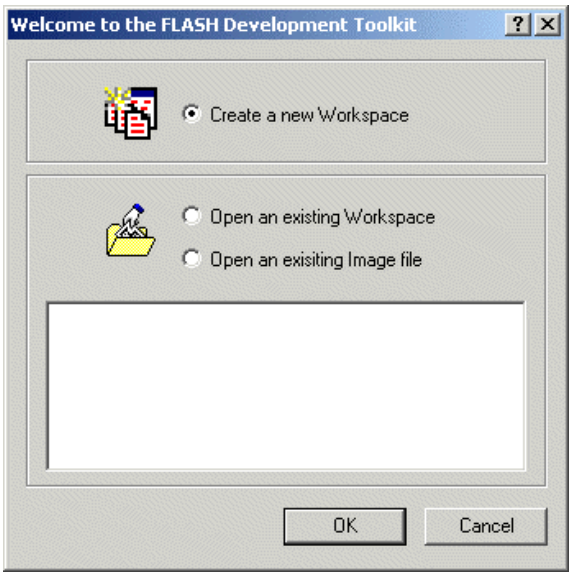


Fig 4.1 Welcome to FLASH Development Toolkit dialog box

- Enter the workspace name and click **OK** button.

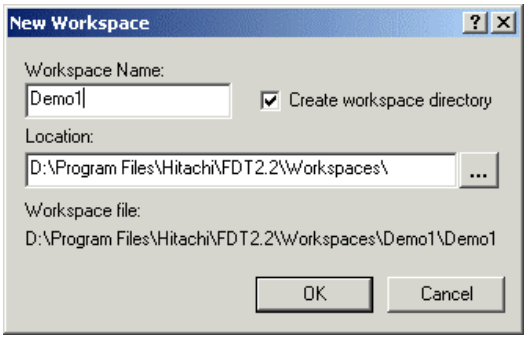


Fig 4.2 New Workspace dialog box

- Click **Yes** button to run Project Wizard

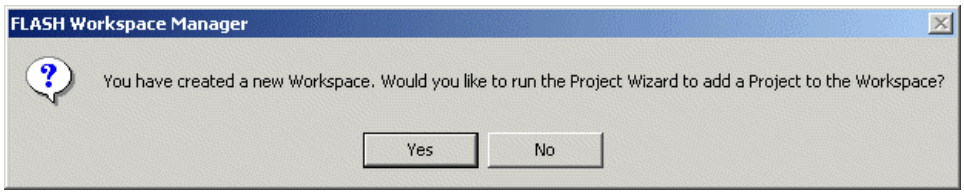


Fig 4.3 FLASH Workspace Manager dialog box

- Enter the project name, then click **Next** button

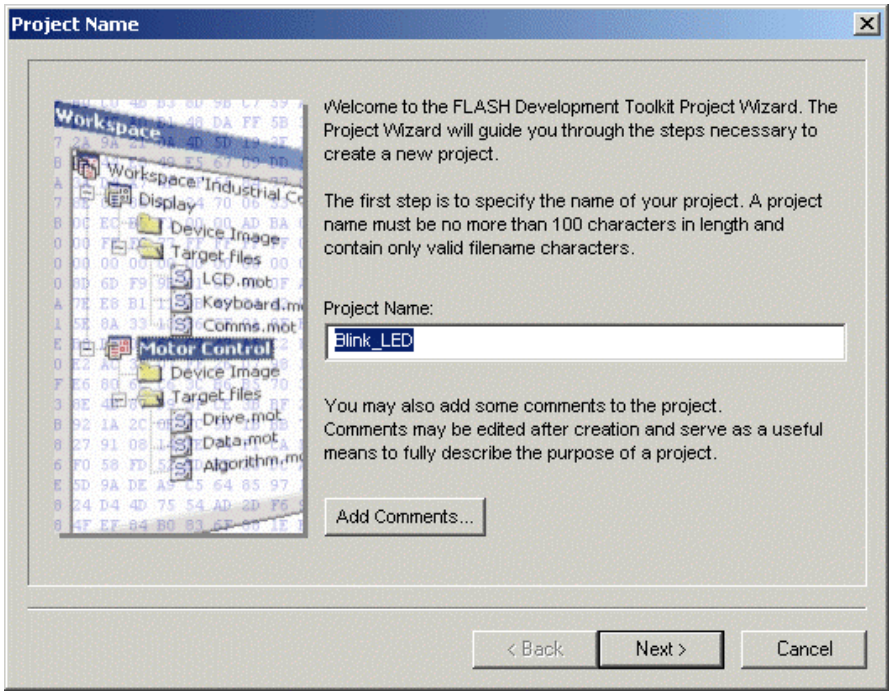


Fig 4.4 Project Name dialog box

- Select Device **H8/38024F** from the drop-down list, otherwise click **Other…** button to specify the kernel file (.fcf)

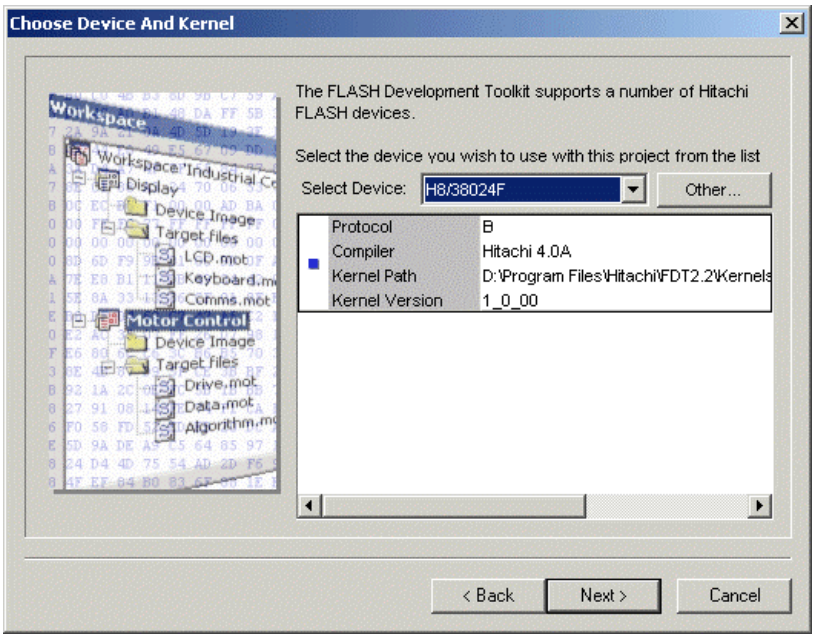


Fig 4.5 Choose Device And Kernel dialog box

- Select a port and use the default baud rate of 38400 bps, then click the **Next** button.

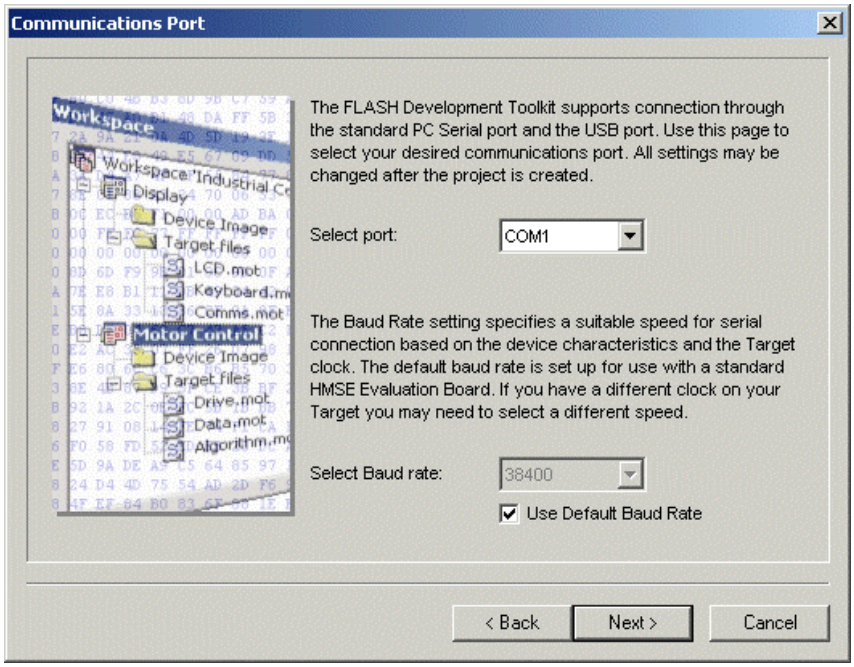


Fig 4.6 Communication dialog box

- Enter the numerical values for the input clock of **9.83** MHz

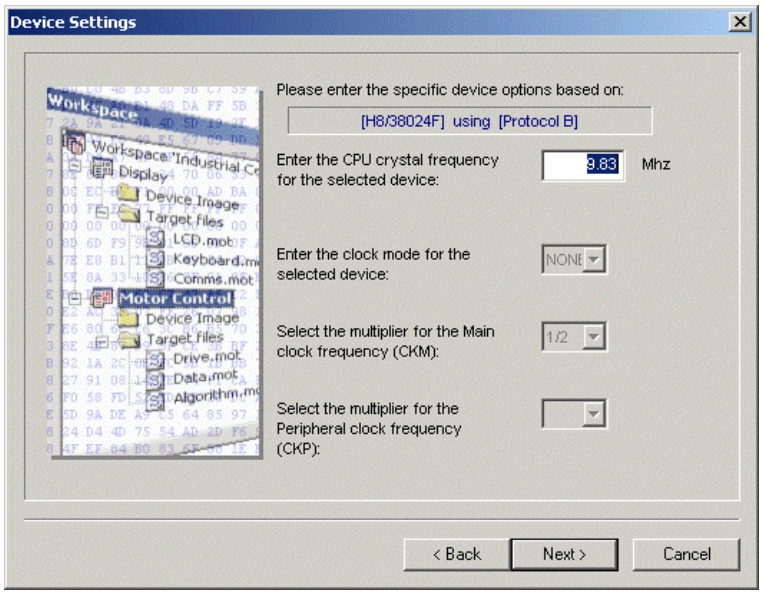


Fig 4.7 Device Setting dialog box

- Choose **BOOT Mode** as the operating mode, then click **Next**

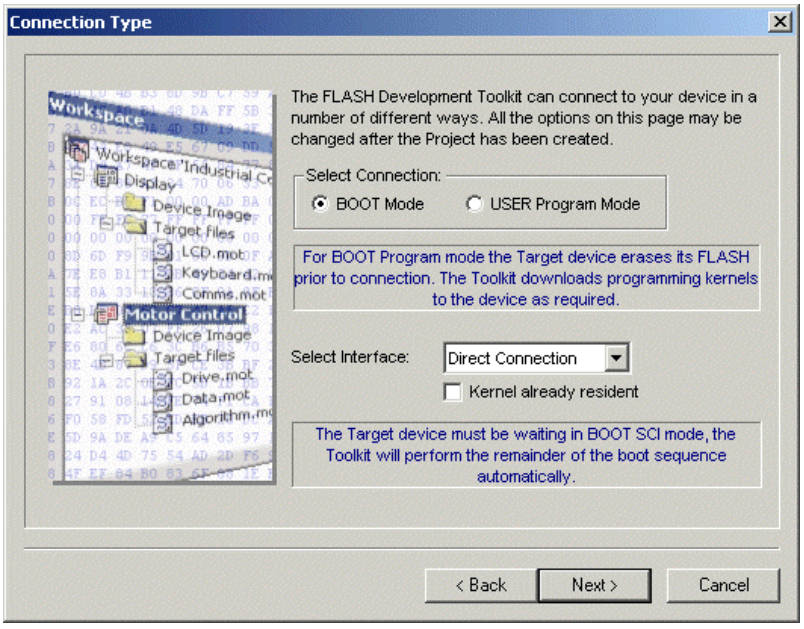


Fig 4.8 Communication dialog box

- Select the **Protection Level** and **Message Level** during programming, then click the **Finish** button

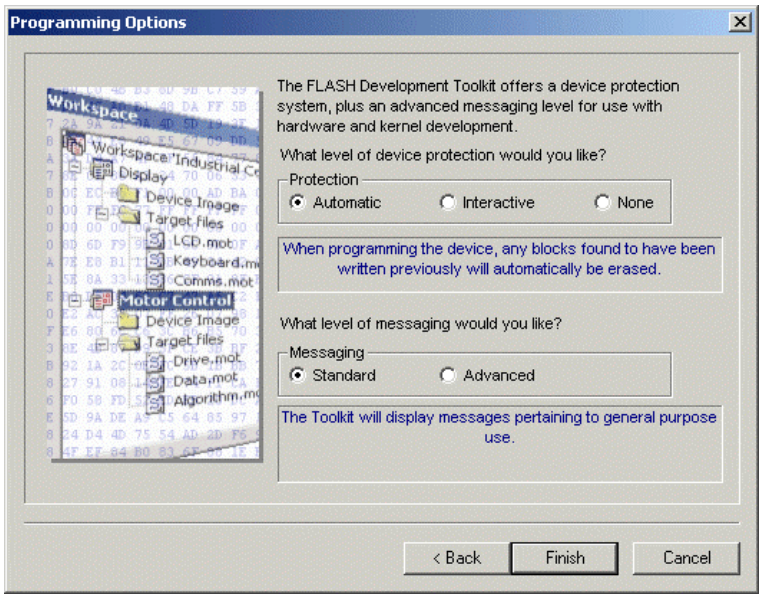


Fig 4.9 Programming Options dialog box

- An empty workspace will appear

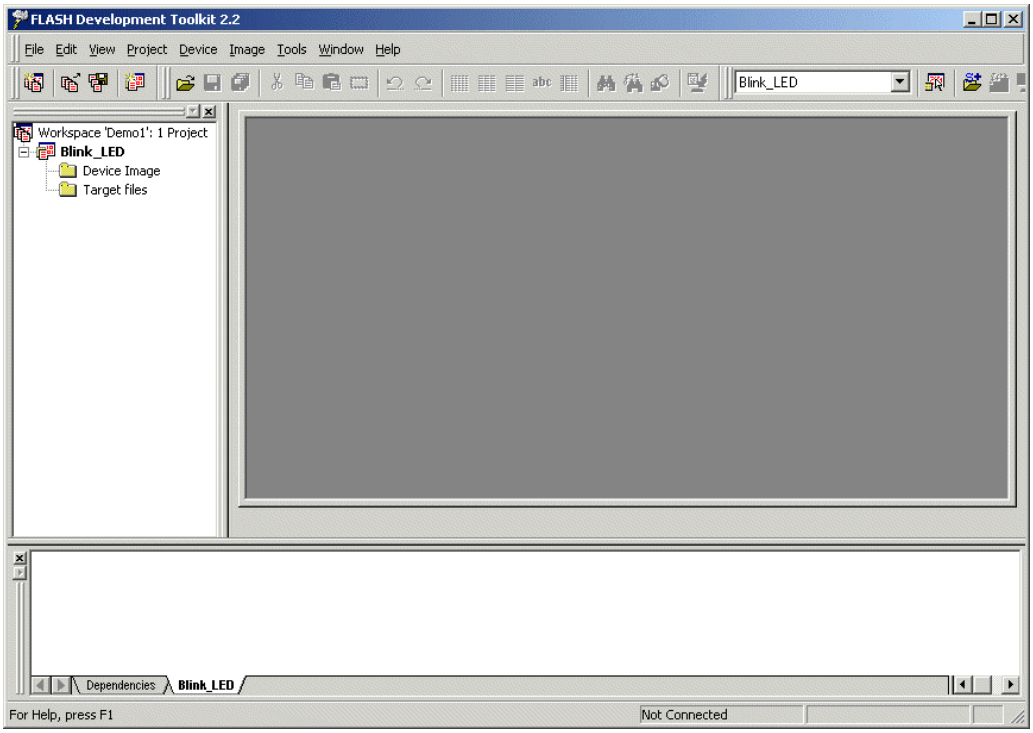


Fig 4.10 FLASH Development Toolkit V2.2 Window

4.2 Data Programming to the Flash Memory in Boot Mode

- Press **Reset Switch** (S1) once and select **[Device -> Connect to device]**

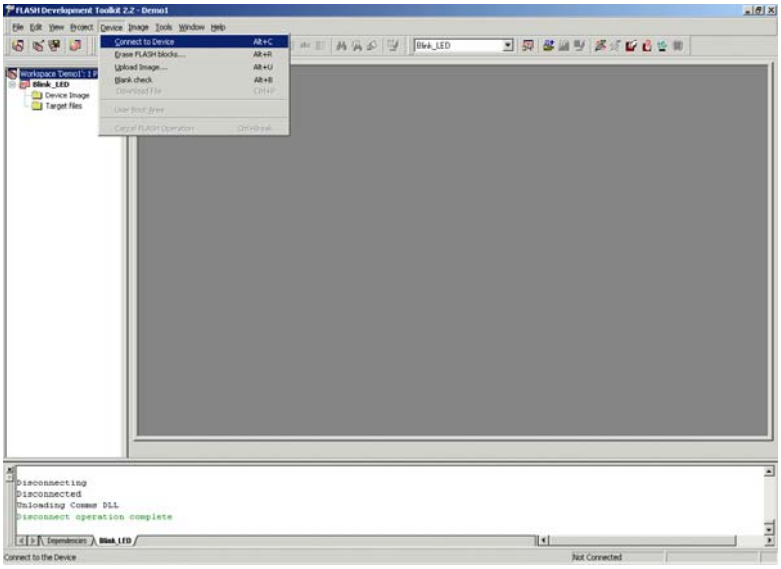


Fig 4.11 Connect to Device pop-up menu

- Select **Target Files** and right-click to **Add Files to Project …**

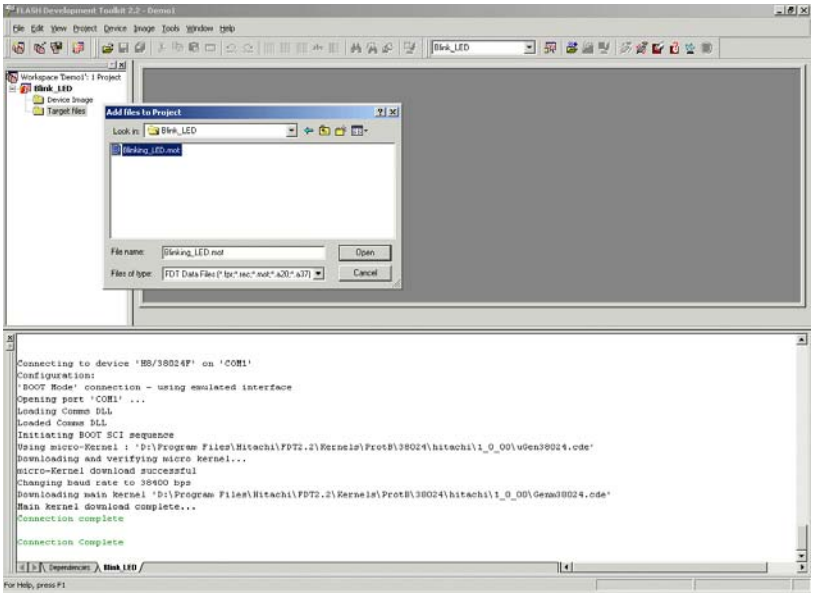


Fig 4.12 Add Target to Project dialog box

- Select the target module and right-click to **Download to Device**. This will program the flash device.

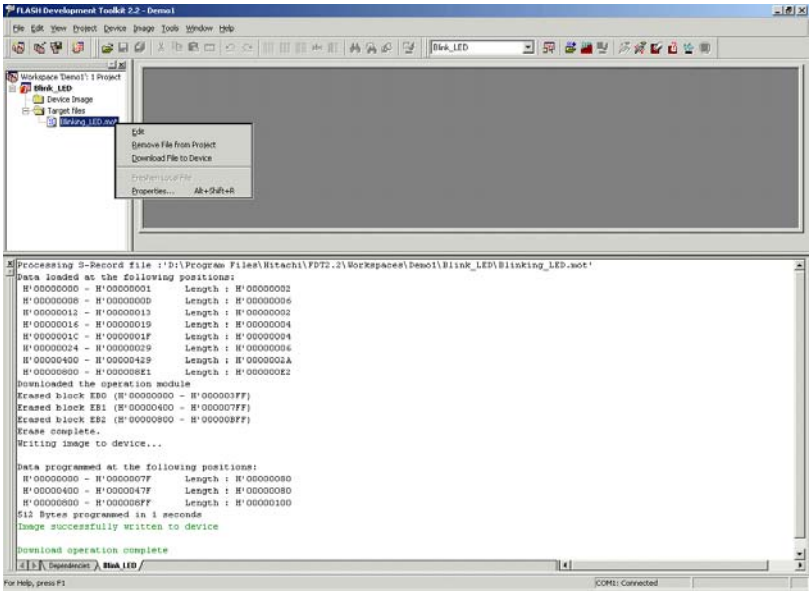


Fig 4.13 Download to Device pop-up menu

4.3 Viewing or Erasing The Device Data

- Select **[Device -> Upload image …]** to display Upload Image dialog box
- Enter the **Start** and **End addresses**
- Click **Upload** button to read the Flash Memory data

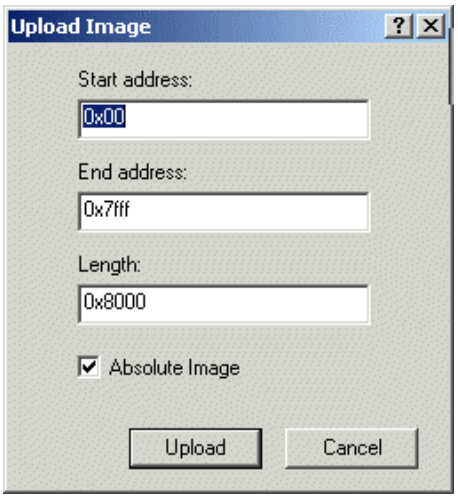
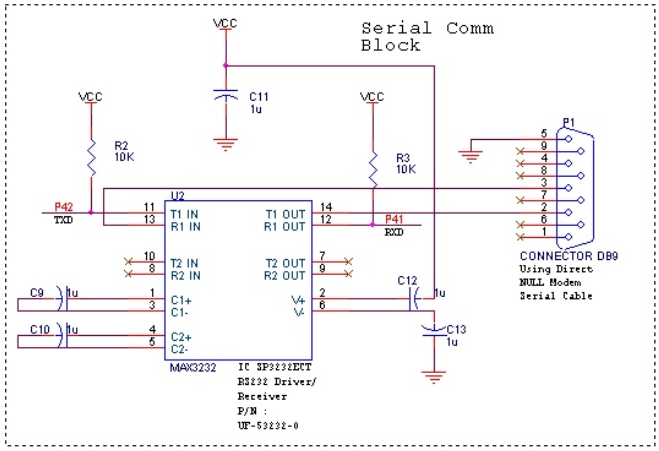
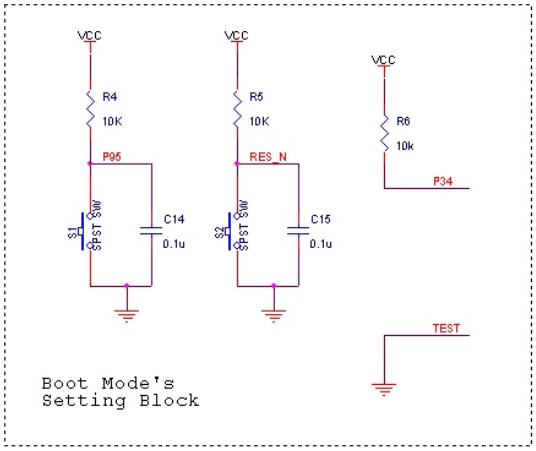
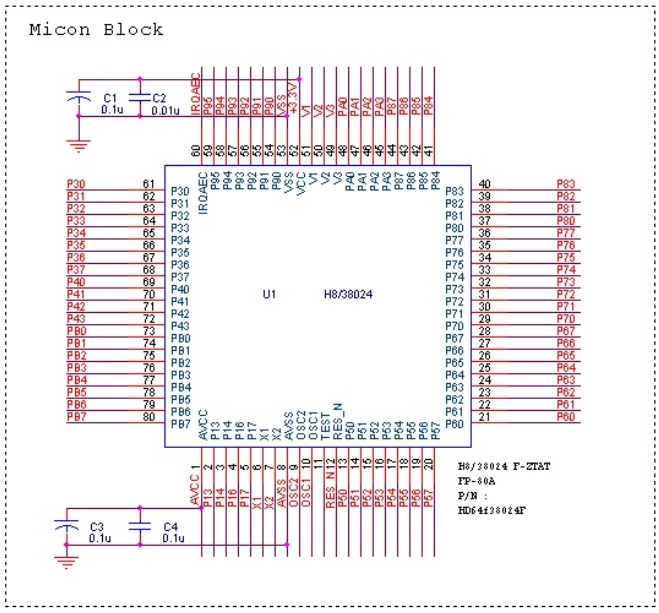


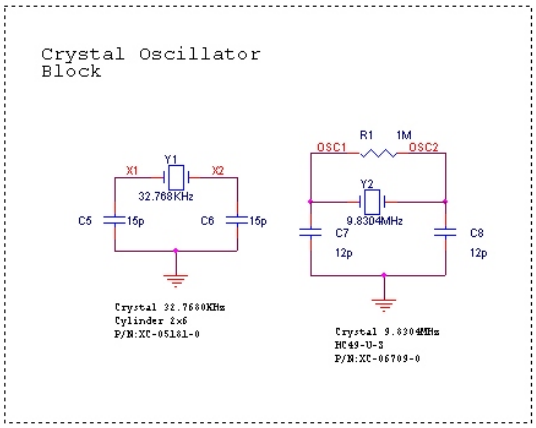
Fig 4.14 Upload Image dialog box

APPENDIX A: Circuit Diagram









Appendix B: BOM List

	Designators	Part Description	Qty	Remarks
1.	C1, C3	Cap Electrolytic 100nF/50V	2	
2.	C2	Cap Ceramic 10nF/50V 10%	1	
3.	C4, C14 – 15	Cap Ceramic 100nF/50V 10%	3	
4.	C5 – 6	Cap Ceramic 15pF/50V 5%	2	
5.	C7 – 8	Cap Ceramic 12pF/50V 5%	2	
6.	C9 – 13	Cap Electrolytic 1uF/50V	5	
7.	R1	Res 1/4w 1MΩ 2%	1	
8.	R2 – 6	Res 1/8w 10kΩ 5%	5	
9.	U1	H8/38024F, FP-80A	1	
10.	U2	IC SP3232ECT RS 232 Driver/Receiver	1	
11.	Y1	Crystal 32.768 kHz Cylinder 2x6	1	
12.	Y2	Crystal 9.8304 MHz HC49/U-S	1	
13.	P1	Connector D-Sub Female 9-way	1	
14.	S1 – 2	Switch Tactile Round	2	

Reference

1. Renesas FLASH Development Toolkit 2.2: User's Manual
2. H8/300L Super Low Power Series – Low-cost CPU Board CPUBD-38024F User' CPUBD-38024F User's Manual
3. H8/38024 Series, H8/38024F-ZTAT™ Hardware Manual
4. FLASH Development Toolkit Kernel Guide [for FDT v1.5]

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.03	-	First edition issued

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