ZBT SRAMS: SYSTEM DESIGN ISSUES AND BUS TIMING

Application Brief AN-203

by Pat Lasserre

Introduction

In order to increase system throughout, today's systems require a more efficient utilization of system buses. To support this need for higher system bandwidth IDT pioneered, and along with partners Micron and Motorola further developed a new SRAM architecture known as Zero Bus Turnaround (ZBT). This ZBT architecture allows the designer to utilize 100% of the data bus cycles without design restrictions. ZBT allows for either a write or a read to be initiated on every rising clock edge, which makes the device ideal for performance-driven networking applications that require frequent random reads and writes. The bus timing associated with ZBT SRAMs is shown in Figure 1.

Traditional pipelined SRAMs require two idle cycles when turning the bus around from a Write to a Read. This can result in as low as 50% bus utilization for applications requiring frequent back-to-back write and read operations. Figure 2 illustrates the bus timing associated with these pipelined SRAMs, which were originally designed for secondary cache applications.

By eliminating idle cycles, ZBT SRAMs utilize 100% of the bus cycles. The condition that arises from this 100% bus utilization is an increased potential for the devices on the bus to suffer from the condition of "bus contention". This document describes the concerns and affects associated with bus contention.

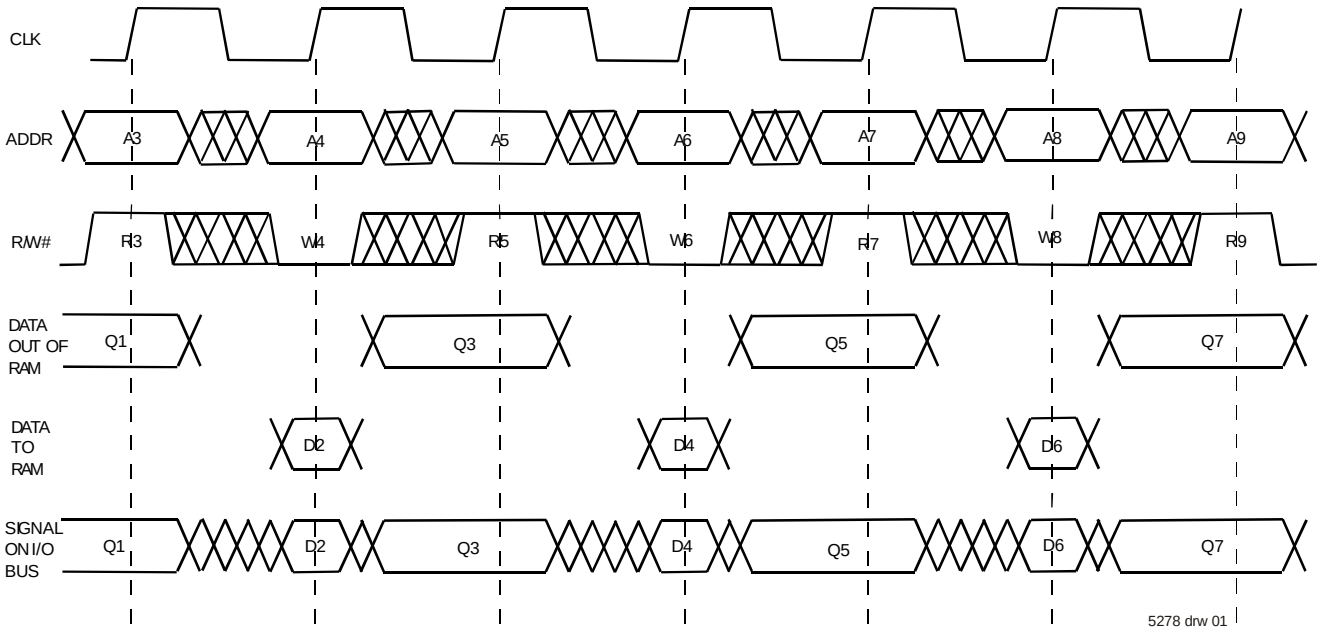
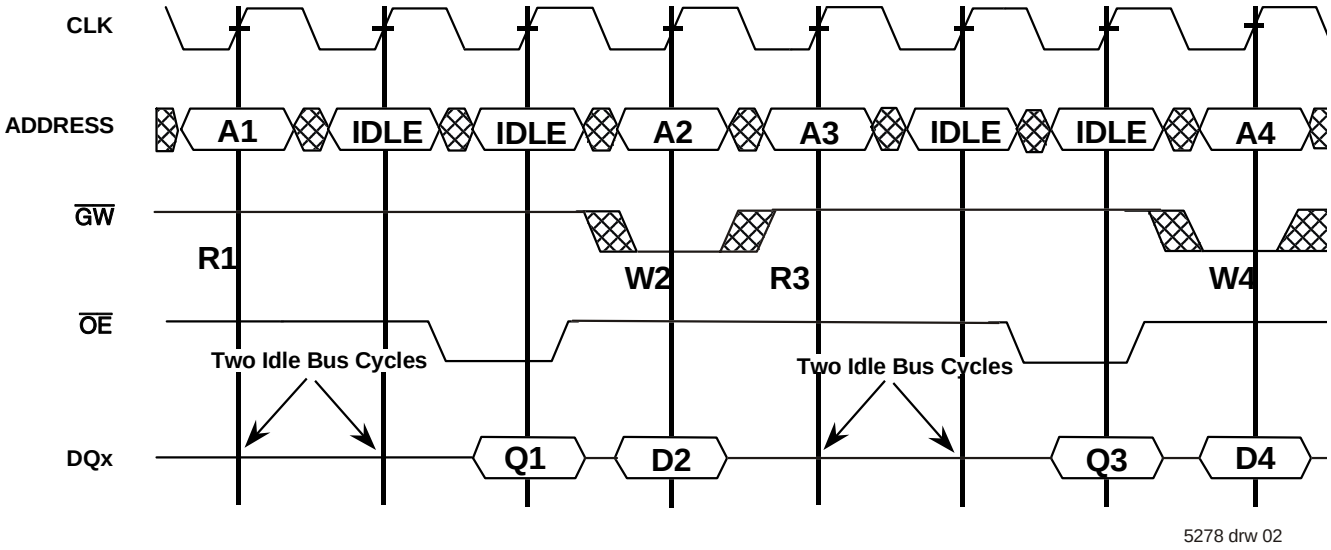


Figure 1
Bus Cycles: Pipelined ZBT, Alternating Reads and Writes



D = Data_in: Q = Data_out: R = Read: W = Write

Figure 2
Bus Cycles: Synchronous Pipelined, Alternating Reads and Write

What is Bus Contention?

Bus contention occurs when two or more devices are enabled on a bus at the same time and attempt to drive the bus to opposite logic values. For example, in Figure 3, Device A attempts to drive the bus to a logic 1 value while Device B attempts to drive the bus to a logic 0. This contention results in a current path between the contending devices. The current path is from Vcc through the "on" transistor of Device A to ground through the "on" transistor of Device B. This current path does not exist if the contending devices attempt to drive the bus to the same logic value.

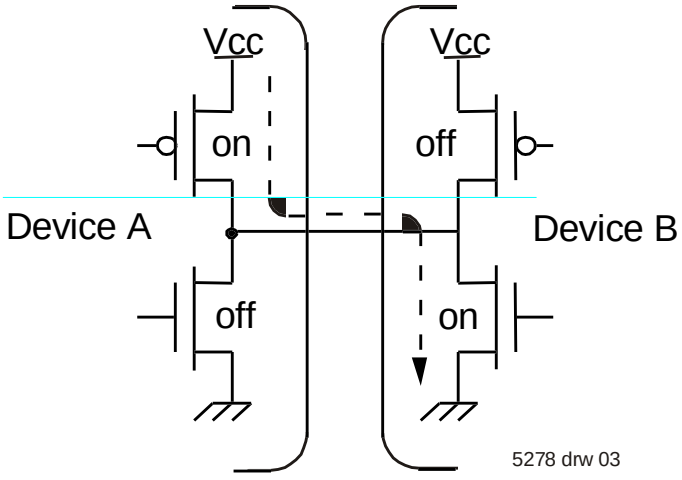


Figure 3

Definition of tCHZ and tCLZ

The two timing parameters, which define the potential for bus contention, are tCHZ (turn-off) and tCLZ (turn-on) of the two devices contending for the bus. Figure 4 shows tCHZ and tCLZ. The turn-on time (tCLZ) of a device is the time it takes for its outputs to become active, or go into a low impedance state (logic 1 of logic 0). The turn-off time (tCHZ) of a device is the time it takes for its outputs to go into a high impedance (High-Z) state. In the High-Z state the output structure of a device is off (i.e. both its pull-up and pull-down are off). Thus the output structure behaves as if it were not connected to the circuit and does not sink or source current. Also, in the High-Z state the output voltage follows whatever is driving the bus.

For the remainder of this discussion an SRAM to ASIC interface will be assumed. In order to avoid bus contention, the turn-off time (tCHZ) of a device must be less than the turn-on time (tCLZ) of the device to

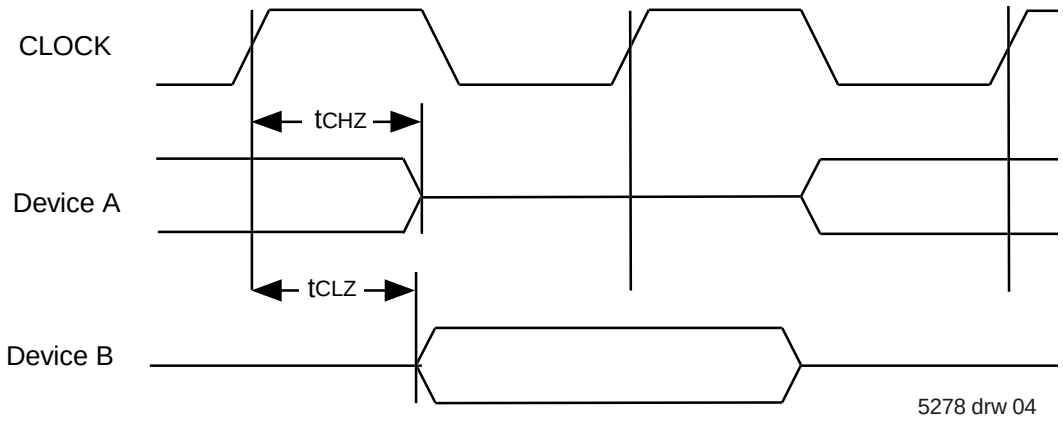


Figure 4
tCH and tCLZ

which it is interfacing. An example of this would be an read from an SRAM following a write to the SRAM. In order to avoid bus contention in this case, the ASIC, which is controlling the write, must turn off (tCHZ) and relinquish control of the bus prior to the SRAM output drivers turning on (tCLZ) to complete the read.

Data Sheet Specifications

In order to ensure quality, semiconductor manufacturers test at extremes. These “data sheet” extremes are at worst case device conditions and parameter process runs. Certain parameters may have worst case conditions at opposite extremes and therefore relating them based solely on data sheet parameters may be misleading.

If a system designer were to use the data sheet parameters for tCHZ and tCLZ then it would appear that the bus could not successfully be turned around without contention occurring. This is due to the fact that data sheets specify the worst case conditions for tCHZ and tCLZ. These worst case conditions are tCHZ (maximum) and tCLZ (minimum).

Fortunately, these two aforementioned conditions occur at opposite extremes of voltage and temperature. Maximum tCHZ occurs at high temperature and low Vcc whereas minimum tCLZ occurs at low temperature and high Vcc.

Since components, which interface with one another, operate at similar voltage and temperature, a more realistic approach to evaluating tCLZ and tCHZ would be to measure the two parameters at the same voltage and temperature. IDT’s ZBT RAMs are designed to ensure that under the same conditions of voltage and temperature that the turn-off time (tCHZ) of the RAMs are faster than their turn-on time (tCLZ) by approximately 1ns. Thus bus contention between ZBT RAMs interfacing with one another will not occur.

System Effects On Bus Contention

System effects such as clock skew, inductance and capacitance play important roles with regards to bus contention.

Clock skew represents the possible difference in time between the arrival of the clock at two different devices that are interfacing with one another. This is shown in Figure 5. Clock skew may move the turn-off time of one device closer (or past) the turn-on time of the device to which it is interfacing. This could increase the chances of bus contention. Thus, minimizing clock skew is an essential part of board-level design when using ZBT SRAMs.

Both the power supply inductance and lead inductance help minimize the effects of bus contention. Since an inductor resists instantaneous changes in current, the power supply inductance and lead inductance will reduce the effects of possible bus contention by delaying the onset of contention current.

Also helping to minimize the effects of bus contention is the capacitive loading on the outputs. This can be seen is Figure 6

In this case we will use the example of the output switching from a logic 1 to a logic 0 where the pull-up of Device B does not get off the bus before the pull-down of Device A turns on. For simplification the pull-up of Device A and the pull-down of Device B are not shown since they are not active in this example. As the pull-down of Device A attempts to bring the output to a logic 0, the capacitor (C) will initially resist this change and keep the output at a logic 1. This is due to the fact that the voltage across a capacitor can not change instantaneously. With the output at a logic 1, there will be no voltage across the pull-up of Device B and thus no current through the device. The only current will be through the pull-down of device A to discharge the capacitor. This current through Device A would flow regardless of whether or not bus contention was present. By initially preventing any current flow through Device B, the capacitor reduces the effects of bus contention.

The larger the capacitor is, the larger its RC time constant will be, and thus the larger its discharge time will be. A longer discharge time means the output will remain at higher values for an extended period of time. Higher values on the output means less voltage across Device B and therefore less current through the pull-up device. Thus a larger output capacitance results in less contention current. This is shown in Figure 7 Diagrams A through E. These diagrams measure the contention current through the contending Device B for different values of output capacitance and for varying degrees, or lengths of time, of bus contention. For example, diagram A is measured with an output load of 20pF and Diagram C is measured with a 50pF output load. Each diagram measures the contention current through Device B for varying amounts of contention in 0.5ns increments from 1ns to 2.5ns. The total charge (Q) accumulated due to this contention current is also shown in each figure. Using Diagram A as an example, 1ns of contention results in 19.6pC of accumulated charge, 1.5ns of contention produces 43.6pC of charge, and so forth. Using the equation for current (I= dq/dt) it can be seen that for 1ns of contention, the contention current for a 20pF load is 2.4 times that for a 50pF load (19.6pC/8.11pC). Thus the larger capacitor had the effect of limiting the amount of contention current. This can also be seen by looking at Diagrams A–E where it is evident that the current values decrease with increasing capacitance.

Effects of Bus Contention

In terms of power consumption, simulations reveal that a small amount of bus contention (< 1.5ns) is equivalent to the addition of capacitance to the system bus. Transient power is defined by the following equation: $P = CV^2F$ where C is the output capacitance, V is the logic swing on the output, and F is the switching frequency of the

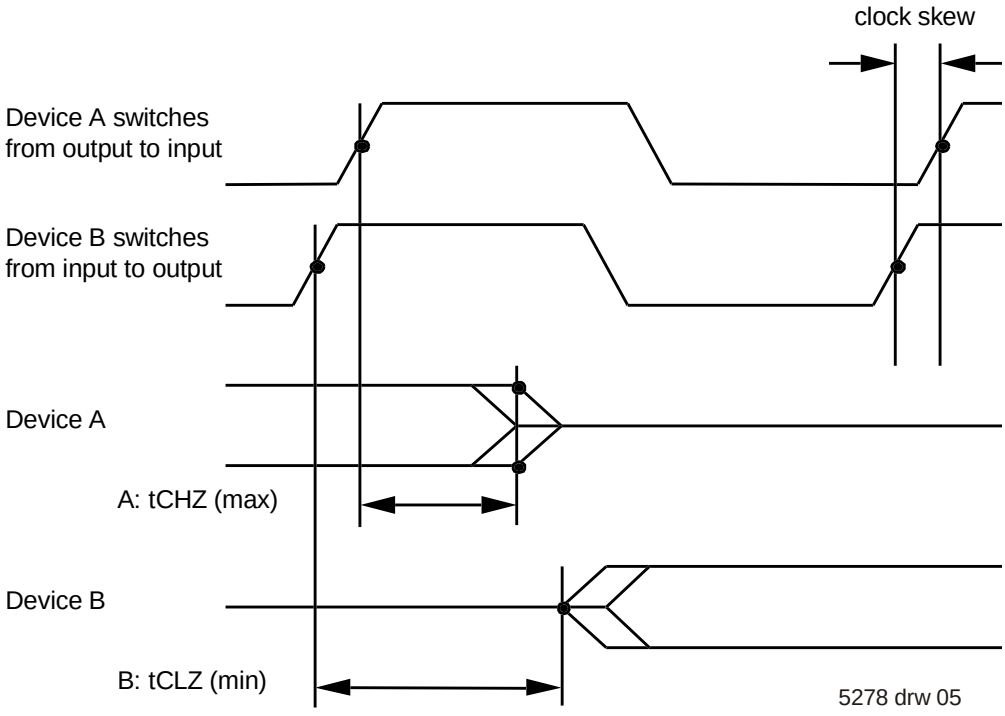


Figure 5
Clock Skew Reduces Timing Margins

system. This equation reveals that an increase in output capacitance results in increased power consumption. With respect to power consumption, small amounts of bus contention (< 1.5ns) can be equated to a slight increase in bus capacitance.

With regards to long term reliability, however, bus contention has much less of an impact on the system than does the addition of a true capacitance on the bus. As mentioned previously, output capacitance will delay the output from changing state. Referring once again to Figure 6, this delay will keep a high drain to source voltage (Vds) on Device A for an extended period of time. A high Vds can lead to high electric fields, which in turn causes hot electrons. Hot electrons are high-energy carriers from the channel of a device that can enter the oxide and become trapped. Once trapped in the oxide, these hot electrons alter the device's threshold voltage (Vt), negatively impacting the long-term reliability of the device.

In terms of short-term reliability, bus contentions has virtually no effect on the system. The diagrams in Figure 7 show the current through the contending pull up device for various amounts of contention (from 1ns to 2.5ns in .5ns increments). The important thing to note from these diagrams is for a given output load, the slopes of the lines

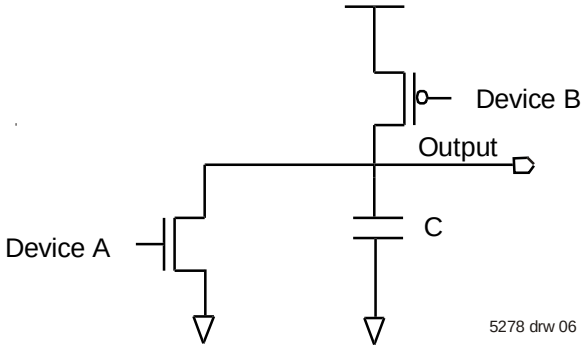


Figure 6

are the same regardless of the amount of contention. This is important because noise is generated by the **rate of change** in current (di/dt), not the total amount of current in a system. Noise in a system is seen as a voltage pulse generated by a current pulse and is described by the equation: V=Ldi/dt, where L is the lead inductance and di/dt is the rate of change of current across the inductor. Since the slopes of the current in Figure 7 are the same for varying amounts of contention this means there is no difference in the di/dt of a device with contention or without contention. Therefore, by referring back to the equation V=Ldi/dt, it can be seen that the contention current does not create any additional voltage noise pulse. Any noise in the system would be due to normal operating transitions of the data bus and therefore would be present regardless of the existence of bus contention.

The only real concern, with contention, in terms of reliability, would be the additional heat generated by the additional charge (Q). This can be quantified by using the amount of charge accumulated in a cycle due to contention current. Our simulations reveal that with a 30pF output load, 1.0ns of bus contention generates an additional 14.1pC of charge per output. Using a 36 output device this will result in a total charge of 14.1pC * 18 = 253.8pC (only 18 outputs are used since an output can be either a 1 or a 0 therefore the probability for contention between two devices is only 50%). At a frequency of 133MHz (7.5ns period) this results in a current of 33.8mA (I= dq/dt = 253.8pC/7.5ns). Using a thermal resistance of 40^0C/W this results in a temperature increase of (33.8mA)(3.3V)(40^0C/W) = 4.5^0C which is well within the range of system tolerance.

Conclusion

Zero Bus Turnaround™, or ZBT SRAM, is the new synchronous SRAM standard for high performance communications designs. By eliminating idle cycles when turning the bus around, ZBT maximizes bus bandwidth and data throughput.

With this high performance comes tight timing requirements and the possibility of bus contention. As outlined in this paper, capacitance and inductance in the system help reduce bus contention. Also, since data sheets specify t_{CHZ} and t_{CLZ} under opposite extremes, the possibility of bus contention is greatly overstated in a data sheet. With regards to power consumption, a small amount of bus contention can be viewed as a slight increase in system capacitance. Lastly, a small amount of bus contention (<1.5ns) has little impact on either the long-term or short-term reliability of the system. Thus, small amounts of bus contention (<1.5ns) can be present with little impact to the system.

Diagram A

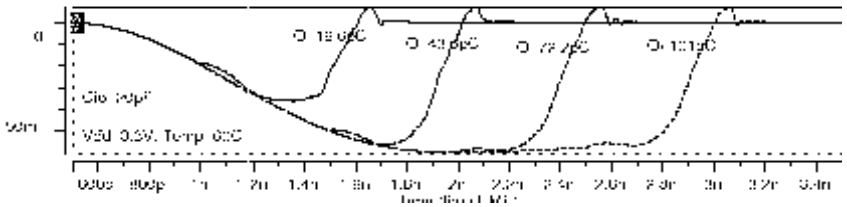


Diagram B

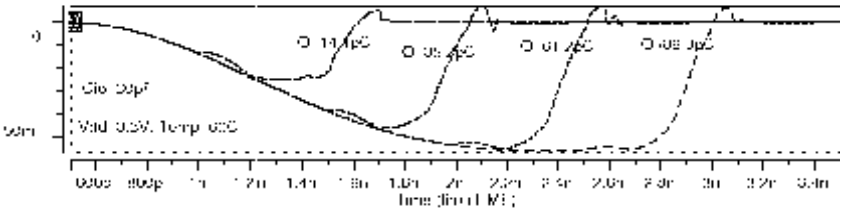


Diagram C

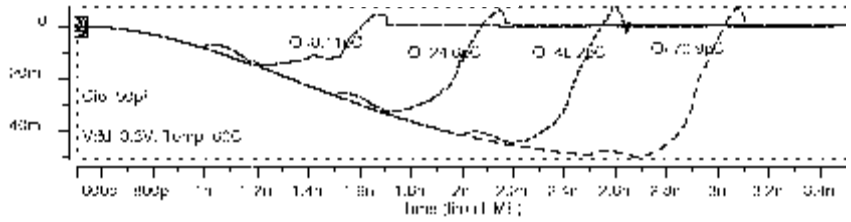


Diagram D

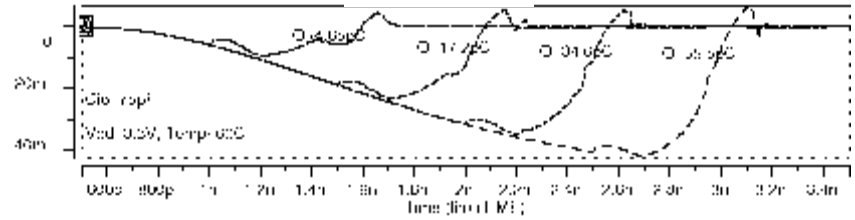


Diagram E

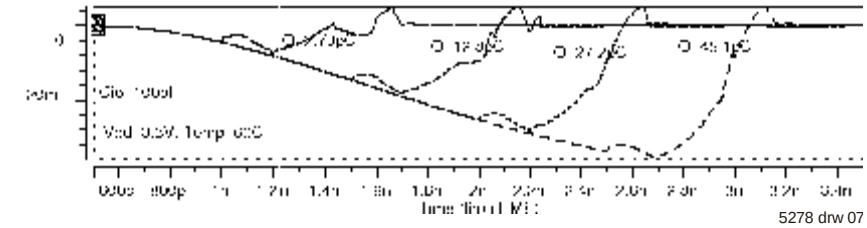


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Figure 7
Contention Current vs. Time

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