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Renesas Electronics Corporation

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R32C/100 Series

A/D Conversion in Repeat Mode

1. Abstract

In repeat mode, the A/D converter repeatedly performs A/D conversion on the input voltage of one pin from the following: AN_0 to AN_7, AN15_0 to AN15_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, or ANEX1.

2. Introduction

The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

This section describes how to perform A/D conversion on the input voltage of the AN_i pin (i = 0 to 7). The following conditions are necessary to perform conversion:

- Operation clock (φAD): fAD divided-by-2
- Resolution: 10-bit
- A/D conversion start condition: Software trigger
- Sample and hold function: Enabled
- DMAC operation mode: Disabled

3.1 Explanation

- (1) After setting the ADST bit in the AD0CON0 register to 1 (A/D conversion started), the A/D converter starts the conversion.
- (2) When conversion on the AN_i pin is complete, the value from the successive approximation register (conversion results) is transferred to the AD0i register (i = 0 to 7). Note that the IR bit in the AD0IC register does NOT become 1 (interrupt requested).
- (3) A/D conversion continues until the ADST bit is set to 0 (A/D conversion stopped). Each time conversion is completed, the conversion results are transferred to the AD0i register.

The diagram below shows operation timing.

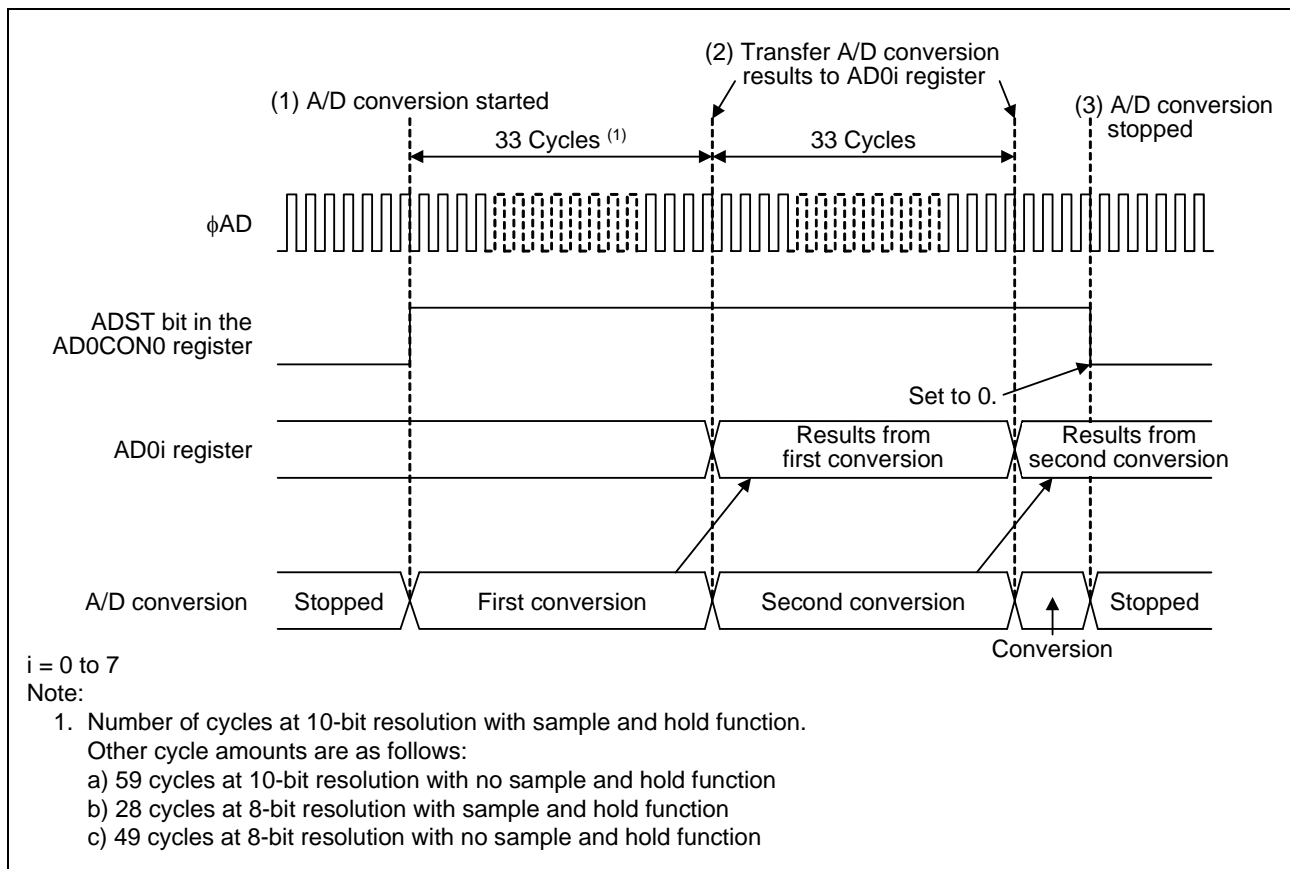
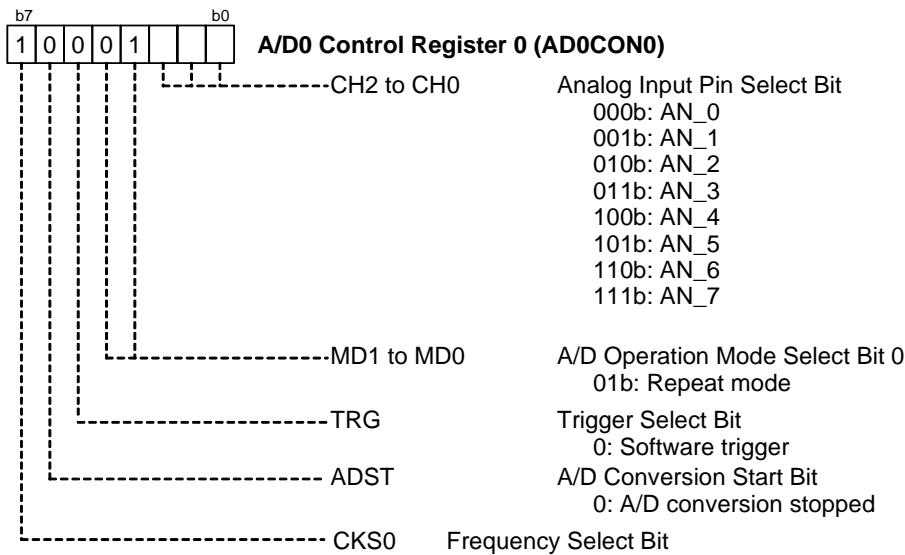


Figure 3.1 Operation in Repeat Mode

3.2 Setting

This section shows the procedures and values to set the example in section 3.1 “Explanation”. Refer to individual MCU hardware manuals for details on individual registers.

(1) Set the A/D0 control register 0.



Use the following bits to select the A/D converter operation clock (fAD):
 CKS0 bit in the AD0CON0 register
 CKS1 bit in the AD0CON1 register
 CKS2 bit in the AD0CON3 register

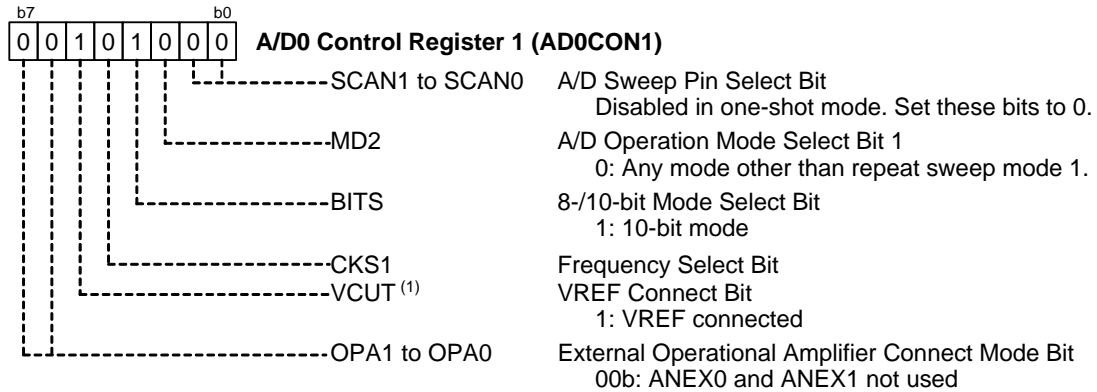
CKS2	CKS1	CKS0	Frequency
0	0	0	fAD divided-by-4
0	1	0	fAD divided-by-3
0	0	1	fAD divided-by-2
0	1	1	fAD
1	0	0	fAD divided-by-8
1	1	0	fAD divided-by-6

Only set the combinations listed above. When VCC is 5 V, set the ϕ_{AD} frequency to 16 MHz or less. When VCC is 3.3 V, set the ϕ_{AD} frequency to 10 MHz or less.

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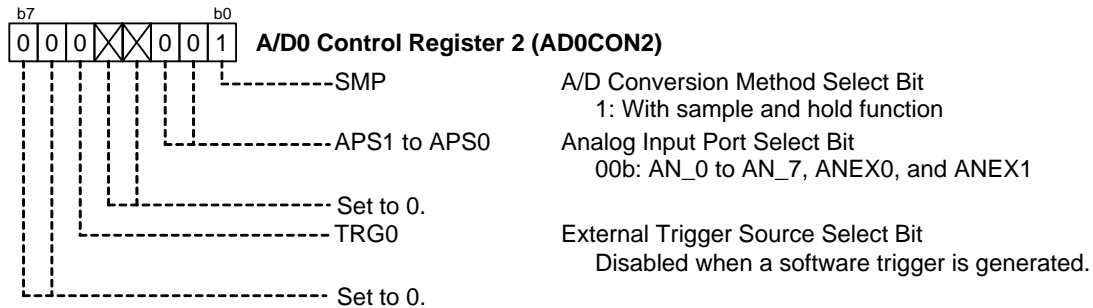
(2) Set the A/D0 control register 1.



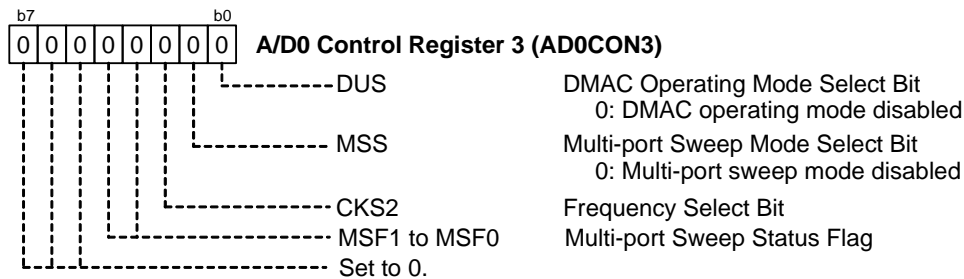
Note:

1. When rewriting this bit from 0 to 1, wait 1 μ s before starting A/D conversion.

(3) Set the A/D0 control register 2.



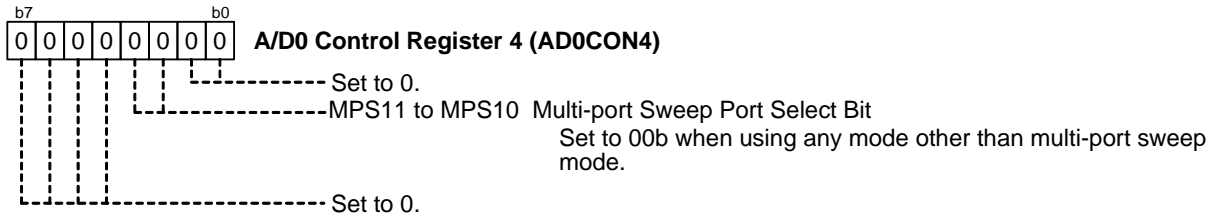
(4) Set the A/D0 control register 3.



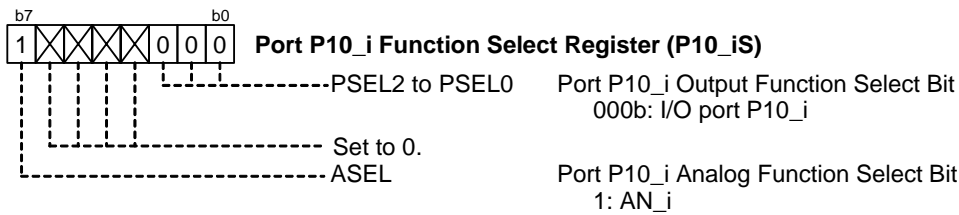
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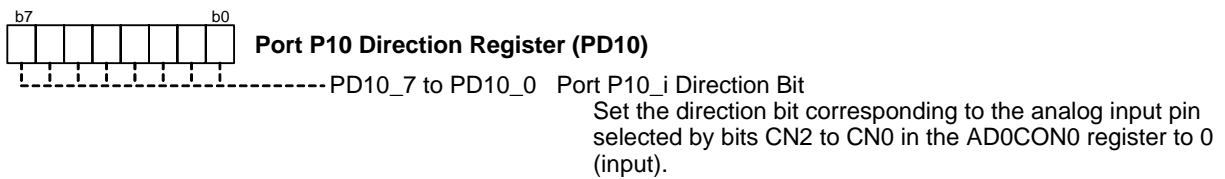
(5) Set A/D0 control register 4.



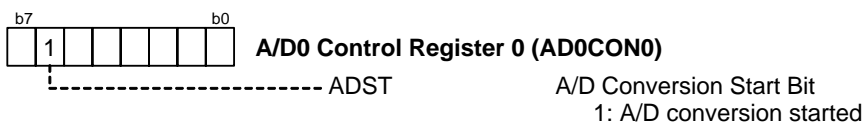
(6) Set the port P10_i function select register (i = 0 to 7).



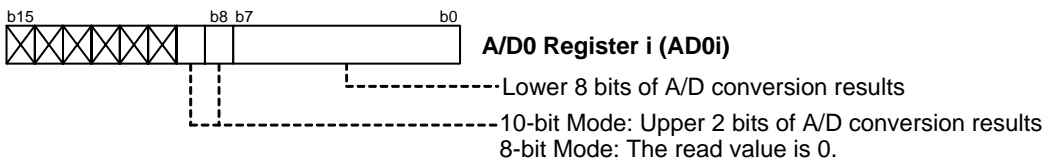
(7) Set the port P10 direction register.



(8) Start A/D conversion (set the A/D0 control register 0).



(9) Read the A/D conversion results (read the A/D0 register i).



4. Sample Program

A sample program can be downloaded from the Renesas Technology website.

5. Reference Documents

Hardware Manual

R32C/118 Group Hardware Manual Rev. 1.00

The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual

R32C/100 Series C Compiler Package Ver. 1.02 Compiler User's Manual Rev. 1.00

The latest version can be downloaded from the Renesas Technology website.

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REVISION HISTORY	A/D Conversion in Repeat Mode
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Rev.	Date	Description	
		Page	Summary
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