

To our customers,

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## H8/3664

### Access to the Serial EEPROM (I<sup>2</sup>C EEPROM) (H8/3664)

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#### Introduction

The H8/3664 group are single-chip microcomputers based on the high-speed H8/300H CPU, and integrate all the peripheral functions necessary for system configuration. The H8/300H CPU employs an instruction set which is compatible with the H8/300 CPU.

The H8/3664 group incorporates, as peripheral functions necessary for system configuration, four types of timers, I<sup>2</sup>C bus interface, serial communication interface, and 10-bit A/D converter. These devices can be utilized as embedded microcomputers in sophisticated control systems.

These H8/300 H Series -H8/3664- Application Notes consist of a "Basic Edition" which describes operation examples when using the on-chip peripheral functions of the H8/3664 group in isolation; they should prove useful for software and hardware design by the customer.

The operation of the programs and circuits described in these Application Notes has been verified, but in actual applications, the customer should always confirm correct operation prior to actual use.

#### Target Device

H8/3664

#### Contents

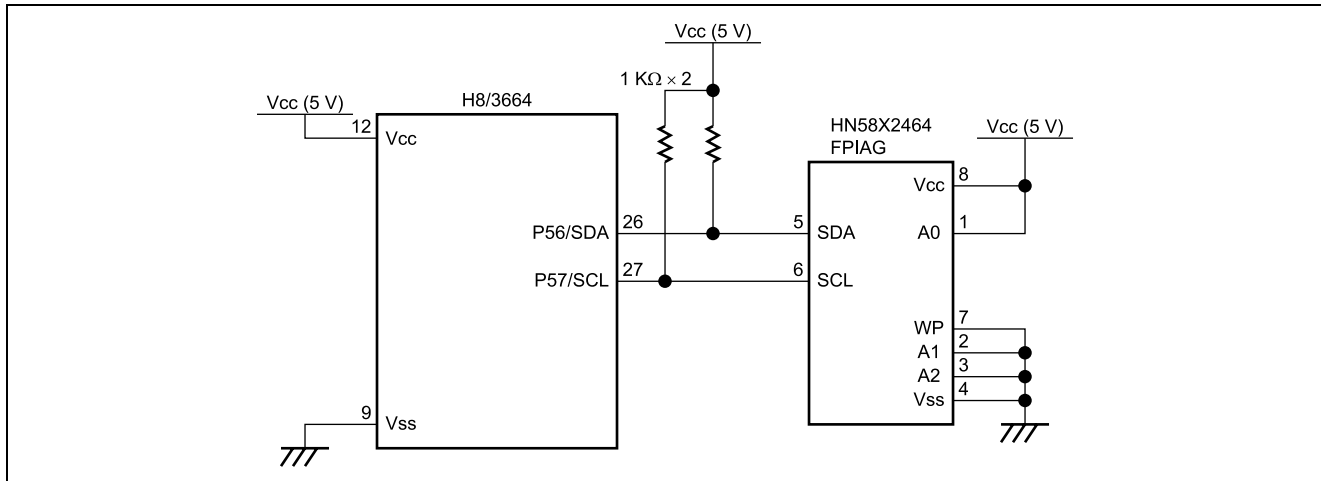
|                              |    |
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| 1. Overview .....            | 2  |
| 2. Configuration.....        | 2  |
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| 4. Reference Documents ..... | 42 |

### 1. Overview

The I<sup>2</sup>C EEPROM is read or written to via the H8/3664 I<sup>2</sup>C interface.

### 2. Configuration

Figure 2.1 shows a diagram of connections between the H8/3664 and I<sup>2</sup>C EEPROM.



**Figure 2.1 Connection to I<sup>2</sup>C EEPROM**

Specifications:

- H8/3664 operating frequency: 16 MHz
- Table 2.1 shows the I<sup>2</sup>C EEPROM (HN58X2464FPIAG) pin specifications
- I<sup>2</sup>C EEPROM specifications: 64 kbits (8192 x 8 bits)

**Table 2.1 I<sup>2</sup>C EEPROM Pin Specifications**

| Pin Name | Function  |
|----------|---|
| A0 to A2 | Device address (A0 is fixed to high, and A1 and A2 are fixed to low.) |
| SCL      | Serial clock input  |
| SDA      | Serial data input/output  |
| WP       | Write protect   |
| Vcc      | Power supply  |
| Vss      | Ground  |

### 3. Sample Programs

#### 3.1 Functions

1. One byte of data is written to the I<sup>2</sup>C EEPROM (Byte Write).
2. One byte of data is read from the I<sup>2</sup>C EEPROM (Random Read).
3. Data is written to the I<sup>2</sup>C EEPROM continuously (Page Write).
4. Data is read from the I<sup>2</sup>C EEPROM continuously (Sequential Read).

#### 3.2 Embedding the Sample Programs

1. Sample program 1-A  
Incorporate #define directives .
2. Sample program 1-B  
Incorporate prototype declarations.
3. Sample program 1-C  
Incorporate source program.

#### 3.3 Modifications to Sample Programs

Without modifications to the sample program, the system may not run. Modifications must be made according to the customer's program and system environment.

1. A file with definitions of IO register structures can be obtained free of charge from the following Renesas Technology web site: <http://www.renesas.com/eng/products/mpumcu/tool/crosstool/iodef/index.html>  
The sample program can be used without further changes. When creating definitions independently, the customer should modify the IO register structures used in the sample program as appropriate.
2. In the sample program, timer W is designed to start every 10 ms and timeout after 5 seconds, in order to monitor the state of the I<sup>2</sup>C interface. The timer processing can be modified according to the needs of the customer, and of course can be used without modification. When using the timer processing in the sample program without modification, the following changes should be made.
  - A. Sample program 1-E
    - The timer W reset vector should be added.
    - com\_timer should be added as a common variable.
    - The timer W initial setting processing should be added.
    - (The GRA setting should be changed according to the operating frequency of the microcomputer being used, so that the timer W interrupt occurs in 10 ms. For setting values, refer to the H8/3664 Hardware Manual; for the location of the setting to be changed, refer to the program notes in the sample program.)
    - The timer W interrupt processing should be added.
3. The I<sup>2</sup>C interface transfer rate ICMR (CKS2 to CKS0) and TSCR (IICX) should be set according to the target device specifications and the microcomputer operating frequency. Refer to the H8/3664 Hardware Manual for setting values, and to the program notes in the sample program for the location to be changed. In this sample program, the transfer rate is set to 200 kbps.

## 3.4 Method of Use

- One byte of data is written to the I<sup>2</sup>C EEPROM.

```
unsigned int com_i2c_eeprom_write
(unsigned char slave_addr, unsigned int rom_addr, unsigned char rom_data)
```

| Argument  | Description  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
|---|--|-------------------|---|-------------|----|----|---|--|--|-------------|--|--|--|-------------|--|--|--|---|---|---|---|----|----|----|---|
| slave_addr  | Specifies the I <sup>2</sup> C EEPROM slave address. The slave address is determined by the device code (fixed to 1010) and I <sup>2</sup> C EEPROM address pins (A2 to A0). In this sample program, A2 and A1 are low and A0 is high. |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="8">slave_addr format</th> </tr> <tr> <th colspan="4">Device code</th> <th colspan="3">Address pin</th> <th></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">A2</td> <td style="text-align: center;">A1</td> <td style="text-align: center;">A0</td> <td style="text-align: center;">0</td> </tr> </tbody> </table> |  | slave_addr format |   |             |    |    |   |  |  | Device code |  |  |  | Address pin |  |  |  | 1 | 0 | 1 | 0 | A2 | A1 | A0 | 0 |
| slave_addr format   |  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| Device code   |  |                   |   | Address pin |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| 1   | 0  | 1                 | 0 | A2          | A1 | A0 | 0 |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| Therefore, the setting value for slave_addr is 0xA2.  |  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| rom_addr  | Specifies the ROM address where data is written to.  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| rom_data  | Specifies 1-byte data to be written.   |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |

| Return value | Description   |
|--------------|---|
| 0            | Normal termination  |
| 1            | Abnormal termination (bus busy timeout)                             |
| 2            | Abnormal termination (transfer-preparation completion wait timeout) |
| 3            | Abnormal termination (acknowledge timeout)                          |
| 4            | Abnormal termination (transfer-completion wait timeout)             |
| 5            | Abnormal termination (reception-completion wait timeout)            |
| 6            | Abnormal termination (stop-condition detection timeout)             |

Example of use:

```
int ret;
unsigned char slave_addr, rom_data;
unsigned int rom_addr;

ret = com_i2c_eeprom_write (slave_addr, rom_addr, rom_data)
```

2. One byte of data is read from the I<sup>2</sup>C EEPROM.

```
unsigned int com_i2c_eeprom_read
(unsigned char slave_addr, unsigned int rom_addr, unsigned char *rom_data)
```

| Argument   | Description  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
|--|--|-------------------|---|-------------|----|----|---|--|--|-------------|--|--|--|-------------|--|--|--|---|---|---|---|----|----|----|---|
| slave_addr   | Specifies the I <sup>2</sup> C EEPROM slave address. The slave address is determined by the device code (fixed to 1010) and I <sup>2</sup> C EEPROM address pins (A2 to A0). In this sample program, A2 and A1 are low and A0 is high. |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| <table border="1" style="margin: auto;"> <thead> <tr> <th colspan="8">slave_addr format</th> </tr> <tr> <th colspan="4">Device code</th> <th colspan="3">Address pin</th> <th></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">A2</td> <td style="text-align: center;">A1</td> <td style="text-align: center;">A0</td> <td style="text-align: center;">0</td> </tr> </tbody> </table> |  | slave_addr format |   |             |    |    |   |  |  | Device code |  |  |  | Address pin |  |  |  | 1 | 0 | 1 | 0 | A2 | A1 | A0 | 0 |
| slave_addr format  |  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| Device code  |  |                   |   | Address pin |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| 1  | 0  | 1                 | 0 | A2          | A1 | A0 | 0 |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
|  | Therefore, the setting value for slave_addr is 0xA2.   |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| rom_addr   | Specifies the ROM address where data is read from.   |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| *rom_data  | Specifies the address where read data is stored.   |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |

| Return value | Description   |
|--------------|---|
| 0            | Normal termination  |
| 1            | Abnormal termination (bus busy timeout)                             |
| 2            | Abnormal termination (transfer-preparation completion wait timeout) |
| 3            | Abnormal termination (acknowledge timeout)                          |
| 4            | Abnormal termination (transfer-completion wait timeout)             |
| 5            | Abnormal termination (reception-completion wait timeout)            |
| 6            | Abnormal termination (stop-condition detection timeout)             |

Example of use:

```
int ret;
unsigned char slave_addr, *rom_data;
unsigned int rom_addr;

ret = com_i2c_eeprom_read (slave_addr, rom_addr, *rom_data)
```

3. Data is continuously written to the I<sup>2</sup>C EEPROM.

```
unsigned int com_i2c_eeprom_page_write
(unsigned char slave_addr, unsigned int rom_addr, unsigned int rom_length, unsigned
char *rom_data)
```

| Argument   | Description  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
|--|--|-------------------|---|-------------|----|----|---|--|--|-------------|--|--|--|-------------|--|--|--|---|---|---|---|----|----|----|---|
| slave_addr   | Specifies the I <sup>2</sup> C EEPROM slave address. The slave address is determined by the device code (fixed to 1010) and I <sup>2</sup> C EEPROM address pins (A2 to A0). In this sample program, A2 and A1 are low and A0 is high. |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
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| slave_addr format  |  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| Device code  |  |                   |   | Address pin |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| 1  | 0  | 1                 | 0 | A2          | A1 | A0 | 0 |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| Therefore, the setting value for slave_addr is 0xA2.   |  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| rom_addr   | Specifies the start address of the ROM area where data is written to.  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| rom_length   | Specifies the number of bytes to be written. On this device, up to 32 bytes of data can be written.  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| *rom_data  | Specifies the start address of the area where write data is stored.  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |

| Return value | Description   |
|--------------|---|
| 0            | Normal termination  |
| 1            | Abnormal termination (bus busy timeout)                             |
| 2            | Abnormal termination (transfer-preparation completion wait timeout) |
| 3            | Abnormal termination (acknowledge timeout)                          |
| 4            | Abnormal termination (transfer-completion wait timeout)             |
| 5            | Abnormal termination (reception-completion wait timeout)            |
| 6            | Abnormal termination (stop-condition detection timeout)             |

Example of use:

```
int ret;
unsigned char slave_addr, *rom_data;
unsigned int rom_length, rom_addr;

ret = com_i2c_eeprom_page_write (slave_addr, rom_addr, rom_length, *rom_data)
```



4. Data is continuously read from the I<sup>2</sup>C EEPROM.

```
unsigned int com_i2c_eeprom_page_read
(unsigned char slave_addr, unsigned int rom_addr,
unsigned int rom_length, unsigned char *rom_data)
```

| Argument   | Description  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
|--|--|-------------------|---|-------------|----|----|---|--|--|-------------|--|--|--|-------------|--|--|--|---|---|---|---|----|----|----|---|
| slave_addr   | Specifies the I <sup>2</sup> C EEPROM slave address. The slave address is determined by the device code (fixed to 1010) and I <sup>2</sup> C EEPROM address pins (A2 to A0). In this sample program, A2 and A1 are low and A0 is high. |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| <table border="1" style="margin: auto;"> <thead> <tr> <th colspan="8">slave_addr format</th> </tr> <tr> <th colspan="4">Device code</th> <th colspan="3">Address pin</th> <th></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">A2</td> <td style="text-align: center;">A1</td> <td style="text-align: center;">A0</td> <td style="text-align: center;">0</td> </tr> </tbody> </table> |  | slave_addr format |   |             |    |    |   |  |  | Device code |  |  |  | Address pin |  |  |  | 1 | 0 | 1 | 0 | A2 | A1 | A0 | 0 |
| slave_addr format  |  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| Device code  |  |                   |   | Address pin |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| 1  | 0  | 1                 | 0 | A2          | A1 | A0 | 0 |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
|  | Therefore, the setting value for slave_addr is 0xA2.   |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| rom_addr   | Specifies the ROM address where data is read from.   |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| rom_length   | Specifies the number of bytes to be read.  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |
| *rom_data  | Specifies the address to store read data.  |                   |   |             |    |    |   |  |  |             |  |  |  |             |  |  |  |   |   |   |   |    |    |    |   |

| Return value | Description   |
|--------------|---|
| 0            | Normal termination  |
| 1            | Abnormal termination (bus busy timeout)                             |
| 2            | Abnormal termination (transfer-preparation completion wait timeout) |
| 3            | Abnormal termination (acknowledge timeout)                          |
| 4            | Abnormal termination (transfer-completion wait timeout)             |
| 5            | Abnormal termination (reception-completion wait timeout)            |
| 6            | Abnormal termination (stop-condition detection timeout)             |

Example of use:

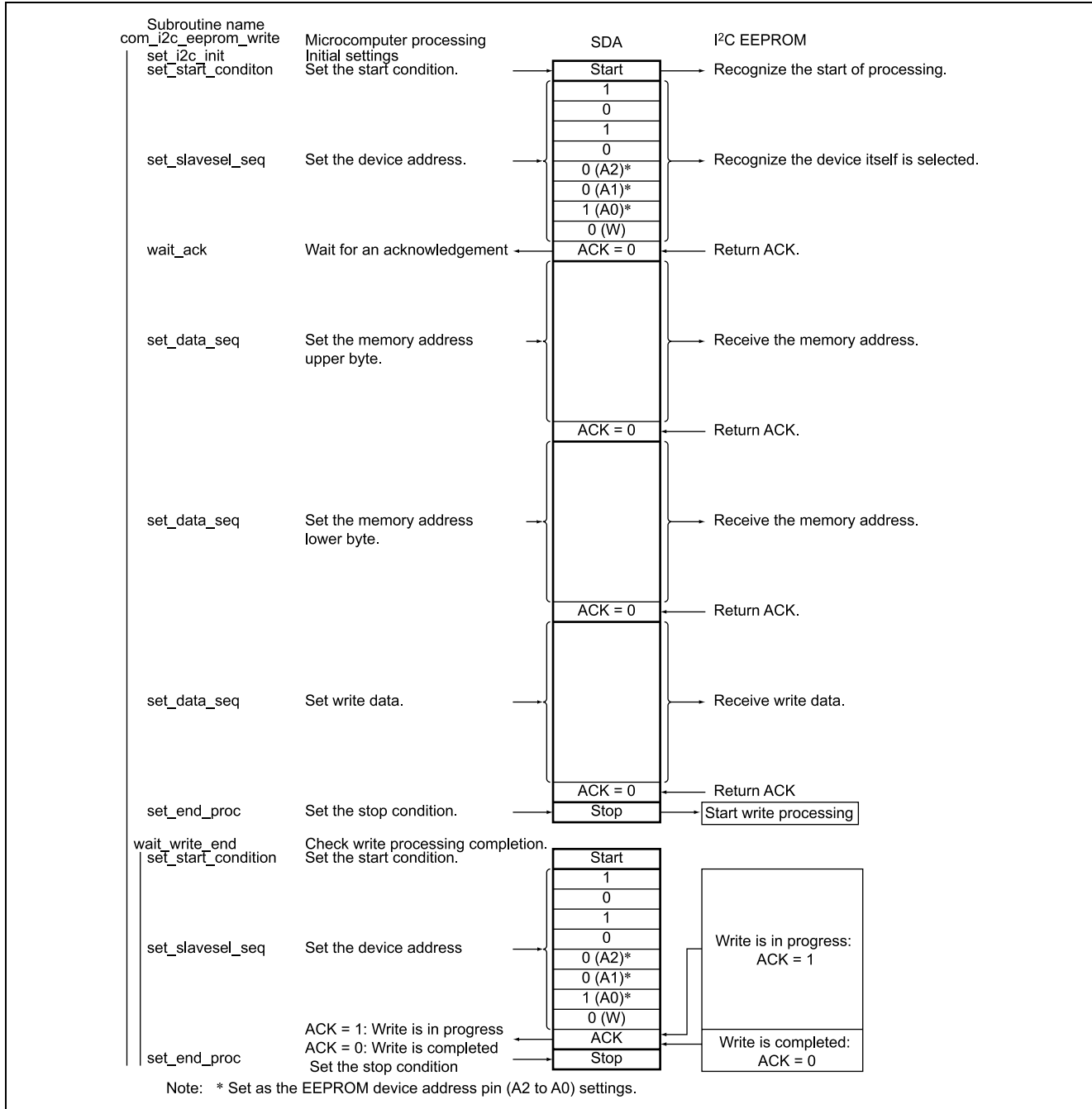
```
int ret ;
unsigned char slave_addr, *rom_data;
unsigned int rom_length, rom_addr;

ret = com_i2c_eeprom_page_read (slave_addr, rom_addr, rom_length, *rom_data)
```

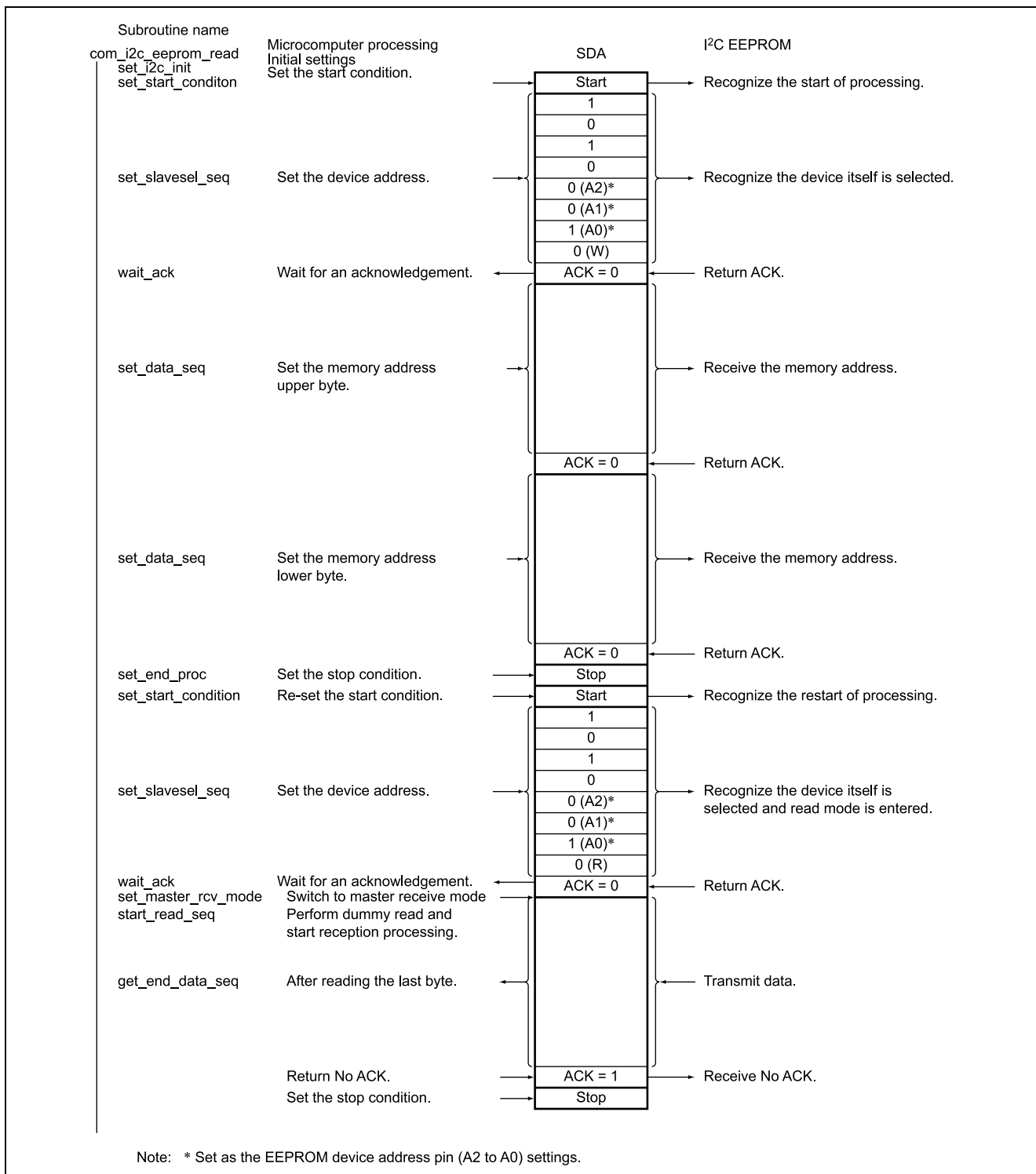
### 3.5 Explanation of Operation

The following figure explains the operation of the H8 microcomputer and the EEPROM with respect to the SDA data flow.

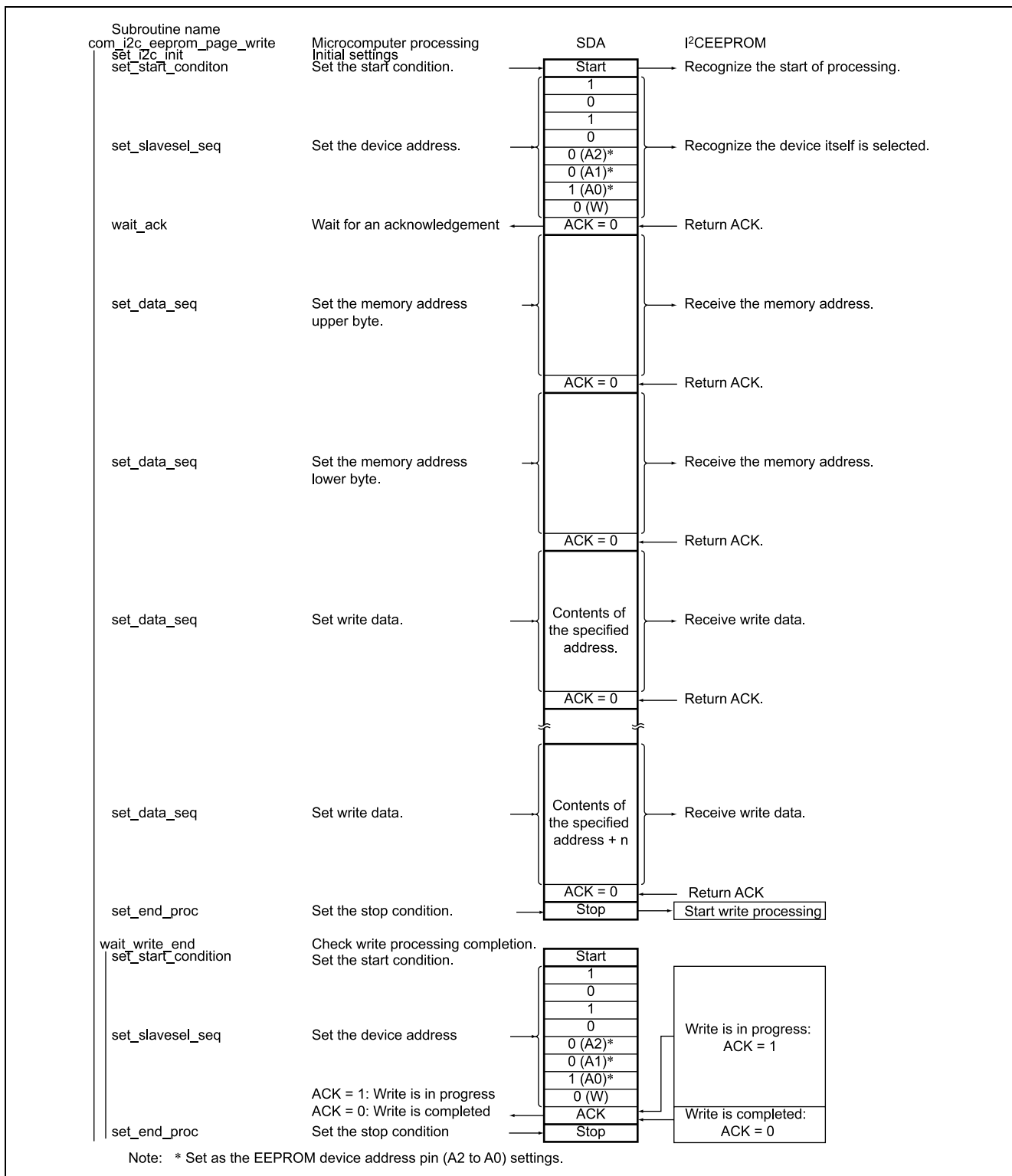
1. One byte of data is written to the I<sup>2</sup>C EEPROM.



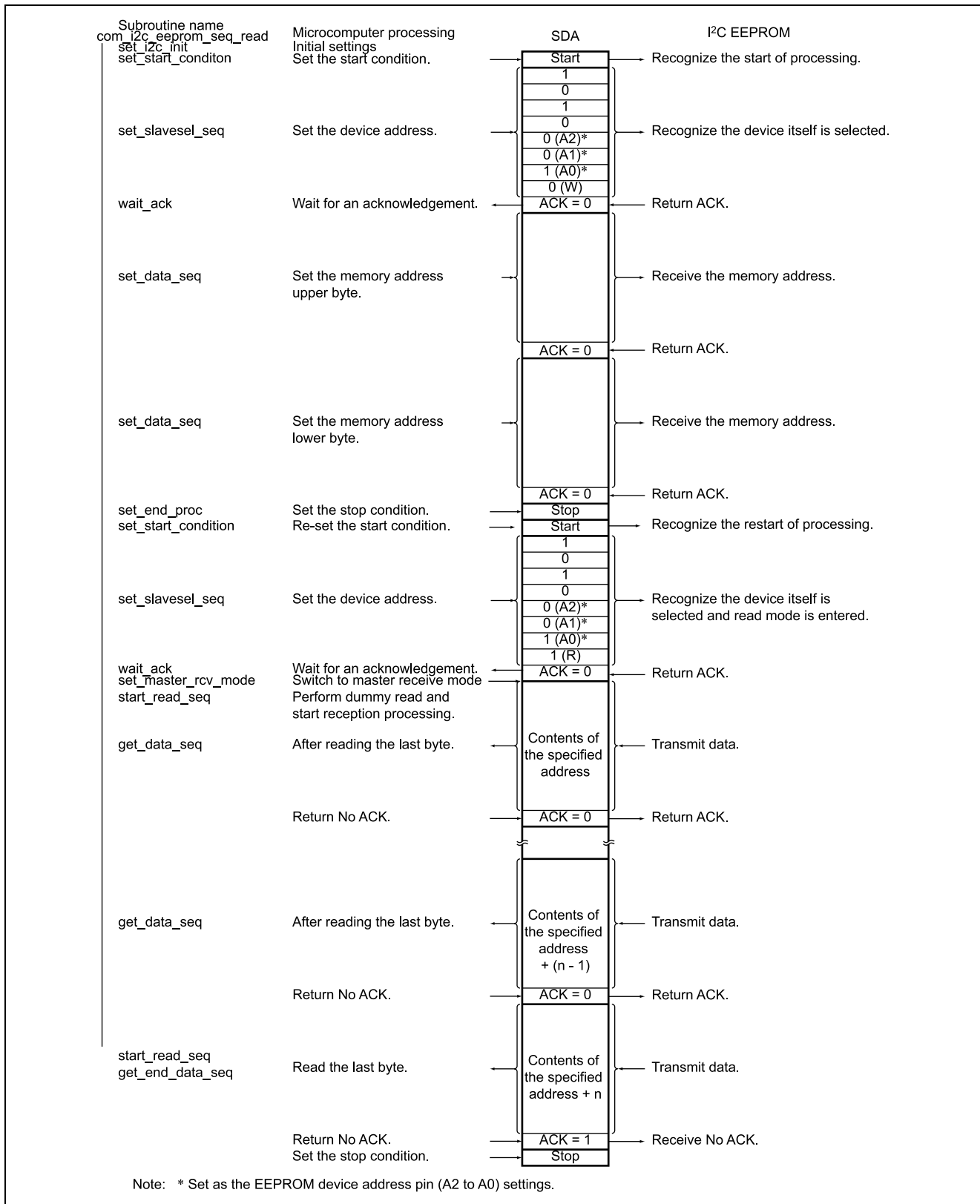
### 2. One byte of data is read from the I<sup>2</sup>C EEPROM.



### 3. Data is continuously written to the I<sup>2</sup>C EEPROM.



### 4. Data is continuously read from the I<sup>2</sup>C EEPROM.



### 3.6 List of Registers Used

The internal registers of the H8 microcomputer used in the sample program are listed below. For detailed information, refer to the H8/3664 Group Hardware Manual.

#### 1. I<sup>2</sup>C-related registers

| Name   | Summary   |
|--|---|
| I <sup>2</sup> C bus data register (ICDR)    | 8-bit read/write register which functions as a transmission data register during transmission, and as a reception data register during reception. |
| Slave address register (SAR)                 | Sets the slave address and transfer format.   |
| Second slave address register (SARX)         | Sets the second slave address and transfer format.  |
| I <sup>2</sup> C bus mode register (ICMR)    | Sets the transfer format and transfer rate. Can only be accessed when the ICE bit of ICCR is 1.   |
| I <sup>2</sup> C bus control register (ICCR) | I <sup>2</sup> C bus interface control bits and interrupt request flags.  |
| I <sup>2</sup> C bus status register (ICSR)  | Status flags  |
| Timer serial control register (TSCR)         | 8-bit read/write register which controls the operation mode.  |

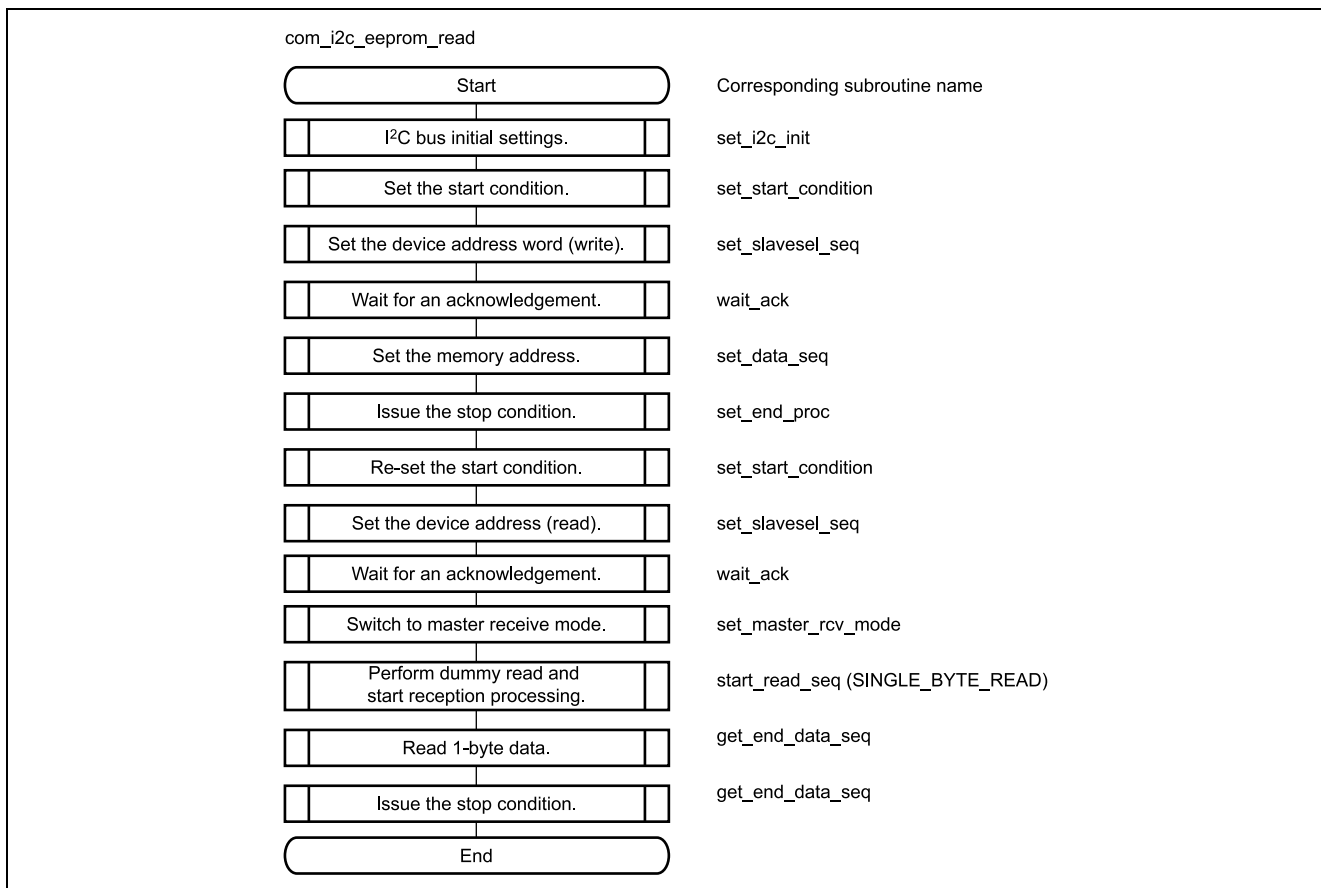
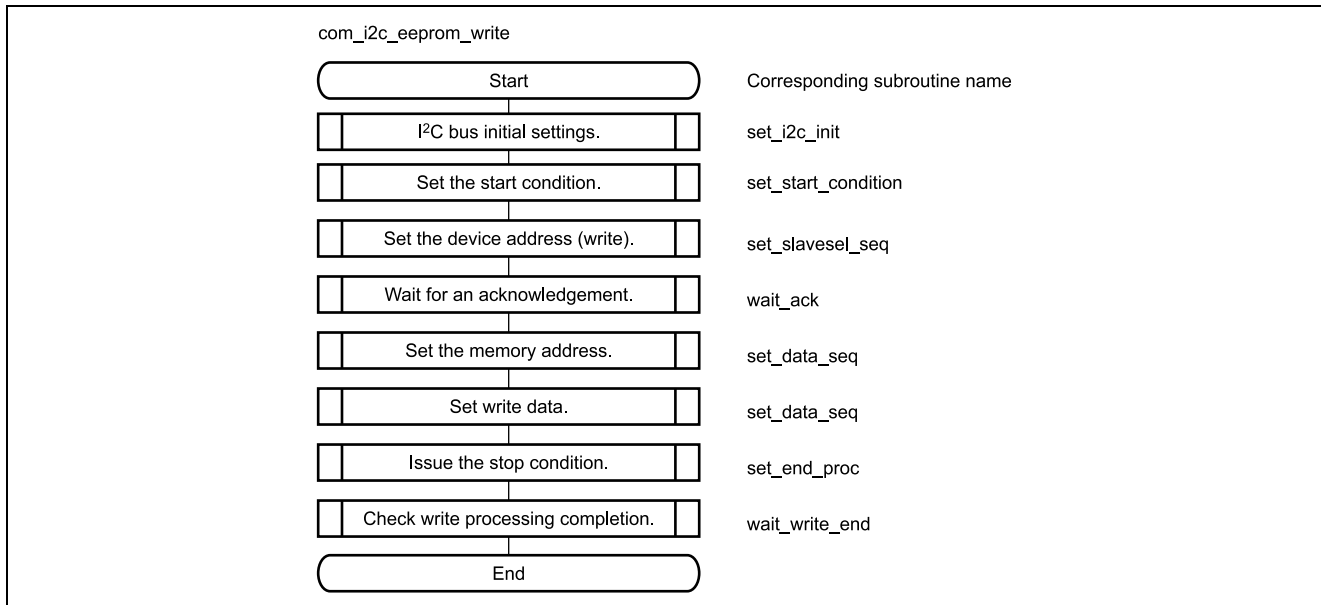
#### 2. Timer W-related registers

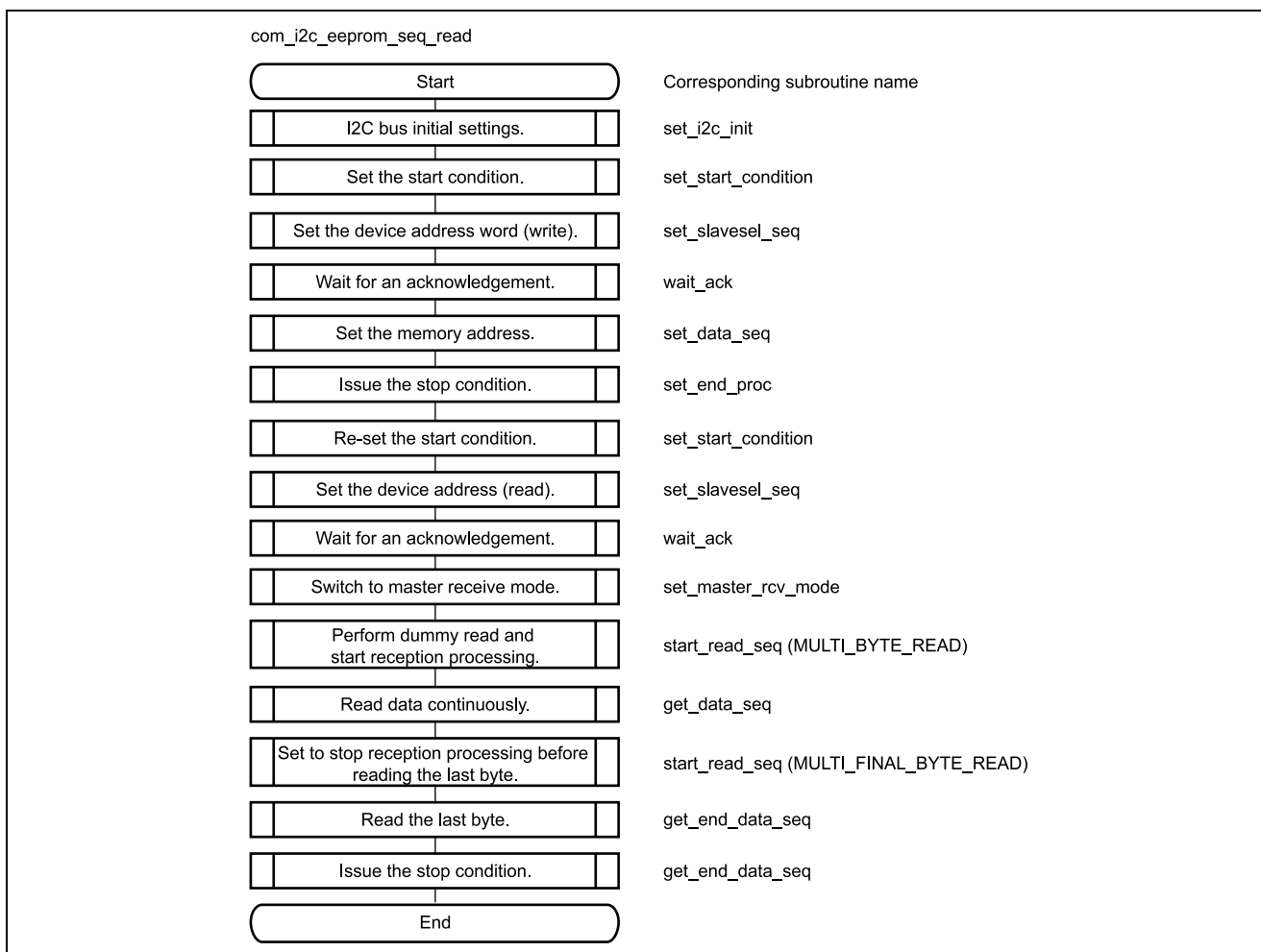
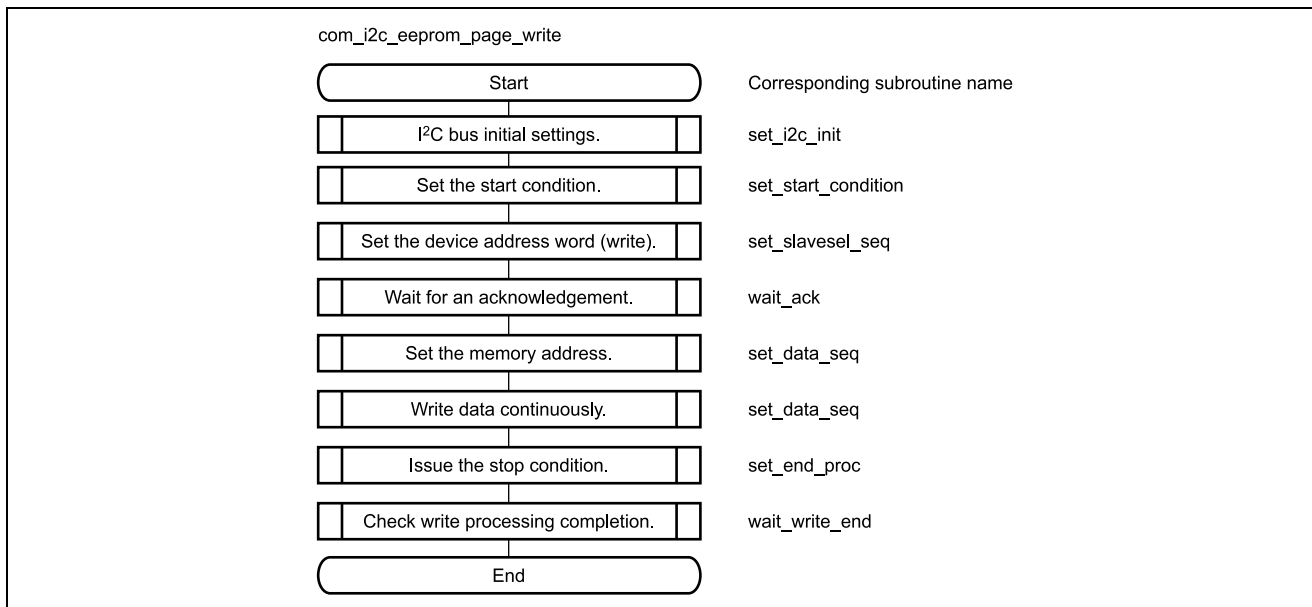
Timer W has various functions, but in the sample program it uses the GRA register compare-match function to generate an interrupt every 10 ms.

| Name  | Summary  |
|---|--|
| Timer mode register W (TMRW)                      | Selects the general register functions, timer output mode, etc.  |
| Timer control register W (TCRW)                   | Selects the TCNT counter clock, counter clear conditions, and timer initial output level settings.   |
| Timer interrupt enable register W (TIERW)         | Controls timer W interrupt requests.   |
| Timer I/O control register 0 (TIOR0)              | Selects the functions of the GRA and GRB and of the FTIOA and FTIOB pins.  |
| Timer I/O control register 1 (TIOR1)              | Selects the functions of the GRC and GRD and of the FTIOC and FTIOD pins. Not used in this sample program.   |
| Timer counter (TCNT)                              | 16-bit read/write count-up counters.   |
| General registers A, B, C, D (GRA, GRB, GRC, GRD) | 16-bit read/write registers which can be used as either output-compare registers or as input-capture registers.<br>16-bit read/write registers which can be used as either output-compare registers or as input-capture registers. |

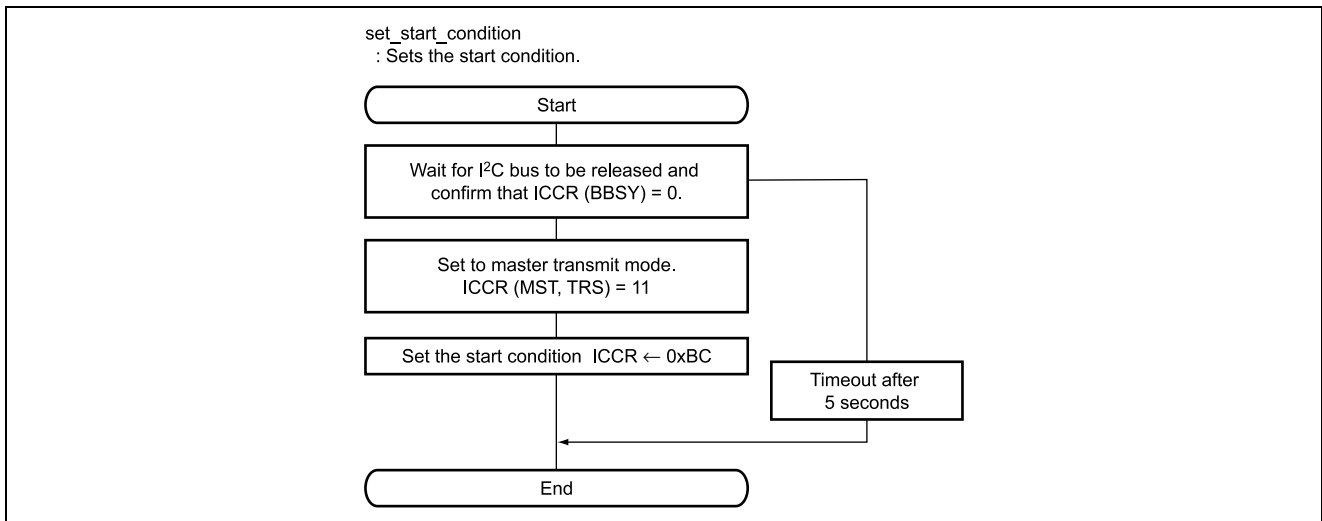
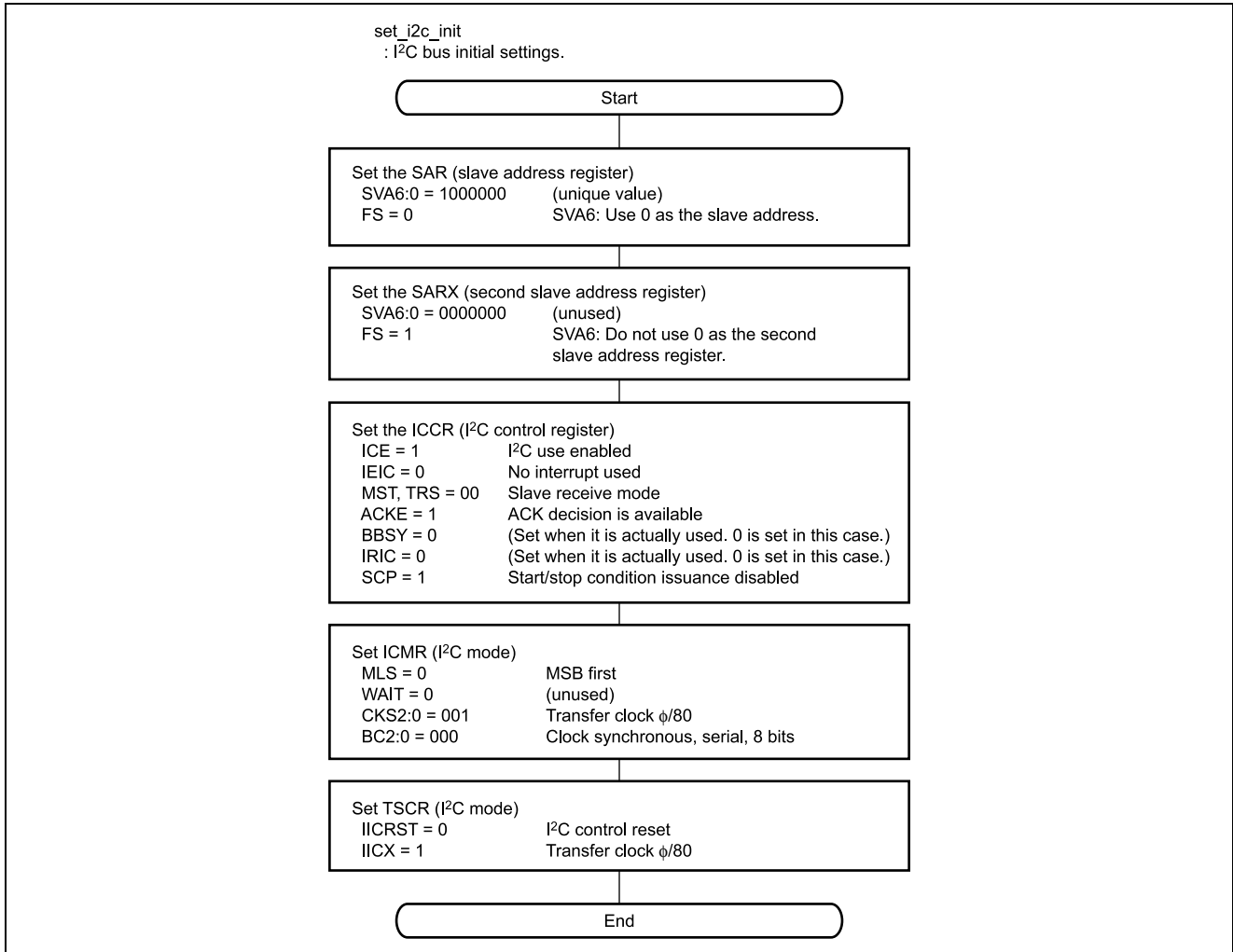
### 3.7 Flowcharts

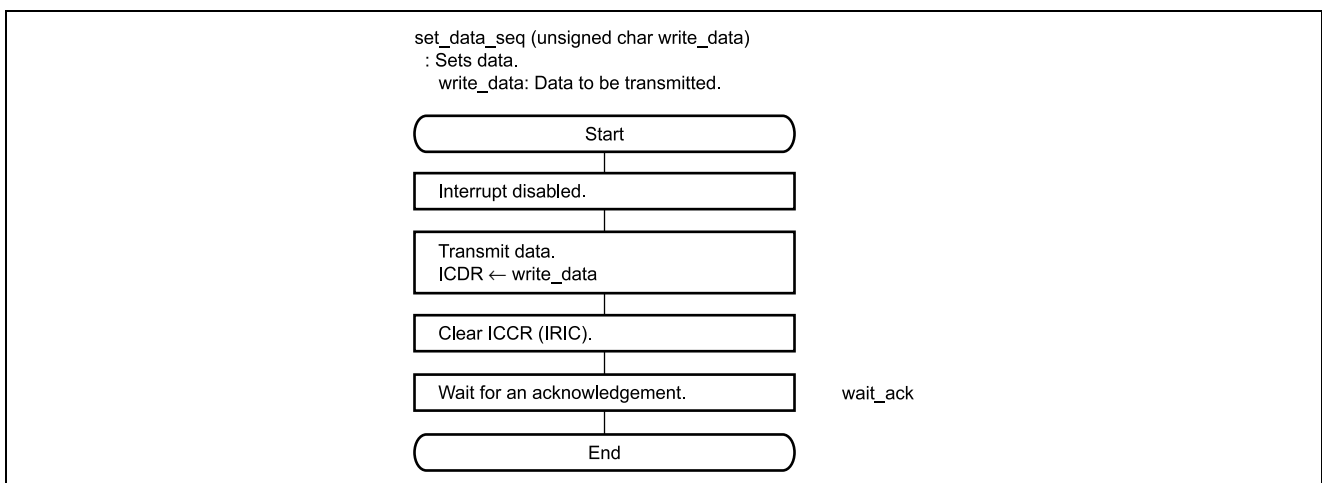
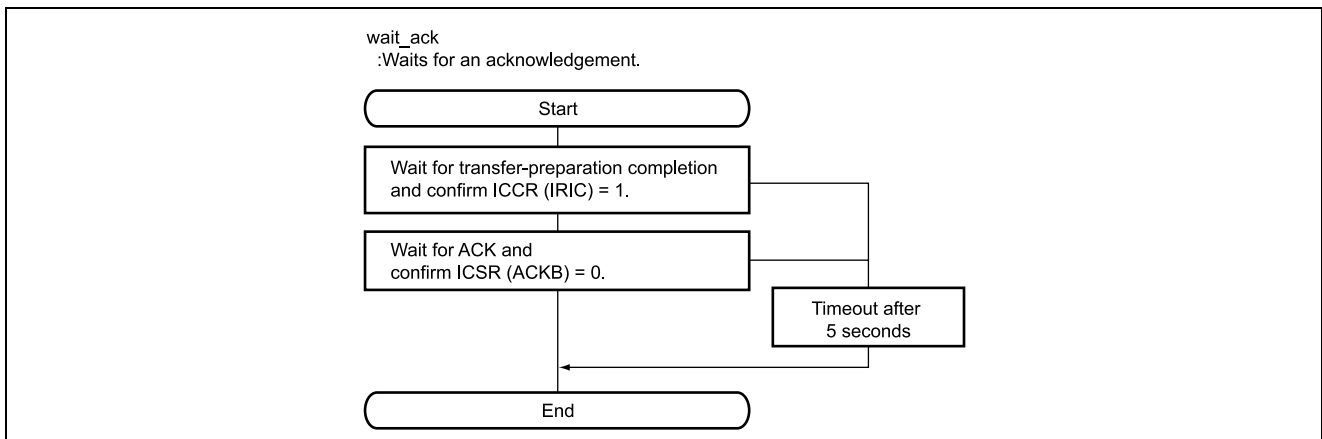
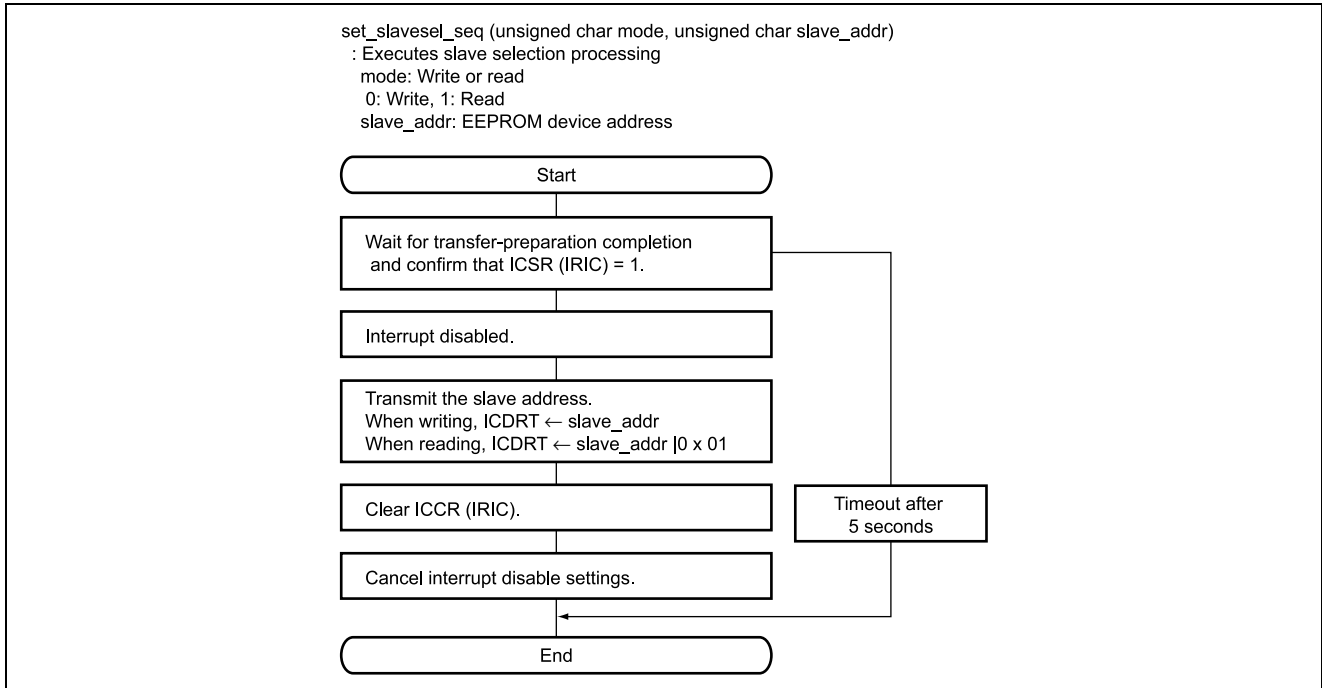
The program processing flow is shown below.

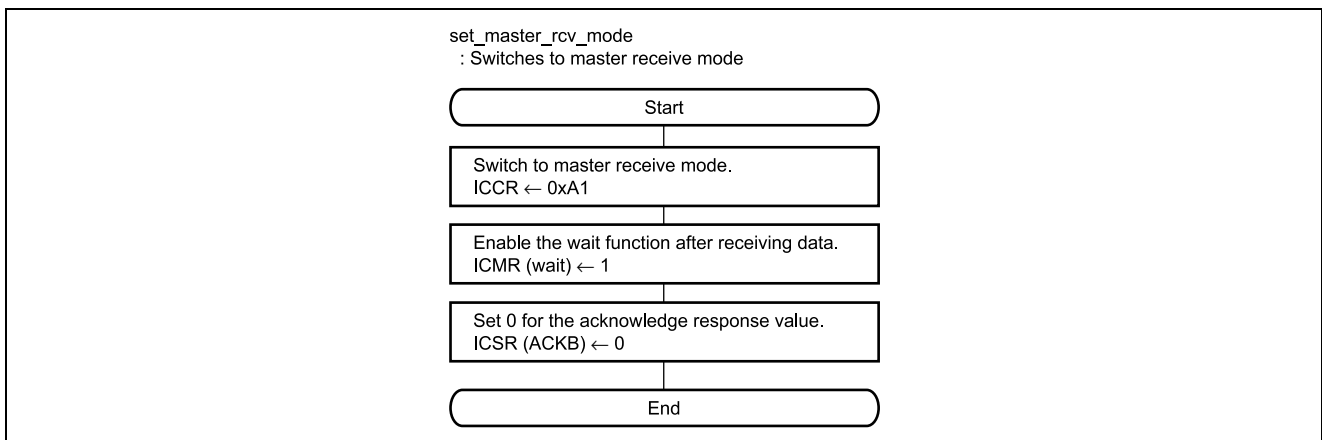
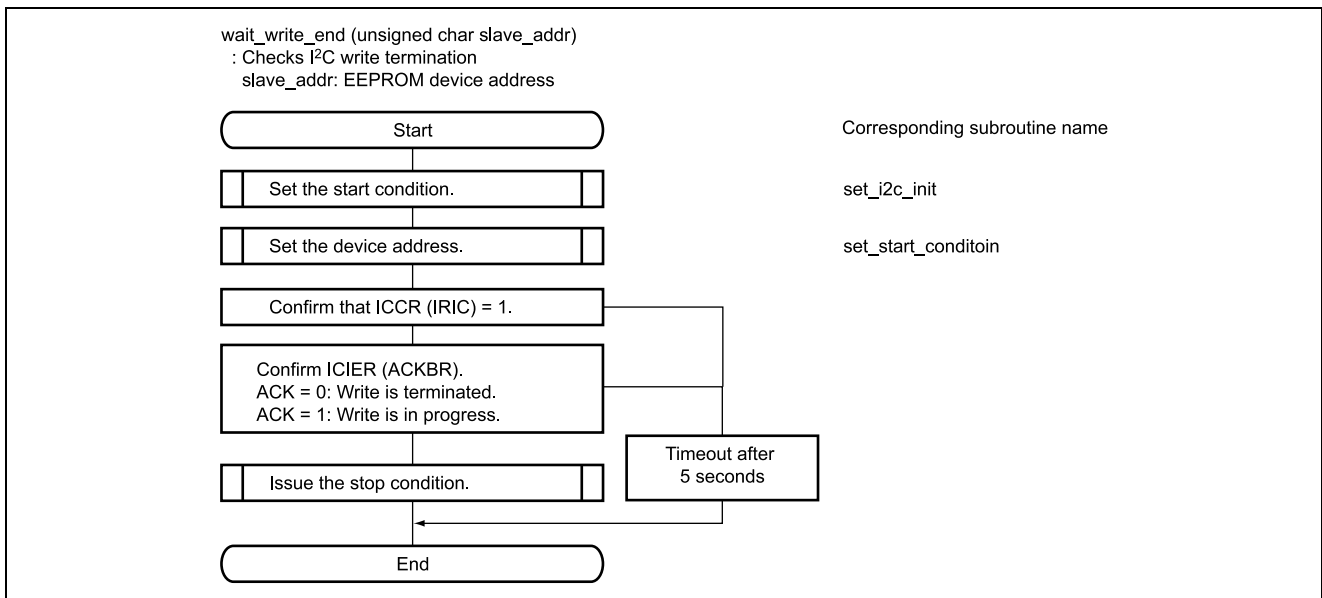
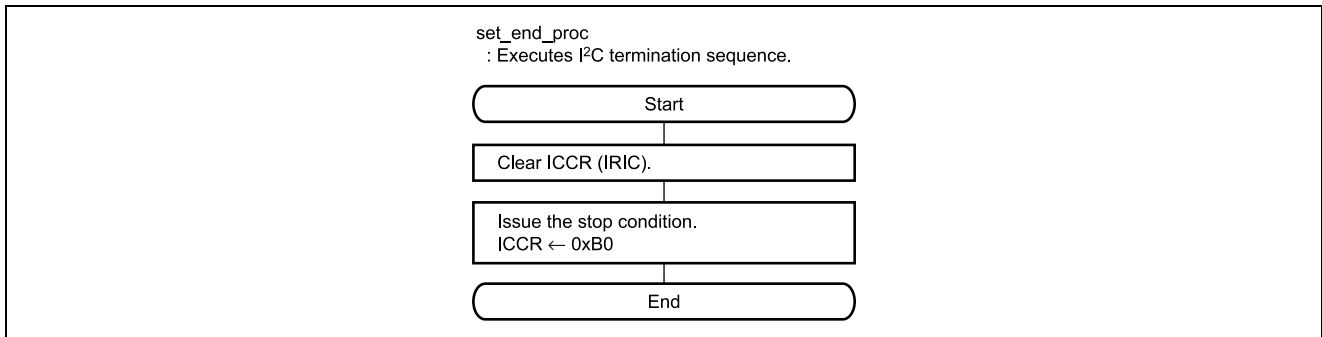




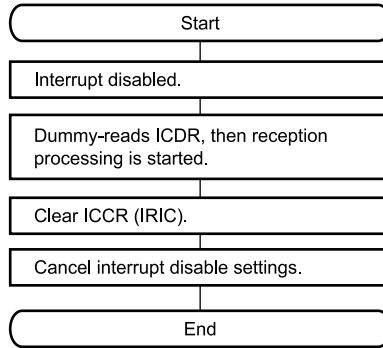




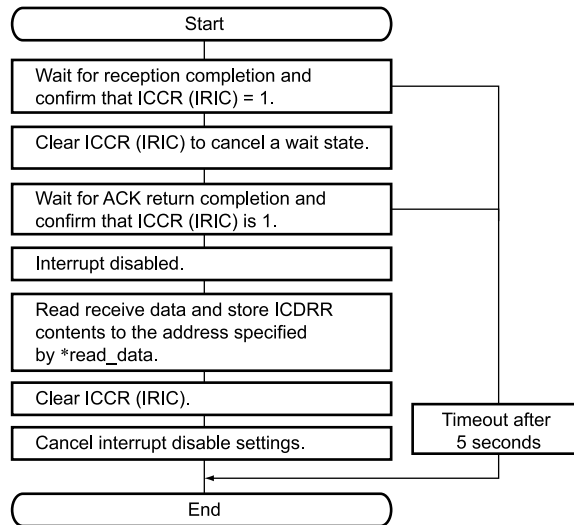


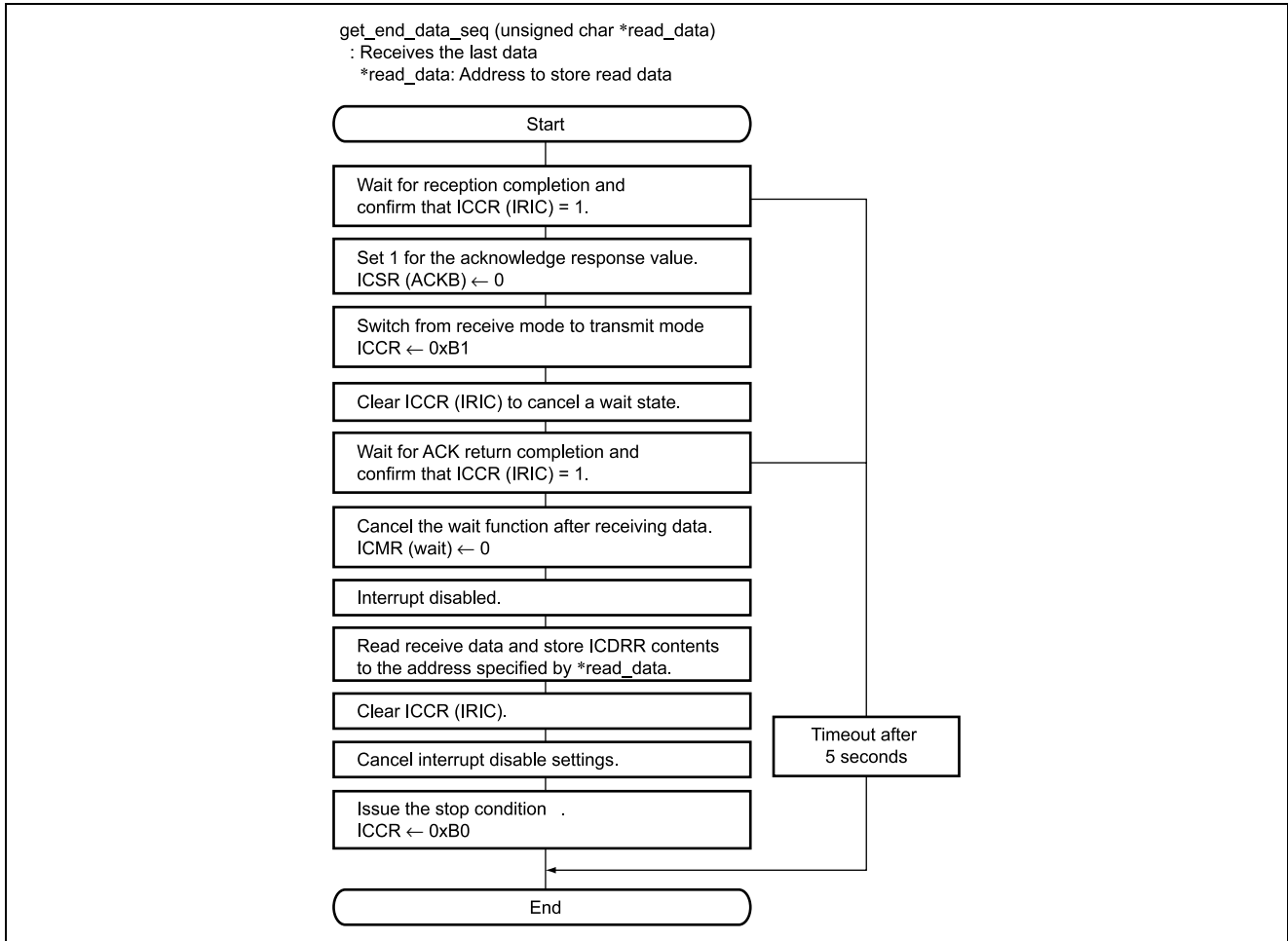


start\_read\_seq  
: Performs dummy read at the beginning of read processing.



get\_data\_seq (unsigned char \*read\_data)  
: Receives data  
\*read\_data: Address to store read data





### 3.8 Program Listing

```

/* ----- */
/* ----- */
/* 1. Sample Program 1-A #define directives ----- */
/* ----- */
/* ----- */
/* ----- */
/*****
/*   For I2CEEPROM access                               */
/*****
#define   CMD_WRITE_OPERATION      0
#define   DATA_READ_OPERATION     1

#define   MULTI_BYTE_READ         0
#define   SINGLE_BYTE_READ       1
#define   MULTI_FINAL_BYTE_READ   2

/*****
/*   I2CEEPROM access error code (other than 0)         */
/*****
#define   I2C_BBSY_TOUT           1
#define   I2C_IRIC_TOUT           2
#define   I2C_ACKB_TOUT           3
#define   I2C_IRTR_TOUT           4
#define   I2C_TRS_TOUT            5

/* ----- */
/* ----- */
/* 2. Sample program 1-B Prototype declaration ----- */
/* ----- */
/* ----- */
/*****
/*   I2C BUS access processing                               */
/*****
void set_i2c_init( );
unsigned int set_start_condition( );
unsigned int wait_ack();
unsigned int set_slavesel_seq (unsigned char mode ,unsigned char slave_addr ) ;
unsigned int set_data_seq(unsigned char write_data);
unsigned int set_end_proc ( );
unsigned int set_master_rcv_mode ( );
unsigned int wait_write_end (unsigned char device_addr_code ) ;

void start_read_seq ( ) ;
unsigned int get_end_data_seq (unsigned char *read_data);
unsigned int get_data_seq (unsigned char *read_data);

unsigned int com_i2c_eeprom_read( unsigned char device_addr_code , unsigned int rom_addr , unsigned char *rom_data );
unsigned int com_i2c_eeprom_write( unsigned char device_addr_code , unsigned int rom_addr , unsigned char rom_data );
unsigned int com_i2c_eeprom_seq_read
    ( unsigned char device_addr_code , unsigned int rom_addr , unsigned int rom_length , unsigned char *rom_data ) ;
unsigned int com_i2c_eeprom_page_write
    ( unsigned char device_addr_code , unsigned int rom_addr , unsigned int rom_length , unsigned char *rom_data ) ;

```

```

/* ----- */
/* ----- */
/* 3. Sample program 1-C Source codes----- */
/* ----- */
/* ----- */
/*****
/*****
/*****
/*
/*          I2C EEPROM control
/*
/*
/*****
/*****
/*****

/* 1. Module name :set_i2c_init
/* 2. Function overview: Set initial settings prior to I2 access
/* . History of revisions: REV Date created/revised Created/revised by Revision contents
/*
/*          000      2002.12.14      Ueda          New
/*****
void set_i2c_init( )
{
/*****
/* SAR          Sets the slave address register
/*          SVA6:0 = 1000000 (Unique value)
/*          FS    = 0 VA6:0 is used as the slave address.
/*****
/* ##(program note)#####
/* ## SVA6:0 is used in the slave mode. It should be set to a unique address that is different ##
/* ## from the addresses used for other slave devices connected to the I2C bus ##
/* #####
IIC.SAR.BYTE= 0x80 ;

/*****
/* SARX        Sets the second slave address register
/*          SVAX6:0 = 0000000 (unused)
/*          FS    = 1 SVAX6: Do not use 0 as the second slave address.
/*
/*
/*****
IIC.SARX.BYTE= 0x01 ;

/*****
/* ICCR        Sets the I2C control register
/*          ICE   = 1 I2C use enabled
/*          IEIC  = 0 Interrupts not used
/*          MST,TRS = 00 Slave receive mode
/*          ACKE  = 1 ACK decision is enabled
/*          BBSY  = 0 (set when it is actually used. 0 is set in this case)
/*          IRIC  = 0 (set when it is actually used. 0 is set in this case)
/*          SCP   = 1 Start/stop condition issuance disabled
/*****
IIC.ICCR.BYTE = 0x89 ;

```

```

/*****
/*  ICMR      Sets I2C mode                                     */
/*      MLS      = 0 MSB first                                 */
/*      WAIT     = 0 (unused)                                 */
/*      CKS2:0   = 001 Transfer clock  $\phi$ /80                 */
/*      BC2:0    = 000 Clock synchronous, serial, 8 bits     */
/*****
IIC.ICMR.BYTE= 0x08 ;
/* ##(program note)##### */
/* ## The value set for CKS2:0 should be modified depending on the necessary transfer rate.      ## */
/* ## For details, refer to the H8/3687 Hardware Manual.      ## */
/* ##### */

/*****
/*  TSCR      Sets I2C mode                                     */
/*      IICRST   = 0 Resets the I2C control                   */
/*      IICX     = 1 Transfer clock  $\phi$ /80                     */
/*****
TSCR.BYTE= 0x01 ;
/* ##(program note)##### */
/* ## The value set for IICX should be modified depending on the necessary transfer rate.      ## */
/* ## For details, refer to the H8/3687 Hardware Manual.      ## */
/* ##### */

}

/*****
/*  1. Module name: set_start_condition                         */
/*  2. Function overview: Sets the I2C start condition.        */
/*  3. History of revisions: REV  Date created/revised  Created/revised by  Revision contents  */
/*                               000      2002.12.14      Ueda                New                */
/*****
unsigned int set_start_condition( )
{
    int ret , timer_wk;

    ret = NORMAL_END ;

    /*****
    /*  Confirms that ICCR (BBSY) = 0.                          */
    /*****
    com_timer.wait_100ms_scan = 50 ;
    while (IIC.ICCR.BIT.BBSY == 1){
        timer_wk = com_timer.wait_100ms_scan ;
        if (timer_wk == 0){
            ret = I2C_BBSY_TOUT;
            goto exit ;
        }

        #ifdef UT
            IIC.ICCR.BIT.BBSY = 0;
        #endif
    }
}

```



```

/*****
/* Sets to master transmit mode */
/*****
IIC.ICCR.BYTE = 0xB9 ; /* Set to master transmit mode */
/* ##(program note)##### */
/* ## Make sure that the ACKE (ACK decision is enabled) is not reset. ## */
/* ##### */

/*****
/* Sets the start condition */
/*****
IIC.ICCR.BYTE = 0xBC ;
/* ##(program note)##### */
/* ## The settings for bits 2 and 0, which set the start condition, have to be set simultaneously, ## */
/* ## so they must be written in byte units. ## */
/* ## Note that if these are set one bit at a time, the start condition may not be set properly. ## */
/* ##### */
/* ##(program note)##### */
/* ## Make sure that the ACKE (ACK decision is enabled) is not reset. ## */
/* ##### */

exit:
    return (ret);

}

/*****
/* 1. Module name :wait_ack */
/* 2. Function overview: Waits for the I2C ACK. */
/* 3. History of revisions: REV Date created/revised Created/ revised by Revision contents */
/* 000 2002.12.14 Ueda New */
/*****
unsigned int wait_ack ()
{
    int ret , timer_wk;

    ret = NORMAL_END ;

/*****
/* Confirms that ICCR (IRIC) = 1. */
/*****
com_timer.wait_100ms_scan = 50 ;
while (IIC.ICCR.BIT.IRIC == 0){ /* Waits until preparation */
/* for transfer has been completed. */

    timer_wk = com_timer.wait_100ms_scan ;
    if (timer_wk == 0){ /* If the value remains 1 for 5 seconds, */
/* exit with an error. */

        ret = I2C_IRIC_TOUT; /* Abnormal termination (timeout) */
        goto exit ;
    }

#ifdef UT
    IIC.ICCR.BIT.IRIC = 1 ;
#endif
}
}

```

```

/*****
/*  Confirms that ICSR (ACKB) = 0.                                     */
/*****
com_timer.wait_100ms_scan = 50 ;
while (IIC.ICSR.BIT.ACKB == 1){                                     /* Waits for ACKB = 0 to be returned.          */
    timer_wk = com_timer.wait_100ms_scan ;
    if (timer_wk == 0){                                           /* If the value remains 1 for 5 seconds,       */
                                                                    /* exit with an error.                         */
                                                                    /* Abnormal termination (timeout)            */
        ret = I2C_ACKB_TOUT;
        goto exit ;
    }

    #ifdef UT
        IIC.ICSR.BIT.ACKB = 0 ;
    #endif
}

exit:
    return (ret);
}

/*****
/*  1. Module name: set_slavesel_seq                                 */
/*  2. Function overview: Executes I2C slave selection processing.   */
/*  3. History of revisions: REV  Date created/revised   Created/revised by   Revision contents   */
/*                               000    2002.12.14         Ueda                      New                */
/*****
unsigned int set_slavesel_seq (unsigned char mode ,unsigned char slave_addr )
{
    int ret , timer_wk;
    unsigned char write_data ;

    ret = NORMAL_END ;

/*****
/*  Confirms that ICCR (IRIC) = 1.                                     */
/*****
com_timer.wait_100ms_scan = 50 ;
while (IIC.ICCR.BIT.IRIC == 0){                                     /* Waits until preparation                      */
                                                                    /* for transfer has been completed.           */
    timer_wk = com_timer.wait_100ms_scan ;
    if (timer_wk == 0){                                           /* If the value remains 1 for 5 seconds,       */
                                                                    /* exit with an error.                         */
                                                                    /* Abnormal termination (timeout)            */
        ret = I2C_IRIC_TOUT;
        goto exit ;
    }

    #ifdef UT
        IIC.ICCR.BIT.IRIC = 1 ;
    #endif
}
}

```

```

/*****
/* Sets the slave address */
/*****
if (mode == DATA_READ_OPERATION){
    slave_addr = slave_addr | 0x01 ;
}
/*****
/* Disables interrupts */
/*****
set_imask_ccr(1); /* Disables interrupts */

/*****
/* Writes data */
/*****
IIC.ICDR = slave_addr ;

/*****
/* Clears ICCR (IRIC) */
/*****
IIC.ICCR.BIT.IRIC = 0 ;
/* ##(program note)##### */
/* ## The ICDR write and IRIC clear operations should be written continuously during the time ## */
/* ## that the transfer time of one byte of data has not elapsed. ## */
/* ## For this reason, all interrupts should be disabled while these operations are being carried out. ## */
/* ##### */

/*****
/* Cancels interrupt disable */
/*****
set_imask_ccr(0); /* Cancels interrupt disable */

exit:
return (ret);

}

/*****
/* 1. Module name: set_data_seq */
/* 2. Function overview: Executes I2C data setting processing */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/* 000 2002.12.14 Ueda New */
/*****
unsigned int set_data_seq (unsigned char write_data)
{
    int ret , timer_wk;

    ret = NORMAL_END ;

/*****
/* Disables interrupts */
/*****
set_imask_ccr(1); /* Disables interrupts */

/*****
/* Writes data */
/*****
IIC.ICDR = write_data ;

```

```

/*****
/*  Clears ICCR (IRIC)
*/
/*****
IIC.ICCR.BIT.IRIC = 0 ;
    /* ##(program note)##### */
    /* ## The ICDR Write and IRIC Clear operations should be written continuously during the time    ## */
    /* ## that the transfer time of one byte of data has not elapsed.                            ## */
    /* ## For this reason, all interrupts should be disabled while these operations are being carried out.  ## */
    /* ##### */
/*****
/*  Cancels interrupt disable
*/
/*****
set_imask_ccr(0);
/* Cancels interrupt disable
*/

/*****
/*  Waits for an acknowledgement
*/
/*****
ret = wait_ack() ;
if (ret !=0) { goto exit ;}

exit:
    return (ret);
}
/*****
/*  1. Module name: set_end_proc
*/
/*  2. Function overview: Executes an I2C exit sequence
*/
/*  3. History of revisions: REV  Date created/revised  Created/revised by  Revision contents
*/
/*          000          2002.12.14          Ueda          New
*/
/*****
unsigned int set_end_proc ()
{
    int ret , timer_wk;

    ret = NORMAL_END ;

/*****
/*  Clears ICCR (IRIC)
*/
/*****
IIC.ICCR.BIT.IRIC = 0 ;

/*****
/*  Issues the stop condition
*/
/*****
IIC.ICCR.BYTE = 0xB0 ;

exit:
    return (ret);
}

```

```

/*****
/* 1. Module name: wait_write_end */
/* 2. Function overview: Checks the completion of I2C write */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/* 000 2002.12.14 Ueda New */
*****/
unsigned int wait_write_end (unsigned char slave_addr )
{
    int ret , timer_wk;
    unsigned char ack_status ;

    ret = NORMAL_END ;

    com_timer.wait_100ms = 50 ;

    do{
        /*****
        /* Sets the start condition */
        *****/
        ret = set_start_condition() ; /* Sets the start condition */
        if (ret !=0) { goto exit ;}

        /*****
        /* Sets the device address word (write) */
        *****/
        ret = set_slavesel_seq ( CMD_WRITE_OPERATION , slave_addr ) ;
        if (ret !=0) { goto exit ;}

        /*****
        /* Confirms that ICCR (IRIC) = 1 */
        *****/
        com_timer.wait_100ms_scan = 50 ;
        while (IIC.ICCR.BIT.IRIC == 0){ /* Waits until the preparation */
                                        /* for transfer has been completed. */

            timer_wk = com_timer.wait_100ms_scan ;
            if (timer_wk == 0){ /* If the value remains 1 for 5 seconds, */
                                /* exit with an error. */
                ret = I2C_IRIC_TOUT; /* Abnormal termination (timeout) */
                goto exit ;
            }

            #ifndef UT
                IIC.ICCR.BIT.IRIC = 1 ;
            #endif

        }

        /*****
        /* Checks ICIBR (ACKBR): ACK = 0 The write has completed ACK = 1 The write is in progress */
        *****/
        if (com_timer.wait_100ms == 0){ /* If the value remains 1 for 5 seconds, */
                                        /* exit with an error. */
            ret = I2C_ACKB_TOUT; /* Abnormal termination (timeout) */
            goto exit ;
        }

        #ifndef UT
            IIC.ICSR.BIT.ACKB = 1 ;
        #endif
        ack_status = IIC.ICSR.BIT.ACKB ;
    }
}

```

```

/*****
/*   Issues the stop condition                                     */
/*****
ret = set_end_proc ( ) ;
    if (ret !=0) { goto exit ;}

} while (ack_status == 1) ;                               /* Enters a loop while ACK = 1 */

exit:
return (ret);

}

/*****
/*  1. Module name: set_master_rcv_mode                           */
/*  2. Function overview: Switches to the master receive mode    */
/*  3. History of revisions: REV  Date created/revised   Created/revised by   Revision contents   */
/*                               000      2002.12.14      Ueda                      New                */
/*****
unsigned int set_master_rcv_mode ()
{
    int ret , timer_wk;
    unsigned char dummy_data ;

    ret = NORMAL_END ;

/*****
/*   Switches to the master receive mode                         */
/*****
IIC.ICCR.BYTE = 0xA1      ;

/*****
/*   Sets an ICMR (WAIT)                                        */
/*****
IIC.ICMR.BIT.WAIT = 1 ;

/*****
/*   Clears ICSR (ACKB) to 0 (sets Acknowledge data)           */
/*****
IIC.ICSR.BIT.ACKB = 0 ;

exit:
return (ret);
}

```

```

/*****
/* 1. Module name: start_read_seq */
/* 2. Function overview: Carries out a dummy read at the start of read processing */
/* . History of revisions: REV Date created/revised Created/revised by Revision contents */
/* 000 2002.12.14 Ueda New */
/*****
void start_read_seq ()
{
    unsigned char dummy_data ;

    /*****
    /* Disables interrupts */
    /*****
    set_imask_ccr(1); /* Disables interrupts */

    /*****
    /* Initiates reception when a dummy read is carried out */
    /*****
    dummy_data = IIC.ICDR ;
    /* ##(program note)##### */
    /* ## Reception begins when a dummy read is carried out, and data is sent from the device synchronized to the SCL. ## */
    /* ## A Low level signal is sent to the device synchronized to the ninth SCL, ## */
    /* ## in response to the ICSR (ACKB) previously set to 0. ## */
    /* ##### */

    /*****
    /* Clears ICCR (IRIC) */
    /*****
    IIC.ICCR.BIT.IRIC = 0 ;
    /* ##(program note)##### */
    /* ## The ICDR Write and IRIC Clear operations should be written continuously during the time ## */
    /* ## that the transfer time of one byte of data has not elapsed. ## */
    /* ## For this reason, all interrupts should be disabled while these operations are being carried out. ## */
    /* ##### */

    /*****
    /* Cancels interrupt disable */
    /*****
    set_imask_ccr(0); /* Cancels interrupt disable */
}

```

```

/*****
/* 1. Module name: get_data_seq */
/* 2. Function overview: Reads data from the I2C target device */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/*           000      2002.12.14      Ueda                New                */
*****/
unsigned int get_data_seq (unsigned char *read_data)
{
    int ret , timer_wk;
    unsigned char dummy_data ;

    ret = NORMAL_END ;

    /*****
    /* Confirms that ICCR (IRIC) = 1 */
    *****/
    com_timer.wait_100ms_scan = 50 ;
    while (IIC.ICCR.BIT.IRIC == 0){
        /* Waits until the preparation */
        /* for transfer has been completed. */
        timer_wk = com_timer.wait_100ms_scan ;
        if (timer_wk == 0){
            /* If the value remains 1 for 5 seconds, */
            /* exit with an error. */
            ret = I2C_IRIC_TOUT;
            /* Abnormal termination (timeout) */
            goto exit ;
        }

        #ifdef UT
            IIC.ICCR.BIT.IRIC = 1 ;
        #endif
    }

    /*****
    /* Clears ICCR (IRIC) (to cancel Wait status) */
    *****/
    IIC.ICCR.BIT.IRIC = 0 ;

    /*****
    /* Confirms that ICCR (IRIC) = 1 */
    *****/
    com_timer.wait_100ms_scan = 50 ;
    while (IIC.ICCR.BIT.IRIC == 0){
        /* Waits until the preparation */
        /* for transfer has been completed. */
        timer_wk = com_timer.wait_100ms_scan ;
        if (timer_wk == 0){
            /* If the value remains 1 for 5 seconds, */
            /* exit with an error. */
            ret = I2C_IRIC_TOUT;
            /* Abnormal termination (timeout) */
            goto exit ;
        }

        #ifdef UT
            IIC.ICCR.BIT.IRIC = 1 ;
        #endif
    }
}

```



```

/*****
/* Disables interrupts */
/*****
set_imask_ccr(1); /* Disables interrupts */

/*****
/* Reads received data */
/*****
*read_data = IIC.ICDR ; /* data read */

/*****
/* Clears ICCR (IRIC) */
/*****
IIC.ICCR.BIT.IRIC = 0 ;
/* ##(program note)##### */
/* ## The ICDR Write and IRIC Clear operations should be written continuously during the time ## */
/* ## that the transfer time of one byte of data has not elapsed. ## */
/* ## For this reason, all interrupts should be disabled while these operations are being carried out. ## */
/* ##### */

/*****
/* Cancels interrupt disable */
/*****
set_imask_ccr(0); /* Cancels interrupt disable */

exit:
return (ret);
}

/*****
/* 11. Module name: get_end_data_seq */
/* 2. Function overview: Reads data from the I2C target device */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/* 000 2002.12.14 Ueda New */
/*****
unsigned int get_end_data_seq (unsigned char *read_data)
{
int ret , timer_wk;
unsigned char dummy_data ;

ret = NORMAL_END ;

/*****
/* Confirms that ICCR (IRIC) = 1 */
/*****
com_timer.wait_100ms_scan = 50 ;
while (IIC.ICCR.BIT.IRIC == 0){ /* Waits until preparation */
/* for transfer has been completed */

timer_wk = com_timer.wait_100ms_scan ;
if (timer_wk == 0){ /* If the value remains 1 for 5 seconds, */
/* exit with an error. */

ret = I2C_IRIC_TOUT; /* Abnormal termination (timeout) */
goto exit ;

}

#ifdef UT
IIC.ICCR.BIT.IRIC = 1 ;
#endif
}
}

```

```

/*****
/* Sets value for ACK returned after data reception to "1" (NOACK) */
/*****
IIC.ICSR.BIT.ACKB = 1 ;

/*****
/* Switches from receive mode to transmit mode */
/*****
IIC.ICCR.BYTE = 0xB1 ;

/*****
/* Clears ICCR (IRIC) (to cancel Wait status) */
/*****
IIC.ICCR.BIT.IRIC = 0 ;

/*****
/* Confirms that ICCR (IRIC) = 1 */
/*****
com_timer.wait_100ms_scan = 50 ;
while (IIC.ICCR.BIT.IRIC == 0){
    /* Waits until the preparation */
    /* for transfer has been completed. */

    timer_wk = com_timer.wait_100ms_scan ;
    if (timer_wk == 0){
        /* If the value remains 1 for 5 seconds, */
        /* exit with an error. */
        ret = I2C_IRIC_TOUT;
        goto exit ;
        /* Abnormal termination (timeout) */
    }

    #ifdef UT
        IIC.ICCR.BIT.IRIC = 1 ;
    #endif
}

/*****
/* Resets ICMR (WAIT) */
/*****
IIC.ICMR.BIT.WAIT = 0 ;

/*****
/* Disables interrupts */
/*****
set_imask_ccr(1);
/* Disables interrupts */

/*****
/* Reads received data */
/*****
*read_data = IIC.ICDR ;
/* data read */

/*****
/* Clears ICCR (IRIC) (to cancel Wait status) */
/*****
IIC.ICCR.BIT.IRIC = 0 ;
/* ## (program note)##### */
/* ## The ICDR Write and IRIC Clear operations should be written continuously during the time ## */
/* ## that the transfer time of one byte of data has not elapsed. ## */
/* ## For this reason, all interrupts should be disabled while these operations are being carried out. ## */
/* ##### */

/*****
/* Cancels interrupt disable */
/*****
set_imask_ccr(0);
/* Cancels interrupt disable */

```

```

/*****
/* Clears ICCR (IRIC) and issues the stop condition */
/*****
IIC.ICCR.BYTE = 0xB0 ;

exit:

    return (ret);
}

/*****
/* 1. Module name: com_i2c_eeprom_write */
/* 2. Function overview: Writes 1 byte data to I2CEEPROM. */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/*          000          2002.12.14          Ueda          New */
/*****
unsigned int com_i2c_eeprom_write ( unsigned char slave_addr , unsigned int rom_addr , unsigned char rom_data )
{
    int ret ;
    union {
        unsigned int    d_int ;
        unsigned char   d_byte[2];
    } buf;

    ret = NORMAL_END ;

    /*****
    /* Initializes the I2C bus. */
    /*****
    set_i2c_init () ;

    /*****
    /* Sets the start condition. */
    /*****
    ret = set_start_condition() ;                               /* Sets the start condition. */
        if (ret !=0) { goto exit ;}

    /*****
    /* Sets the device address word (write). */
    /*****
    ret = set_slavesel_seq ( CMD_WRITE_OPERATION , slave_addr ) ;
        if (ret !=0) { goto exit ;}

    /*****
    /* Waits for an acknowledgement */
    /*****
    ret = wait_ack() ;
        if (ret !=0) { goto exit ;}

    /*****
    /* Sets the memory address. */
    /*****
    buf.d_int = rom_addr ;

    ret = set_data_seq ( buf.d_byte[0] ) ;                       /* 1st Memory address */
        if (ret !=0) { goto exit ;}

    ret = set_data_seq ( buf.d_byte[1] ) ;                       /* 2nd Memory address */
        if (ret !=0) { goto exit ;}
}

```

```

/*****
/* Sets to write data.
*/
/*****
ret = set_data_seq ( rom_data ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Issues the stop condition.
*/
/*****
ret = set_end_proc ( ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Checks write completion.
*/
/*****
ret = wait_write_end ( slave_addr ) ;
    if (ret !=0) { goto exit ;}
/* ##(program note)##### */
/* ## The I2CEEPROM starts write operation after receiving the stop condition.      ## */
/* ## Since the write operation takes a maximum of 15 ms,                          ## */
/* ## the I2CEEPROM checks write completion using the Acknowledge Pooling method.    ## */
/* ##### */

return (ret);

exit:
/*****
/* Issues a reset and stop condition if an error occurs
*/
/*****
set_end_proc ( ) ;
    return (ret);

}

/*****
/* 1. Module name: com_i2c_eeprom_write
*/
/* 2. Function overview: Writes data to I2CEEPROM continuously.
*/
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents
*/
/*          000      2002.12.14      Ueda      New
*/
/*****
unsigned int com_i2c_eeprom_page_write
    ( unsigned char slave_addr , unsigned int rom_addr , unsigned int rom_length , unsigned char *rom_data )
{
    int ret , i ;
    union {
        unsigned int    d_int ;
        unsigned char    d_byte[2];
    } buf;

ret = NORMAL_END ;

/*****
/* Initializes the I2C bus.
*/
/*****
set_i2c_init ( ) ;

/*****
/* Sets the start condition.
*/
/*****
ret = set_start_condition() ;
    if (ret !=0) { goto exit ;}
/* Sets the start condition
*/

```

```

/*****
/* Sets the device address word (write). */
/*****
ret = set_slavesel_seq ( CMD_WRITE_OPERATION , slave_addr ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Waits for an acknowledgement. */
/*****
ret = wait_ack() ;
    if (ret !=0) { goto exit ;}

/*****
/* Sets the memory address. */
/*****
buf.d_int = rom_addr ;

ret = set_data_seq ( buf.d_byte[0] ) ;                               /* 1st Memory address */
    if (ret !=0) { goto exit ;}

ret = set_data_seq ( buf.d_byte[1] ) ;                               /* 2nd Memory address */
    if (ret !=0) { goto exit ;}

/*****
/* Writes data continuously. */
/*****
for (i=0; i< rom_length ; i++){
    buf.d_byte[0] = *rom_data ;
    ret = set_data_seq ( buf.d_byte[0] ) ;
        if (ret !=0) { goto exit ;}
        *rom_data ++ ;
}

/*****
/* Issues the stop condition */
/*****
ret = set_end_proc ( ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Checks write completion. */
/*****
ret = wait_write_end ( slave_addr ) ;
    if (ret !=0) { goto exit ;}
    /* ##(program note)##### */
    /* ## The I2CEEPROM starts write operation after receiving the stop condition. ## */
    /* ## Since the write operation takes a maximum of 15 ms, ## */
    /* ## the I2CEEPROM checks write completion using the Acknowledge Pooling method. ## */
    /* ##### */

return (ret);

exit:
/*****
/* Issues a reset and stop condition if an error occurs */
/*****
set_end_proc ( ) ;
    return (ret);

}

```

```

/*****
/* 1. Module name: com_i2c_eeprom_read */
/* 2. Function overview: Reads 1-byte data from I2CEEPROM. */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/* 000 2002.12.14 Ueda New */
*****/
unsigned int com_i2c_eeprom_read ( unsigned char slave_addr , unsigned int rom_addr , unsigned char *rom_data )
{
    int ret ;
    union {
        unsigned int d_int ;
        unsigned char d_byte[2];
    } buf;

    ret = NORMAL_END ;

/*****
/* Initializes the I2C bus */
*****/
set_i2c_init () ;

/*****
/* Sets the start condition */
*****/
ret = set_start_condition() ; /* Sets the start condition */
    if (ret !=0) { goto exit ;}

/*****
/* Sets the device address word (write). */
*****/
ret = set_slavesel_seq ( CMD_WRITE_OPERATION , slave_addr ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Waits for an acknowledgement */
*****/
ret = wait_ack() ;
    if (ret !=0) { goto exit ;}

/*****
/* Sets the memory address. */
*****/
buf.d_int = rom_addr ;

ret = set_data_seq ( buf.d_byte[0] ) ; /* 1st Memory address */
    if (ret !=0) { goto exit ;}

ret = set_data_seq ( buf.d_byte[1] ) ; /* 2nd Memory address */
    if (ret !=0) { goto exit ;}

/*****
/* Issues the stop condition to bring SDA to high. */
*****/
ret = set_end_proc ( ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Sets the start condition again. */
*****/
ret = set_start_condition() ; /* Sets the start condition */
    if (ret !=0) { goto exit ;}

```

```

/*****
/* Sets the device address word (read). */
/*****
ret = set_slavesel_seq ( DATA_READ_OPERATION , slave_addr ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Waits for an acknowledgement */
/*****
ret = wait_ack() ;
    if (ret !=0) { goto exit ;}

/*****
/* Switches to the master receive mode. */
/*****
ret = set_master_rcv_mode () ;
    if (ret !=0) { goto exit ;}

/*****
/* Carries out a dummy read at the start of data reading. */
/*****
start_read_seq () ;

/*****
/* ues the stop condition after data (1 byte) has been read. */
/*****
ret = get_end_data_seq ( &buf.d_byte[0] ) ;
    if (ret !=0) { goto exit ;}

    *rom_data = buf.d_byte[0] ;

    return (ret);

exit:
/*****
/* Issues a reset and stop condition if an error occurs */
/*****
set_end_proc ( ) ;
    return (ret);

}
/*****
/* 1. Module name: com_i2c_eeprom_seq_read */
/* 2. Function overview: Reads a specified length of data from I2CEEPROM. */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/*          000          2002.12.14          Ueda          New */
/*****
unsigned int com_i2c_eeprom_seq_read
    ( unsigned char slave_addr , unsigned int rom_addr , unsigned int rom_length , unsigned char *rom_data )
{
    int ret , i ;
    union {
        unsigned int    d_int ;
        unsigned char    d_byte[2];
    } buf;

    ret = NORMAL_END ;

/*****
/* Initializes the I2C bus */
/*****
set_i2c_init () ;

```

```

/*****
/* Sets the start condition
/*****
ret = set_start_condition() ; /* Sets the start condition */
    if (ret !=0) { goto exit ;}
/*****
/* Sets the device address word (write).
/*****
ret = set_slavesel_seq ( CMD_WRITE_OPERATION , slave_addr ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Waits for an acknowledgement
/*****
ret = wait_ack() ;
    if (ret !=0) { goto exit ;}

/*****
/* Sets the memory address.
/*****
buf.d_int = rom_addr ;

ret = set_data_seq ( buf.d_byte[0] ) ; /* 1st Memory address */
    if (ret !=0) { goto exit ;}

ret = set_data_seq ( buf.d_byte[1] ) ; /* 2nd Memory address */
    if (ret !=0) { goto exit ;}

/*****
/* Issues the stop condition to bring SDA to high.
/*****
ret = set_end_proc ( ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Sets the start condition again.
/*****
ret = set_start_condition() ; /* Sets the start condition */
    if (ret !=0) { goto exit ;}

/*****
/* Sets the device address word (read).
/*****
ret = set_slavesel_seq ( DATA_READ_OPERATION , slave_addr ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Waits for an acknowledgement
/*****
ret = wait_ack() ;
    if (ret !=0) { goto exit ;}

/*****
/* Switches to the master receive mode.
/*****
ret = set_master_rcv_mode ( ) ;
    if (ret !=0) { goto exit ;}

/*****
/* Carries out a dummy read at the start of data reading.
/*****
start_read_seq ( ) ;

```



```

/*****
/* Reads data continuously. */
/*****
for (i=0; i< (rom_length-1) ; i++){
    ret = get_data_seq ( &buf.d_byte[0] ) ;
    if (ret !=0) { goto exit ;}

    *rom_data = buf.d_byte[0] ;
    *rom_data ++ ;
}

/*****
/* Issues the stop condition after the last data (1 byte) has been read */
/*****
ret = get_end_data_seq ( &buf.d_byte[0] ) ;
if (ret !=0) { goto exit ;}

*rom_data = buf.d_byte[0] ;

return (ret);

exit:
/*****
/* Issues a reset and the stop condition if an error occurs */
/*****
set_end_proc ( ) ;
return (ret);
}

```

```

/* ----- */
/* ----- */
/* 4. Sample Program 1-D TimerW Processing ----- */
/* ----- */
/* ----- */

/* ----- */
/* 4.1 Addition of reset vectors ----- */
/* ----- */
/* Set the jump destination to h8_timerw. */

/* ----- */
/* 4.2 TimerW common variable definition ----- */
/* ----- */
struct {
    int counter;           /* 100 ms counter */
    int wait_10ms;        /* Sets a wait time of 10 ms */
    int wait_100ms;       /* Sets the wait time in 100 ms units (common) */
    int wait_100ms_scan;  /* Sets the wait time in 100 ms units (for I2C) */
}com_timer;

/* ----- */
/* 4.3 TimerW initial settings ----- */
/* ----- */
/* ##### */
/* ##### */
/* Sets TimerW */
/* ##### */
/* ##### */
/* Sets TimerW initial settings */
/* ##### */
TW.TCRW.BIT.CKS = 3 ;           /* Counts using internal clock φ/8 */
TW.TCRW.BIT.CCLR = 1 ;         /* Clears the counter */
/* when a GRA compare match occurs. */
TW.TIOR0.BIT.IOA = 0 ;         /* GRA is used as an output compare register */
TW.TIERW.BIT.IMIEA = 1 ;       /* Enables IMFA */
TW.GRA = 20000 ;               /* Issues an interrupt every 10 ms */
/* ##(program note)##### */
/* ## The set values differ depending on the operating frequency of the microcomputer. ## */
/* ## Refer to the H8/3687 Hardware Manual. ## */
/* ##### */

TW.TCNT = 0 ;                  /* Clears the timer counter */

/* ##### */
/* Cancels interrupt disable */
/* ##### */
set_imask_ccr(0);              /* Enables interrupts */
/* ##### */
/* Starts TimerW */
/* Recovers from the sleep state and changes the frequency using the TimerW interrupt, */
/* without using direct feedback interrupts, by and starting the timer before executing "com_change_frq" */
/* ##### */
TW.TMRW.BIT.CTS = 1 ;         /* timer start

```

```

/* ----- */
/* 4.4 TimerW interrupt processing ----- */
/* ----- */
/*****/
/* 1. Module name: h8_timerw */
/* 2. Function overview: Interval timer processing every 10 ms */
/* 3. History of revisions: REV Date created/revised Created/revised by Revision contents */
/*          000          2002.02.11          Ueda          New          */
/*****/
#pragma interrupt( h8_timerw )
void h8_timerw( void )
{

    /*****/
    /* Clears the source */
    /*****/
    com_global.dummy = TW.TSRW.BYTE; /* dummy read */

    TW.TSRW.BIT.IMFA = 0; /* IMFA clear

    /*****/
    /* -1 in units of 10 ms
    */
    /*****/
    if( com_timer.wait_10ms>0 )
        com_timer.wait_10ms --;

    /*****/
    /* Increments the counter
    */
    /*****/
    com_timer.counter++;
    if( com_timer.counter >= 10 ){
        /*****/
        /* -1 in units of 100 ms
        */
        /*****/
        if( com_timer.wait_100ms>0 )
            com_timer.wait_100ms --;
        if( com_timer.wait_100ms_scan>0 )
            com_timer.wait_100ms_scan --;

        com_timer.counter = 0;
    }
}
}

```

#### 4. Reference Documents

- H8/3664 Group Hardware Manual (published by Renesas Technology Corp.)
- HN58X2464FPIAG Data Sheet (published by Renesas Technology Corp.)
- I<sup>2</sup>C Bus Usage (published by Phillips)

### Revision Record

| Rev. | Date      | Description |                      |
|------|-----------|-------------|----------------------|
|      |           | Page        | Summary              |
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|      |           |             |                      |
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