Introduction

This application note describes how to use the different boot configurations supported by the IDT 8T49N240, 8T49N241, and 8T49N242 devices. Whether fine-tuning during initial prototype builds, or deploying the 8T49N24x devices in full-scale production runs, the combination of boot configurations provide a flexible, reliable method of loading the right configuration settings.

Upon power-up or reset, the 8T49N24x devices can load the register settings from either One-Time-Programmable memory (fused at the factory) or from an external serial I2C EEPROM. The following table describes the register control bits in Register 0x00, which determine the boot configuration.

Table 1. Register 0x0000, OTP, and EEPROM Boot Settings

Scenario	Bit 1	Bit 0	Boot Sequence	Usage	Dash Code
	nBoot OTP	nBoot EEPROM			
1	1	1	Load only the first 8 registers of OTP	Predefine I2C address and configure the device using I2C.	-999
2	1	0	Load all registers from EEPROM	Configuration is still under development. Fine tune the system and test the new settings at power-up.	-998
3	0	1	Load all registers from OTP	Load a fixed configuration at power-up.	Custom
4	0	0	Load all registers from OTP and then EEPROM	Load a fixed configuration at power-up but maintain the option to load an alternate configuration at power-up.	Custom

The following sections provide more information about the behavior of the device for each of the boot configuration scenarios listed in the table.

Scenario 1: Load Only First 8 Registers of OTP

In this configuration, the 8T49N24x device will only load the first 8 bytes of One-Time Programmable (OTP). This register range contains the Device ID, Device Revision, Dash Code number, and the I2C base address. The I2C address can be pre-configured at the Factory, thus providing a flexible addressing scheme. The rest of the registers contain their default values and the device is configured in a low-power state, with all the outputs disabled. The device can be configured using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset.

Recommendation

If there is a need for a device in this state, we recommend the 8T49N24x-999 part. Samples are readily available and the part can be fully configured through I2C.

Scenario 2: Boot from External EEPROM

The ability to boot from an external EEPROM provides a flexible option when fine-tuning the 8T49N24x in a system. This allows for quick iterations of settings, each of which can be evaluated at power-up. Furthermore, it reduces development time by eliminating the need to have parts configured at the factory.

On power-up, or after reset, the 8T49N24x will function as an I2C master. It will perform an I2C read attempt to address the EEPROM at the address specified in the “EEP_ADDR” register, at location 0x01 bits 6:0. After the read completes, the device will function as an I2C slave.

EEPROM Read Fails

The first read attempt may not always succeed if other devices are concurrently arbitrating for control of the same I2C bus, if there is no EEPROM device present, or if the CRC value is incorrect (for more information on programming the EEPROM, see the application note titled *How to Program the EEPROM on IDT8T49N24X Evaluation Boards*). If the first read attempt is unsuccessful, the EEPROM will perform additional read attempts as specified by the counter “EEP_RTY”, in register 0x00 bits 7:3. For example, if EEP_RTY = 3, the EEPROM will perform four read attempts (the first read attempt plus three retries). If the EEPROM retries are unsuccessful, the registers can still be written to via the I2C interface.

EEPROM Read Success

After a successful read of the EEPROM contents, the device will be configured with the EEPROM settings. The lock sequence starts immediately after the EEPROM load. The I2C address of the 8T49N24x is determined by EEPROM register 0x06. This configuration can be overwritten using the serial interface once reset is complete. Any configuration settings written via the serial programming interface needs to be rewritten after any power cycle or reset.

Recommendation

If there is a need for a device in this state, IDT recommends the 8T49N24x-998 part. At power-up, it will attempt to read the configuration from an EEPROM at address 0xA0. Samples are readily available and the part can be fully configured through I2C. If a different EEPROM address or two-byte addressing is needed, then please contact IDT for a custom dash code.

Scenario 3: Boot from OTP

The IDT8T49N24x devices support an internal OTP memory that can be pre-programmed at the factory with one complete device configuration. This configuration can be overwritten using the serial interface once reset is complete. Any configuration written via the serial programming interface must be rewritten after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is required.

Recommendation

IDT provides full support in configuring, measuring, and optimizing custom configurations. However, due to the fluctuating nature of system requirements before specifications and requirements are finalized, there are many times when the configuration needs to be modified. IDT recommends that this option be used once the device performance has been evaluated by the customer and the configuration is “frozen”, i.e. no more changes are expected. Please contact IDT for support with custom OTP configurations.

Scenario 4: Boot from OTP and EEPROM

This option offers the ability to boot from either EEPROM or OTP. At power-up, if the EEPROM read is unsuccessful, the device will default to the OTP settings. This option allows customers to use a single device (and part number) to evaluate it under varying scenarios.

Setup

With both the EEPROM and OTP boots selected, the EEPROM configuration will take precedence over the OTP configuration. Thus, to boot from the EEPROM, the EEPROM must be present, powered on, its address must match the EEP_ADDR field programmed in OTP, and it must have the correct CRC value appended to the end of the register values.

To boot from OTP, a number of options are available. First, if an EEPROM with address selection pins is used, a switch or jumper can be used to change the EEPROM address so that it does not match the EEP_ADDR register set in OTP. Alternatively, the connection to either VDD, SDA, or SCK can be removed or switched off to prevent the EEPROM from loading. Lastly, the CRC value can be changed to an incorrect value so that the read fails and prevents loading the register values.

Conclusion

Changes in system requirements and fine-tuning a system both require iterations of a configuration before it is finalized. By using the flexible boot options of the 8T49N24x devices, immediate results can be obtained, thus reducing development time.

For more information on OTP and EEPROM load times, please see the relevant datasheet. For support on a customer configuration, please submit an IDT technical support request.

Revision History

Revision Date	Description of Change
June 5, 2017	▪ Added support for the 8T49N240i device ▪ Converted the document to the latest template
August 6, 2015	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.