Introduction

This application note provides details on how to program the frequency for the IDT 8T49N24X devices.

Overview

Programming the frequency inputs and outputs for the 8T49N24x devices involves three main steps:

1. Calculate the possible output dividers and choose the highest value. This establishes the VCO frequency.

2. Based on the ratio between the VCO frequency and Crystal/XO frequency, calculate the upper loop feedback divider settings.

3. If the device is operating in jitter attenuator mode, calculate the reference clock lower loop feedback divider settings.

4. Optionally, use the register settings to calculate the actual output frequency. Compare that result to the target frequency.

Jitter Attenuator vs Synthesizer Mode

– **Synthesizer mode** generates output frequencies directly from the crystal or XO input. Any error in the frequency will be passed on to the outputs, so a 10ppm crystal error would result in a 10ppm output frequency error.

– **Jitter attenuator mode** uses an input reference frequency to correct any error in the crystal/XO frequency by adjusting the VCO frequency. The output frequencies, derived from the VCO frequency, then have the same error as the input reference.

When the device is used in jitter attenuator mode, steps 1 through 3 are all necessary. When the device is used in synthesizer mode, only steps 1 and 2 apply. Step 4 is only used to calculate the expected output error for reference.

The 8T49N241 and 8T49N242 devices both have an integer output divider for Q0. However, the 8T49N241 has fractional output dividers for outputs Q1-Q3, whereas the 8T49N242 has all integer dividers for outputs Q0-Q3. For the working example that follows, an 8T49N241 device will be used, with the following configuration:

Clock Input/Output	Frequency (MHz)
Crystal Input	38.88
Reference Clock Input	25
Q0 Output	125
Q1 Output	156.25

1: Calculate the Output Dividers

The first step in creating the desired outputs is to solve for the VCO frequency, and calculate the output dividers. Both types of output dividers create an output frequency based on the VCO output frequency, and divide it down by either an integer or fractional number. The divider output frequency is given as:

$$F_{out} = F_{VCO}/N$$

where N is either an integer or fractional number.

Integer Divider Calculation:

The integer dividers create an output frequency that is an integer fraction of the VCO output frequency. There are two stages to the integer output dividers, such that in the above equation:

$$N = NS1 * NS2$$

where

$$NS1 = \div 5, \div 6, or \div 4$$

(Note: The actual NS1 register contains 0,1,or 2 for the values shown above)

and

$$NS2 = \div 1, or \div (2 * n) \ with \ n = 1 \ to \ 2^{16}$$

(Note: The actual NS2 register contains 0 for ÷1 or the n value above)

The valid VCO range is 3000–4000MHz, meaning that divider values that would require a VCO frequency outside of this range in order to produce the desired output, would be invalid. In order to obtain the range of valid output dividers, the VCO max and min frequencies are divided by the output frequency. Thus, for the integer output Q0, the range is between:

$$N = floor(VCO_{max}/F_{out}) = floor(4000/125) = 32$$
$$N = ceil(VCO_{min}/F_{out}) = ceil(3000/125_{min}) = 24$$

This gives us the overall divider value ranges. However, since there are two stages, the individual stages must then be found. Since the first stage can only take values of 4, 5, and 6, and the second stage can only take on values of 1 or a multiple of 2, many numbers in the range found above may not be possible. The following combinations of NS1 and NS2 fall into the above range, and are listed along with the resulting VCO frequencies:

NS1	NS2	N	VCO Freq (MHz)
6	4	24	3000
4	6	24	3000
5	6	30	3750
4	8	32	4000

For this example, we'll pick the 4000MHz VCO solution. If more integer dividers were being used (i.e. in the '242 device), the solutions for the other integer dividers must be found and a common VCO frequency must exist. If no solution works for all the integer dividers, the '241 may be necessary to produce all output frequencies.

Fractional Divider Calculation:

The fractional dividers create an output frequency that can be any fraction of the VCO frequency from 6.0 and 524287.99..., and can be produced with a resolution of at least 1.24 parts per billion or better (depending on the integer value used). Since the divider can produce almost any desired output frequency, the integer dividers should be first used to find the list of VCO frequencies that can be used to produce all the desired output frequencies. However, performance is normally best on a fractional divider when it takes on an integer value, or has a fraction of 0.5.

The divider ratio is composed of an integer and a fractional component, so the divider value N is:

$$N = 2 * \left(N_{INT} + \frac{N_{FRAC}}{2^{28}}\right)$$

where $N_{INT} >= 3$ to 262144, and $N_{FRAC} = 0$ to $2^{28}-1$.

To find the N_{INT} and N_{FRAC} values, we first solve for N_{INT}:

$$N_{INT} = floor\left(F_{VCO}/(2 * F_{out})\right)$$

The fractional part can then be found:

$$N_{FRAC} = round(\{F_{VCO}/(2 * F_{out}) - N_{INT}\} * 2^{28})$$

For the example above, there is one fractional divider output on Q1 of 156.25MHz. The divider values are:

$$N_{INT} = floor\left(\frac{4000}{(2 * 156.25)}\right) = floor(12.8) = 12$$

$$N_{FRAC} = round(\{4000/(2 * 156.25) - 12\} * 2^{28}) = round(214748364.8) = 214748365$$

In this example, picking the 3750MHz VCO frequency would have allowed for a fractional divider value of 30, which would be expected to have better phase noise performance.

2: Calculate the PLL Feedback Dividers

After the VCO frequency has been picked and the output divider values have been found, the PLL feedback divider values may be calculated. The PLL feedback dividers take the input frequency and effectively multiply it by the divider value to produce a higher output frequency on the VCO. The 8T49N241 and 8T49N242 have identical functionality for this process. The first step is to find the PLL input frequency. This is given by the crystal or crystal oscillator input frequency, which is typically multiplied by 2 by the on-chip doubler (recommended as long as the resulting frequency is <=125MHz). For this example, the input is a 38.88MHz crystal, so with the doubler enabled the PLL input is:

$$F_{IN} = 2 * 38.88MHz = 77.76MHz$$

The VCO output frequency is given by:

$$F_{VCO} = F_{IN} * N$$

where N is a fractional divider that operates similarly to the fractional output divider, and can be any fraction between 24.0 to 512.99... with a resolution of 19.9 parts per billion or better (depending on the integer value used):

$$N = DSM_{INT} + \frac{DSM_{FRAC}}{2^{21}}$$

where DSMINT >= 24 to 512, and DSMFRAC = 0 to 221-1

The integer and fractional portions are solved in a similar manner to the fractional output dividers:

$$DSM_{INT} = floor(F_{VCO}/F_{IN})$$

$$DSM_{FRAC} = round(\{F_{VCO}/F_{IN} - DSM_{INT}\} * 2^{21})$$

For the example above, $F_{IN} = 77.76$ and $F_{VCO} = 4000MHz$, so:

$$DSM_{INT} = floor(4000/77.76) = floor(51.440329218107) = 51$$

$$DSM_{FRAC} = round(\{4000/77.76 - 51\} * 2^{21}) = round(923437.300411531) = 923437$$

3: Calculate the PLL Lower Loop (Reference Input) Dividers

This step is only required if the device is operating in Jitter Attenuator mode, and corrects the VCO output frequency by using one of the reference clock inputs. The lower loop effectively adjusts the PLL feedback divider value to compensate for the error in the input frequency, which is calculated using the reference clock as a basis. The VCO and the reference clock both contain integer dividers that divide the clocks down to a lower frequency. The divider values for each should be picked such that the nominal divider outputs for both are the exactly the same. And deviation from the nominal value on the input frequency (e.g. a crystal or crystal oscillator error) will therefore be corrected by the reference clock input, which is assumed to be much more accurate.

The output dividers' frequency is called the phase frequency detector frequency, and is given by:

$$F_{PFD} = F_{REF}/PRE = F_{VCO}/M1, \text{ with } F_{PFD} >= 8kHz \text{ to } 8MHz$$

where F_{REF} is the reference input frequency, PRE is the reference input integer divider value, and M1 is the VCO integer divider. The range should be within 8kHz to 8MHz. A value of around 128kHz is typically used. For close-in noise performance below 1kHz offset, values below 100kHz should be avoided.

For the example, F_{REF} = 25MHz and F_{VCO} = 4000MHz. A common frequency would be:

F_{PFD} = 0.127551020408163MH, obtained with $PRE=196$ and $M1=31360$

The 8T49N241 and 8T49N242 devices contain two separate reference clock inputs, which provide a backup reference clock in case the primary clock is lost. Each reference clock has its own PRE and $M1$ dividers, so the above process needs to be repeated for each reference clock that is used.

4: Calculate the Output Frequency Error

The error in the output frequency can come from one of two sources, the first of which depends on whether the device is operating in Jitter Attenuator or Synthesizer mode.

Synthesizer Mode:

In Synthesizer mode, the VCO error comes from the input clock error, combined with any PLL rounding error. In the above example, if the reference input was not used and the 38.88MHz crystal input had a relative error of -1 parts per million, the VCO error would be:

$$F_{VCO} = F_{IN} * relative_{error} * Doubler * \left(DSM_{INT} + \frac{DSM_{FRAC}}{2^{21}} \right)$$

$$= 38.88MHz * (1 - 1^{-6}) * 2 * \left(51 + \frac{923437)}{2^{21}} \right) = 3999.9599888612MHz$$

This is a relative error of -1.003 parts per million.

Jitter Attenuator Mode:

In Jitter Attenuator mode, the VCO error is typically dominated by the reference input clock error, but a slight frequency mismatch or rounding error can also contribute to a small deviation in the desired VCO output frequency. The VCO output error is equal to the relative error in the F_{PFD} frequencies. In the above example, if the relative error in the 25MHz reference input is +5 parts per billion, the resulting frequency is:

$$F_{REF}/PRE = (25MHz * relative\_error)/196 = 25MHz * (1 + 5E^{-9}) = 25.000000125MHz$$

The VCO output will therefore be adjusted to:

$$F_{VCO} = 5.000000125MHz * \frac{31360}{196} = 4000.00002MHz$$

This is a relative error of 5 parts per billion, the same as the reference input clock error.

Output Divider:

The last source of error, common to both modes, is a rounding error in the output dividers. Using the Jitter Attenuator error calculated above, the output frequencies after the output dividers are:

$$Q0 = F_{VCO}/(NS1 * NS2) = 4000.00002MHz/(4 * 8) = 125.000000625MHz$$

(Relative error = 5 parts per billion)

$$Q1 = F_{VCO}/(2 * (N_{INT} + N_{FRAC}/2^{28})) = 4000.00002MHz/(2 * (12 + 214748365/2^{28}))$$
$$= 156.250000772155MHz$$

(Relative error = 4.94 parts per billion)

In some Synthesizer mode cases, a smaller error may be required, and may be obtained if knowledge of the crystal / crystal oscillator error is available (i.e. through temperature characterization, etc). In these cases, the PLL may be placed in Manual Override mode, so that the feedback dividers may be manually adjusted via the I2C interface to compensate for the input error. Fine-tuning of the PLL is also available if errors below the PLL feedback divider's granularity are required. These cases are covered in the document titled "8T49N24x Frequency Tuning".

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