Width Expansion Of SyncFIFOs™ (Clocked FIFOS)

by Rob De Voto

INTRODUCTION

The performance requirements of today's systems are continually reaching to new heights. In response to needs for higher performance, IDT has introduced a family of First-In-First-Out (FIFO) buffers which are ideally suited for system speeds of 25MHz or greater. The synchronous interface of this family of Clocked FIFOs offers several advantages over the traditional IDT720X Series of FIFOs:

a) speed (data transfer rates of up to 67MHz;

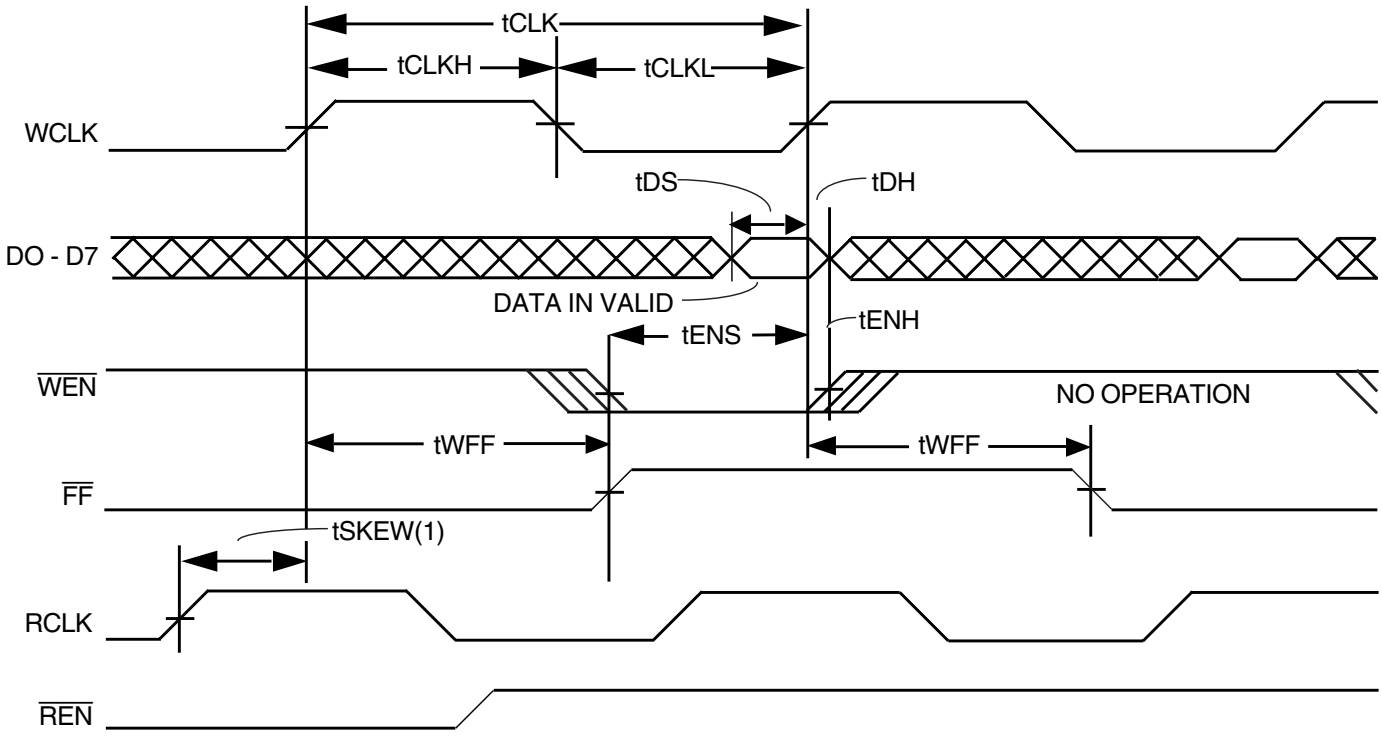
b) free running clock control simplifies system design.

The Clocked FIFO family includes x8-bit, x9-bit, and x18-bit parts in a wide range of densities. To accommodate system requirements beyond this product family, the FIFOs can be easily expanded in width and depth. The purpose of this Application Note is to discuss design considerations and recommendations when designing with SyncFIFOs (Clocked FIFOs) in Width Expansion.

SKEW TIMING

The inherent advantage of FIFO buffers is the ability to buffer data between two mismatched systems or subsys-tems. Inherent to an interface between two asynchronous systems is the issue of synchronizing events on one side with respect to events on the other.

For the Clocked FIFOs, internal logic is used to synchronize the status flags to either the Write Clock (WCLK) or the Read Clock (RCLK). A skew time is specified which deter-mines if sufficient time has been allowed for the flag to be updated in the current clock cycle. If the skew timing is not met, an extra cycle is required to update the flag.



NOTES:

1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge for FF to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then FF may not change state until the next WCLK edge.

Figure 1. Skew Timing

WIDTH EXPANSION

When using the Clocked FIFOs in Width Expansion, the control signals of all parallel FIFOs should be connected together to maintain concurrent operations on all devices. The recommended flag output circuitry is shown in the following section.

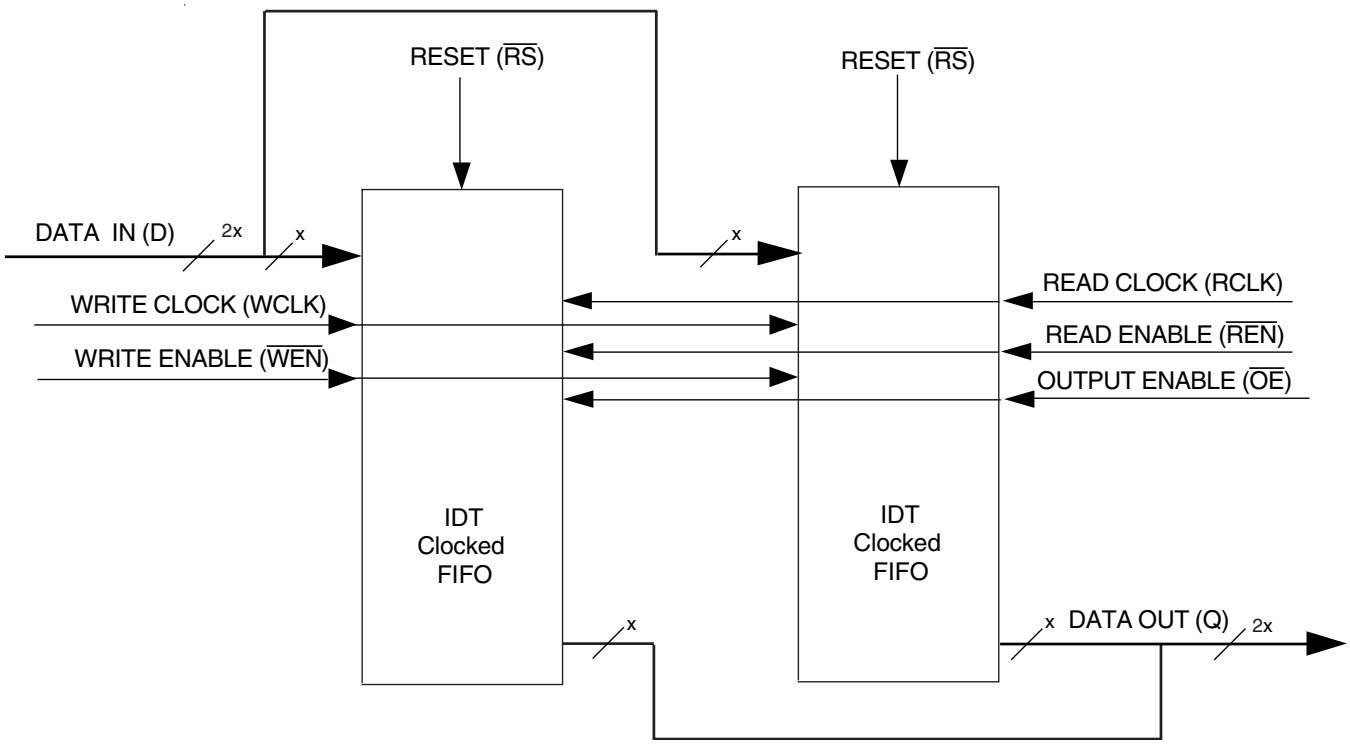


Figure 2. Block Diagram Showing the Control Signals of a SyncFIFO (Clocked FIFO) in a Width Expansion Configuration

DESIGN CONSIDERATIONS

Inherent to all Clocked FIFOs is the concept of skew timing. In reality, the skew timing of individual devices may vary by a small amount. For xample, the tSKEW1 minimum spec for the 20 ns speed grade of the IDT72211 (512 x 9-Bit) equals 8ns. For two devices in width expansion, the actual tSKEW1 of FIFO#1 may equal 7.2ns and the actual tSKEW1 of FIFO#2 may equal 7.4ns.

This small variation in the actual timing of the devices may cause the flags of the parallel devices to be de-asserted in different cycles. For example, if the tSKEW1 timing of the system happens to be 7.3ns on the edge which is de-asserting the $\overline{EF}$, then the $\overline{EF}$ of the two FIFOs will be de-asserted on different clock cycles.

In this situation, if $\overline{REN}$ is asserted to begin read operations when the EF of FIFO#1 is de-asserted but the $\overline{EF}$ of FIFO#2 is not de-asserted, then data on the outputs (Q) of the two devices will not be aligned. In other words, data from FIFO#2 will have a one location lag behind data from FIFO#1.

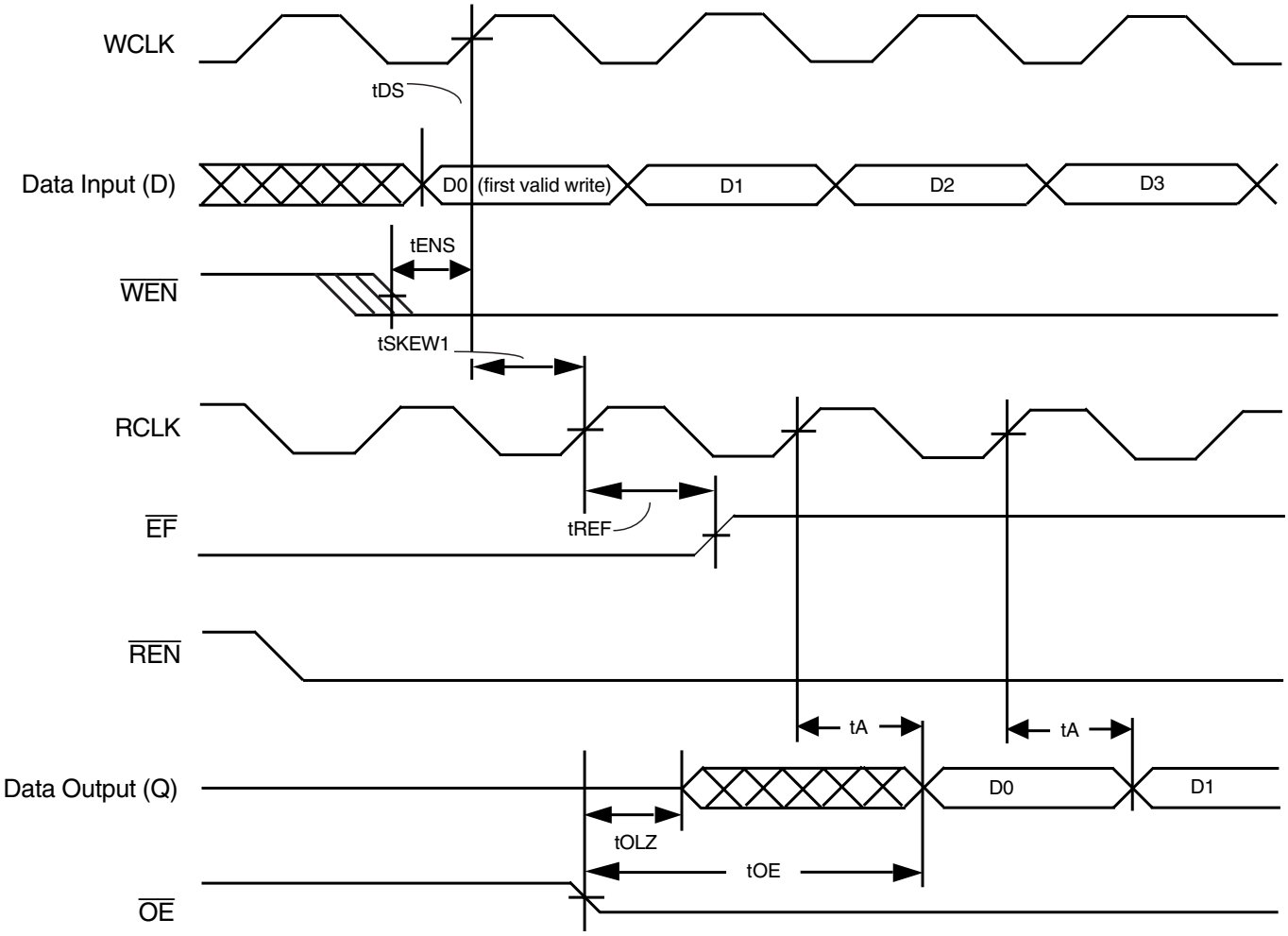


Figure 3. Skew Timing for FIFO#1

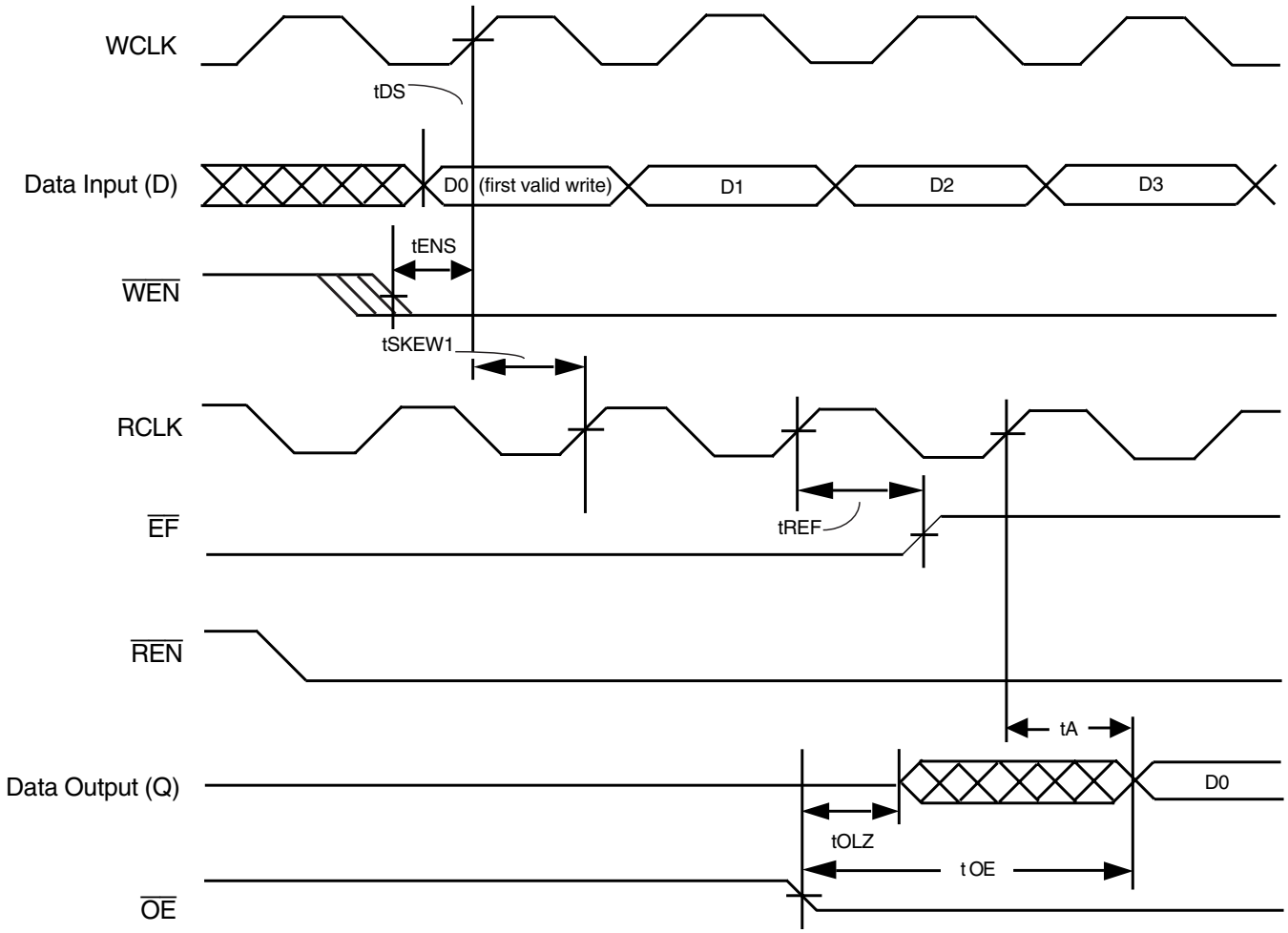


Figure 4. Skew Timing for FIFO#2

SOLUTION AND RECOMMENDATION

There are two solutions to the situation described.

1. Composite Flag. Monitor the $\overline{EF}$ from all FIFOs in Width Expansion. A read operation ($\overline{REN}$ = low) can begin only when the $\overline{EF}$ from all devices have been de-asserted. This is the recommended solution.

2. Use the Almost Empty Flag ($\overline{AE}$) to begin read opera-tions. De-assertion of $\overline{AE}$ may exhibit the same skew affect as the $\overline{EF}$ (see next section), however, using $\overline{AE}$ does not jeopardize data integrity.

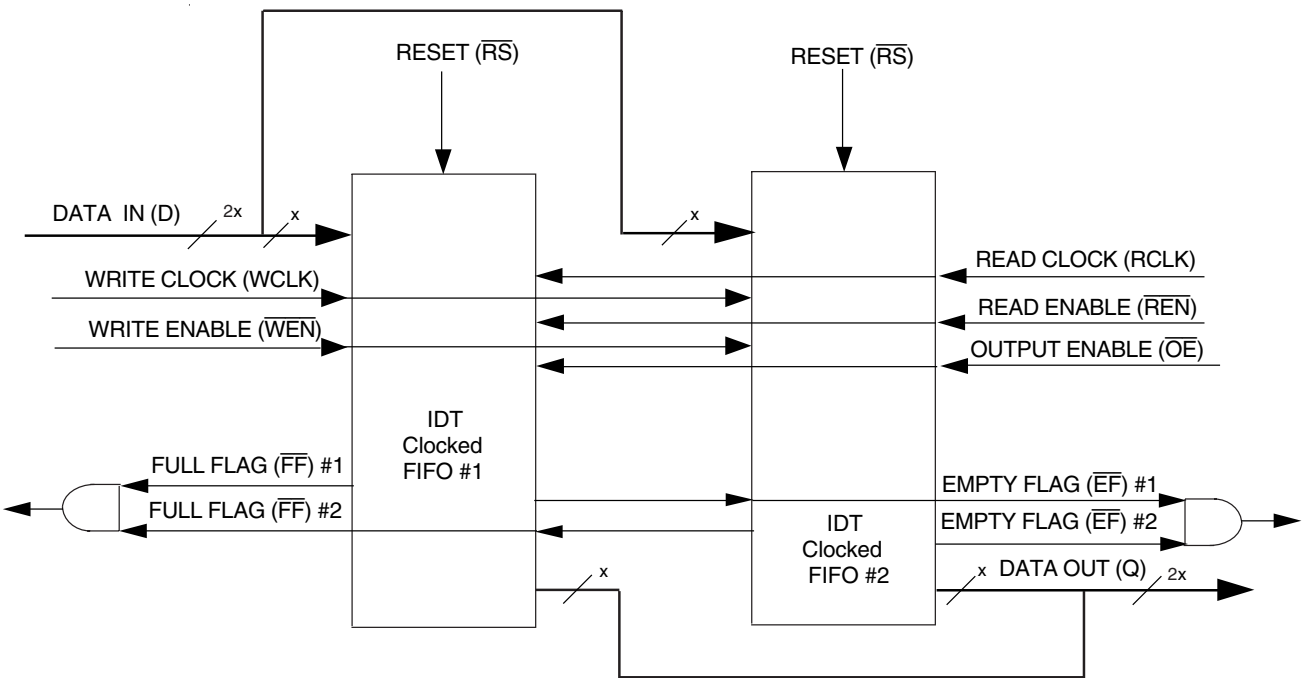


Figure 5. Recommended Block Diagram of Width Expansion using Composite Flags

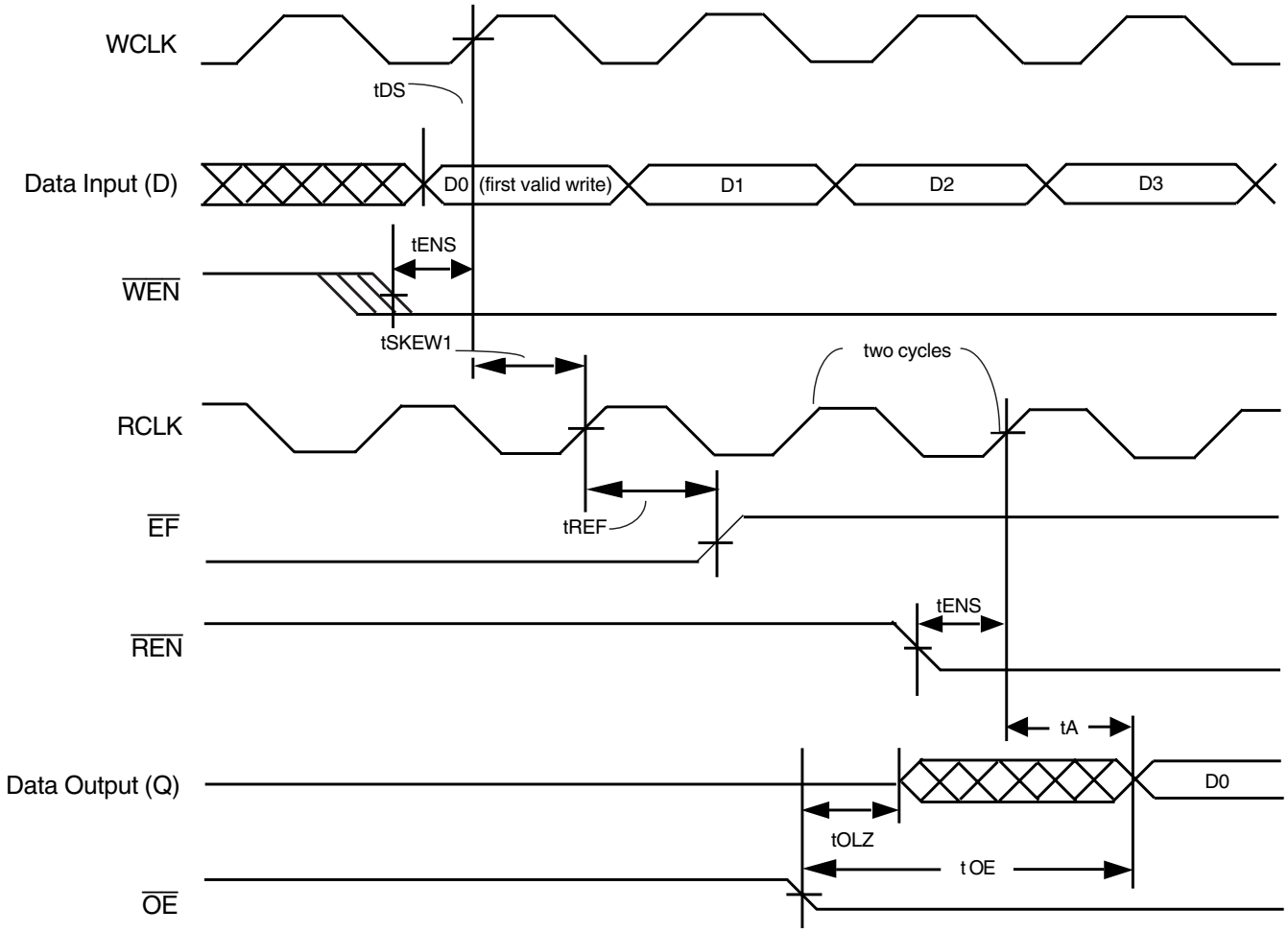


Figure 6. Waiting Two Clock Cycles after Flag Assertion

OTHER FLAGS

This skew affect also applies to the Full Flags ($\overline{FF}$) of all the Clocked FIFOs (x8, x9 and x18 SyncFIFOs), the Almost-Empty Flag ($\overline{AE}$) and Almost-Full Flag (AF) for the IDT72XX0 family (x8 SyncFIFOs), and the Programmable Almost-Empty Flag ($\overline{PAE}$) and Programmable Almost-Full Flag ($\overline{PAF}$) for the IDT72XX1 family (x9 SyncFIFOs). The solution for these flags is identical to those outlined above. In summary, use composite flag, i.e. monitor the flags from all devices.

EXCEPTION

The exception to the skew affect is the Programmable Almost-Empty Flag ($\overline{PAE}$), the Programmable Almost-Full Flag ($\overline{PAF}$), and the Half-Full Flag ($\overline{HF}$) on the IDT722X5 family (x18 SyncFIFOs). These flags are not synchronized with respect to any one clock. In other words, they are asserted and de-asserted with respect to different clocks. In this case, there is no skew timing (tSKEW1). The monitoring of only one device in Width Expansion is adequate for these flags.

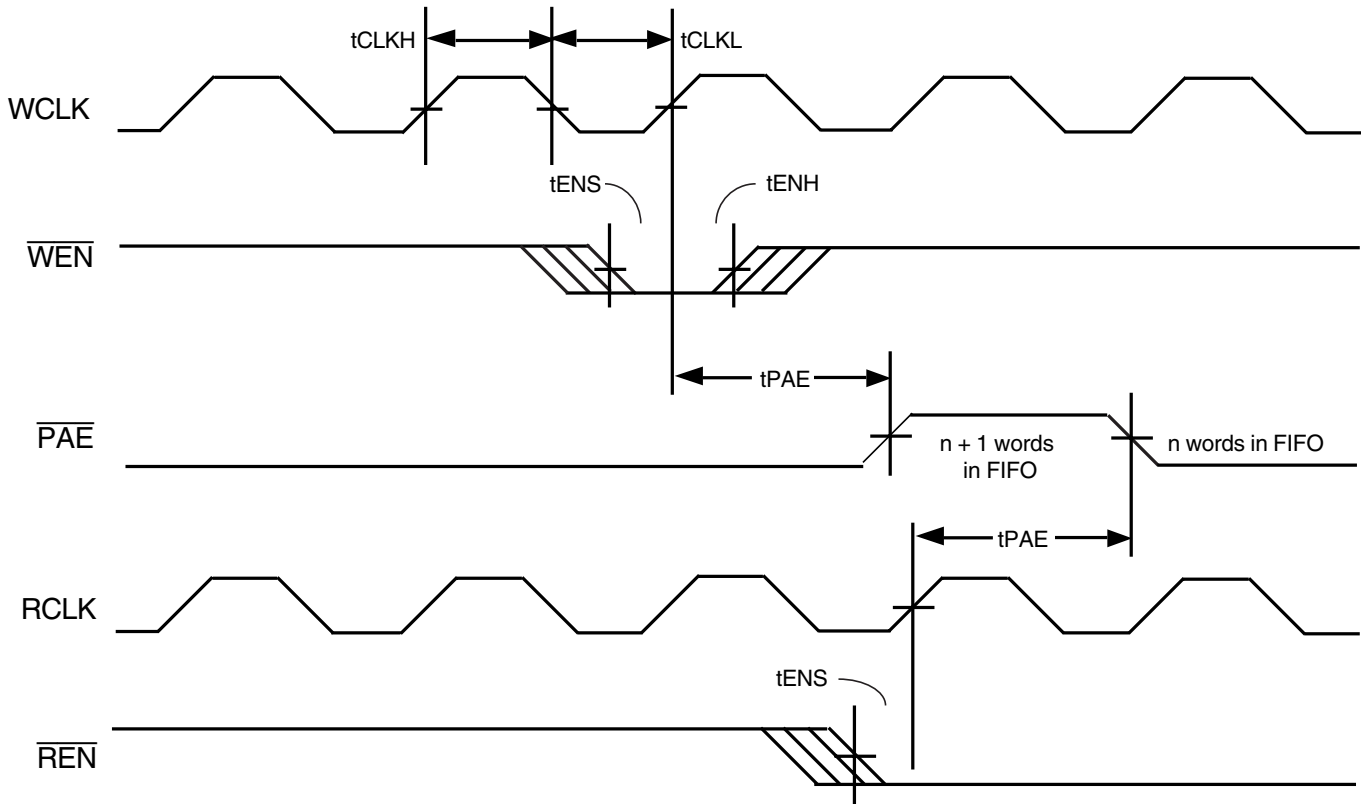


Figure 7. Programmable Flag Timing for the IDT722X5 Family (x18 SyncFIFOs)

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