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April 1st, 2010
Renesas Electronics Corporation

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4283 Group

Staircase Key Matrix (Using 3-Point Switches)

1. Summary

This document describes how to set the staircase key matrix (using 3-point switches) for the 4283-group microcomputers and shows its application example.

2. Introduction

The application example presented here applies for use with the microcomputers listed below under the conditions given.

- Microcomputer : 4283 group
- Oscillation frequency : 4.0 MHz

Please note that the sample program for the 4283 group may somewhere in it manipulate the bits of unused functions for reasons of bit arrangement in the control registers. The values of these bits in a user system should be set to suit the usage condition of the system.

3. Related Registers

3.1 Timer Control Register V1

Table 3.1 shows bit assignments of the Timer Control Register V1.

To write to the Register V1, set a value in Register A and then execute a TV1A instruction.

Table 3.1 Bit Assignments of the Timer Control Register V1

Timer control register V1		at reset : 000_2	at RAM back-up : 000_2	W TV1A
$V1_2$	Carrier wave output auto-control bit	0	Auto-control output by timer 1 is invalid	
		1	Auto-control output by timer 1 is valid	
$V1_1$	Timer 1 count source selection bit	0	Carrier wave output (CARRY)	
		1	Bit 5 of watchdog timer (WDT)	
$V1_0$	Timer 1 control bit	0	Stop (Timer 1 state retained)	
		1	Operating	

Note 1: The letter “W” denotes “writable.”

3.2 Pulldown Control Register PU0

Table 3.2 shows bit assignments of the Pulldown Control Register PU0.

To write to the Register PU0, set a value in Register A and then execute a TPU0A instruction.

Table 3.2 Bit Assignments of the Pulldown Control Register PU0

Pull-down control register PU0		at reset : 0000_2	at RAM back-up : state retained	W TPU0A
$PU0_3$	Ports G_2, G_3 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU0_2$	Ports G_0, G_1 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU0_1$	Port E_1 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU0_0$	Port E_0 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	

Note 1: The letter “W” denotes “writable.”

3.3 Pulldown Control Register PU1

Table 3.3 shows bit assignments of the Pulldown Control Register PU1.

To write to the Register PU1, set a value in Register A and then execute a TPU1A instruction.

Table 3.3 Bit Assignments of the Pulldown Control Register PU1

Pull-down control register PU1		at reset : 0000_2	at RAM back-up : state retained	W TPU1A
$PU1_3$	Port D_7 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU1_2$	Port D_6 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU1_1$	Port D_5 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	
$PU1_0$	Port D_4 pull-down transistor control bit	0	Pull-down transistor OFF, key-on wakeup invalid	
		1	Pull-down transistor ON, key-on wakeup valid	

Note 1: The letter “W” denotes “writable.”

4. Application Example for the Staircase Key Matrix

The staircase key matrix refers to the one where a key is located at all combinatorial positions of two shorted port pins in a key matrix configuration.

Point : Up to 55 switches can be located at 11 input ports.
For a conventional key matrix using the same number of pins (consisting of 6 output ports x 5 input ports), a total number of keys is 30.
Therefore, the staircase key matrix permits a greater number of keys to be arranged than in a conventional key matrix.
However, if two or more keys are pressed at the same time, the matrix cannot determine which key has been depressed.

Specification : The matrix is reawaken by pressing a key (key-on wakeup), and key numbers (1–55) are stored in RAM according to the depressed keys.
Furthermore, when multiple keys are pressed at the same time, key number 255 is assumed; when no keys are entered, key number 0 is assumed; when input on only 1 port can be recognized, key number 254 is assumed.
When the matrix confirms that no keys have been entered, it goes to RAM backup mode.
Keys are scanned in a cycle of 10.24 ms.
If the scan result matches twice in succession, a key is confirmed to have been pressed and a key input confirmed flag is set.
If the scan result does not match, no keys are confirmed to have been pressed and a key input confirmed flag is cleared.

Figure 4.3 shows an example of staircase key matrix settings (1). Figure 4.4 shows an example of staircase key matrix settings (2).

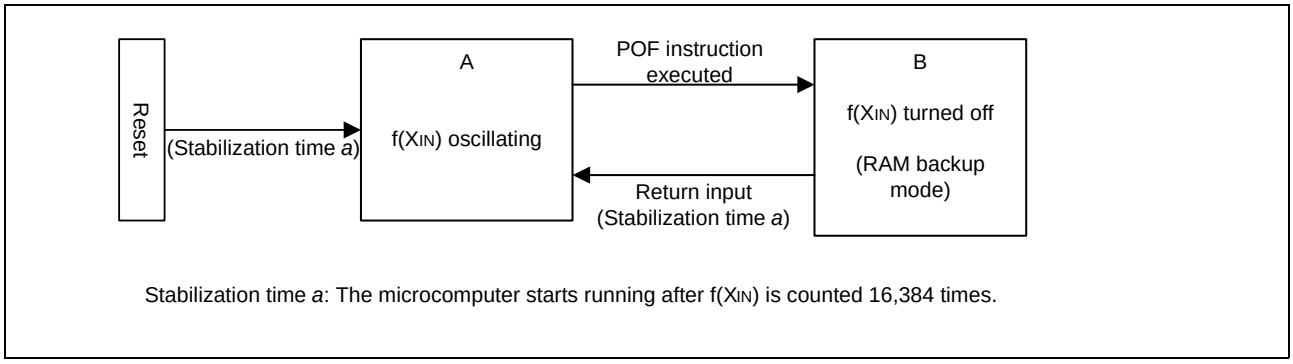
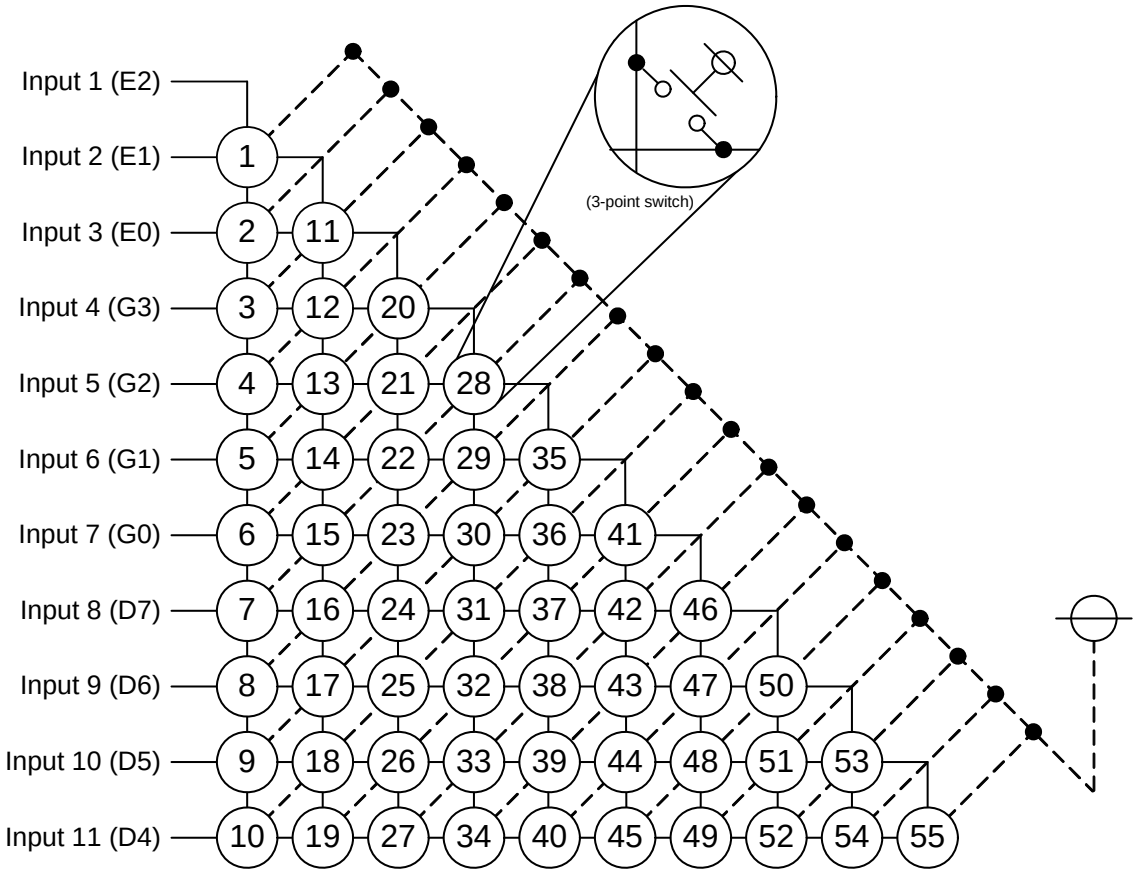


Figure 4.1 State Transition Diagram



<Key number assignments>

Number of high level input ports	Key number	Supplement
0	0	No key input
1	254	Input error
2	1～55	Single key input
3 or more	255	Multiple keys pressed

<Multiple key depressions>
If two or more keys are pressed at the same time, the matrix cannot determine which key is pressed.

<Return conditions from RAM backup mode>
Turn on the pulldown transistor on each input port and enable the key-on wakeup function before entering RAM backup mode.
Then, when any key is pressed and a high level signal is applied to the input port, the matrix returns from RAM backup mode.

Figure 4.2 Key Matrix Arrangement

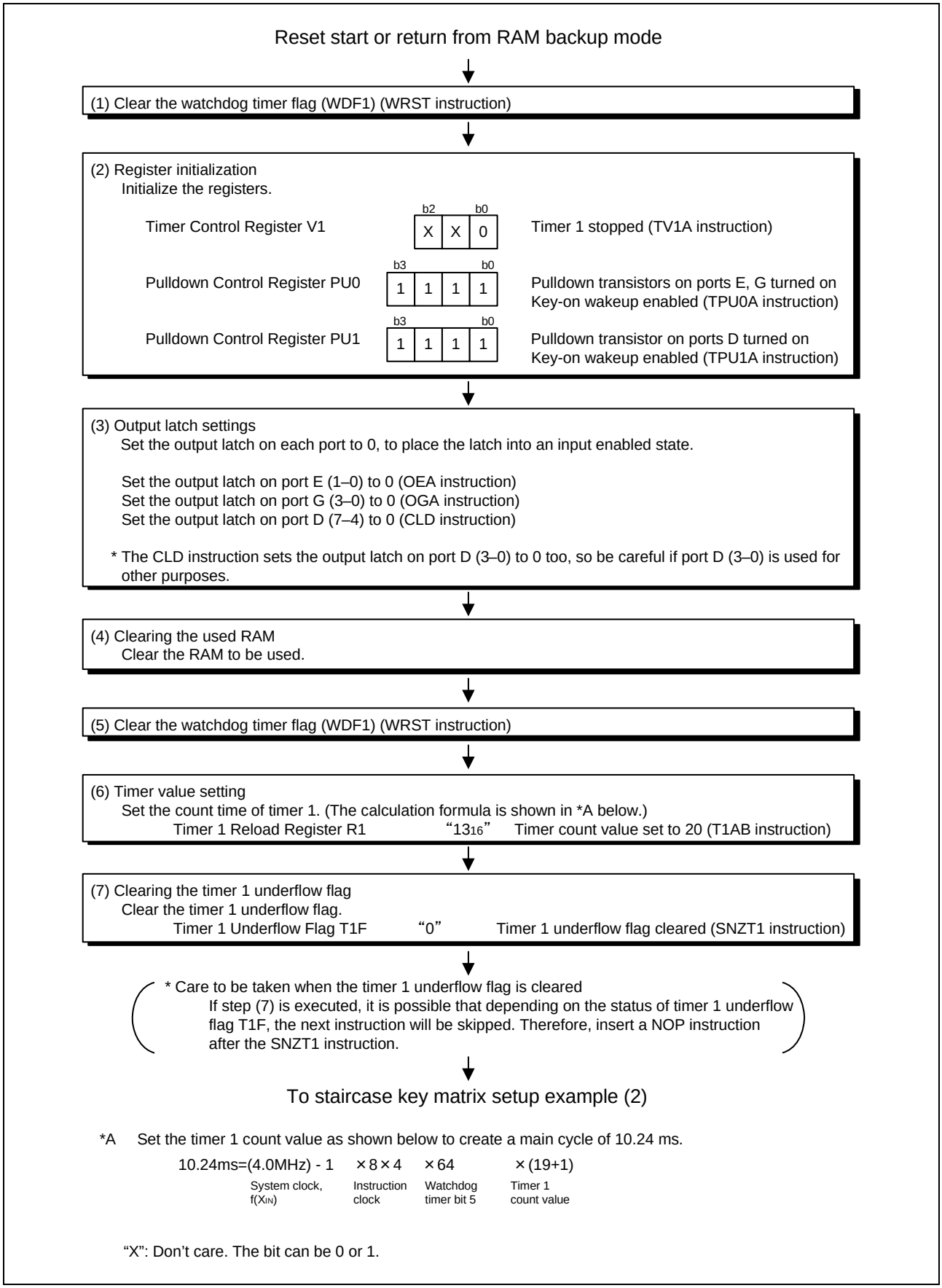


Figure 4.3 Staircase Key Matrix Setup Example (1)

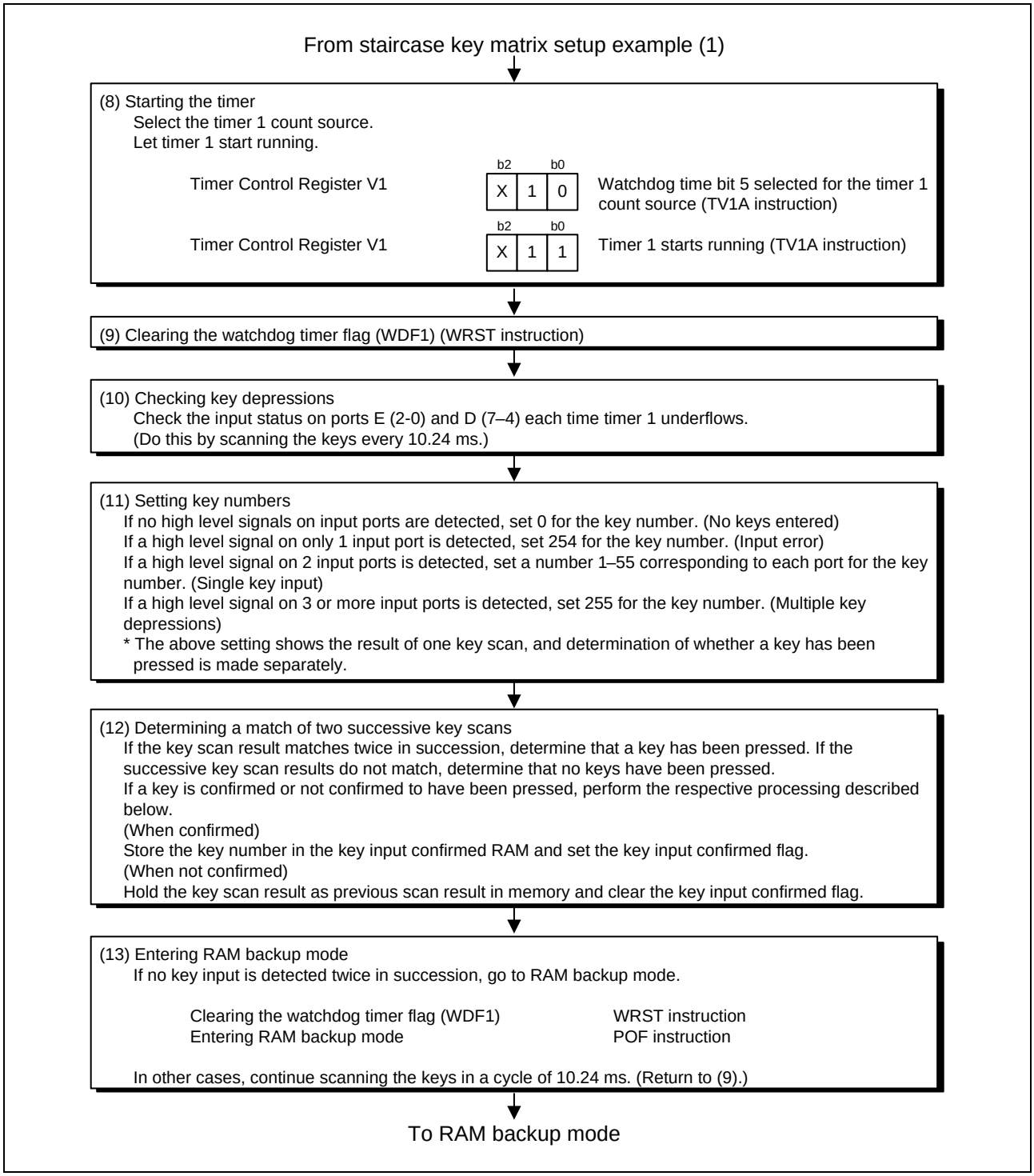


Figure 4.4 Staircase Key Matrix Setup Example (2)

5. Reference Sample Programs

Download reference sample programs from the Renesas Technology website.
Click the screen menu “Application Note” on the left side of the 4283 group web page.

6. Reference Documents

Data sheet
4283 Group Data Sheet

The latest version is available from the Renesas Technology website.

7. Renesas Website and Where to Contact

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Revision history	4283 Group Staircase Key Matrix (Using 3-Point Switches) Application Note

Rev.	Issue date	Content of revision	
		Page	Points
1.00	2007.12.28	—	First edition issued

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