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Renesas Electronics Corporation

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APPLICATION NOTE

14-Bit PWM Function Based Variable Duty-Cycle Pulse Output

Introduction

As shown in figure 1.1, a pulse with a variable duty cycle controlled by a 14-bit PWM function is output from the PWM output pin.

Target Device

H8/300H Tiny Series H8/3687

Contents

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1. Specification

1. As shown in figure 1.1, a pulse with a variable duty cycle controlled by a 14-bit PWM function is output from the PWM output pin.
2. In this task example, the pulse that is output has a 75.4% duty cycle with a period of 102.4 µs and high-level pulse width of 77.2 µs.

$$\text{Duty cycle} = \frac{\text{High-level pulse width}}{\text{Period pulse}} \times 100\ (\%)$$

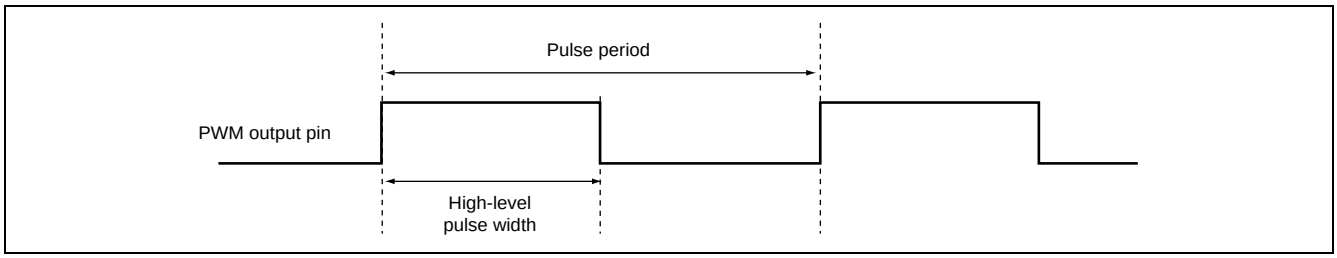

Figure 1.1 Variable Duty-Cycle Pulse Output using 14-Bit PWM Function

2. Description of Functions Used

1. In this task example, a pulse with variable duty cycle controlled by the 14-bit PWM function is output from the PWM output pin.
   A. Figure 2 shows the block diagram of the 14-bit PWM function which is described as follows:
      — The system clock (ϕ) is a 5 MHz clock that is derived from the 10-MHz OSC clock divided by 2, and is used as the reference clock to drive the CPU and peripheral functions.
      — PWM Control Register (PWCR) is an 8-bit write-only register used to select the input clock. Selection of the input clock can be made using one of two conversion periods: One conversion period of 32.768/ϕ with a minimum variation width of 2/ϕ, or one conversion period of 16.384/ϕ with a minimum variation width of 1/ϕ.
      — Applying pulse-frequency division lowers the levels of timing jitter and inaccuracy.
      — PWM Data Register U and L (PWDRU and PWDRL) is a 14-bit write-only register. The six high-order bits of this register constitute PWDRU, and the eight low-order bits are used for PWDRL. The values written in PWDRU and PWDRL correspond to the total time that the pulses in the PWM waveform are high-level over one conversion period. When 14-bit data is written to the PWDRU and PWDRL fields of the PWM data register, the contents of PWDRU and PWDRL are fetched by the PWM waveform generation unit, and subsequently update the data for PWM waveform generation. Further, the sequence for setting the 14-bit data must be performed by first writing the eight low-order bits of the data to PWDRU, and then writing the six high-order bits to PWDRL.
      — Port Mode Register 1 (PMR1) is an 8-bit readable/writable register that controls the functions of the individual pins of port 1. The P14/PWM pin is set to the PWM output pin function by means of P11/PWM pin function switch (PWM) of the bit 4 of PMR1.
      — A PWM waveform derived by the method of pulse width modulation is output from the PWM output pin (PWM).

Note: When the PWM waveform is output using the 14-bit PWM function applicable to this task example, there may be occasions when a normal PWM waveform will fail to be output due to the timing needed to overwrite the PWM data register. In this task example, by using the Timer B1 auto-reload function, Timer B1 interrupt will be generated every 160 µs.

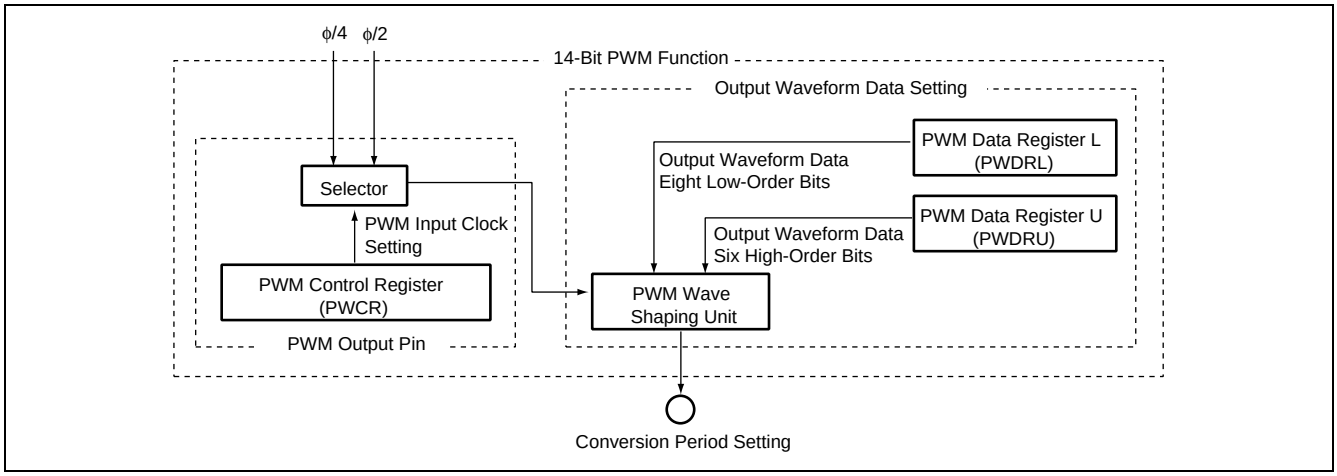

Figure 2.1 Bit PWM Function Block Diagram

2. Table 2.1 lists the function allocation applicable to this task. The allocated functions indicated in table 1 are used to implement output of a variable duty-cycle pulse using the 14-bit PWM function.

Table 2.1 Function Allocation

Function	Function Allocation
PWCR	This register selects a clock that is supplied to the 14-bit PWM.
PWDRU	This register sets the six high-order bits of the PWM output waveform data.
PWDRL	This register sets the eight low-order bits of the PWM output waveform data.
PWM	This is the PWM waveform output pin.

3. Operational Description

Figure 3.1 depicts the waveform diagrams used to describe the main principle of operation. As shown in figure 3.1, the output of a variable duty-cycle pulse is implemented by the 14-bit PWM function using both hardware and software means.

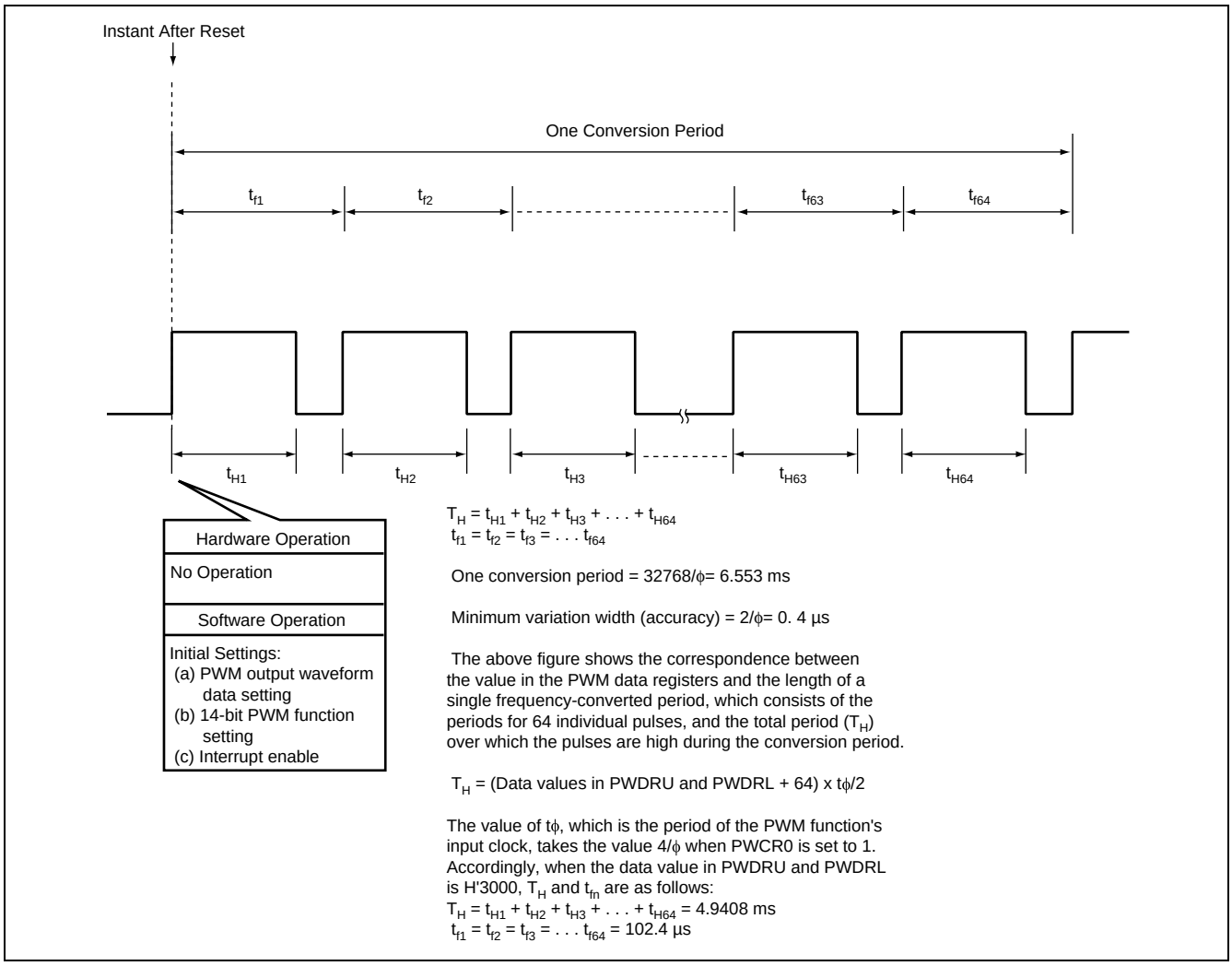

Figure 3.1 Operating Principle of Variable Duty-Cycle Pulse Output by the 14-Bit PWM Function

4. Software Description

4.1 Module Description

The module initializes the stack pointer, sets the 14-bit PWM function, and enables the interrupts.

Table 4.1 Module Description

Module Name	Label Name	Function
Main Routine	main	The main routine initializes the stack pointer, sets the auto-reload function, port 73, and the 8-bit counter, enables the interrupts, and controls on/off illumination of the LED.

4.2 Argument Description

Table 4.2 lists and describes the arguments applicable to this task example.

Table 4.2 Argument Description

Argument Name	Function	Used in	Data Size	I/O
duty_H	Six high-order bits of PWM output waveform data set in PWDRU	Main routine	1 byte	Input
duty_L	Eight low-order bits of PWM output waveform data set in PWDRL	Main routine	1 byte	Input

4.3 Description of Applicable Internal Registers

Table 4.3 lists the internal registers used in this task example.

Table 4.3 Description of Applicable Internal Registers

Register	Name	Functional Description	Address	Setting
PWCR	PWCR 0	PWM Control Register (clock select 0): When PWCR0 = 1, the clock supplied to the 14-bit PWM is set to ϕ/4.	H'FFBE Bit 0	1
PWDRU		PWM Data Register U: Sets the six high-order bits of the PWM output waveform data	H'FFBD	H'30
PWDRL		PWM Data Register L: Sets the eight low-order bits of the PWM output waveform data	H'FFBC	H'00
PMR1	PWM	Port Mode Register 1 (P14/PWM pin function switching) When PWM = 1, P14/PWM is set as PWM output pin function	H'FFE0 Bit 4	1

4.4 Description of RAM Used

RAM is not used in this task example.

5. Flow Chart

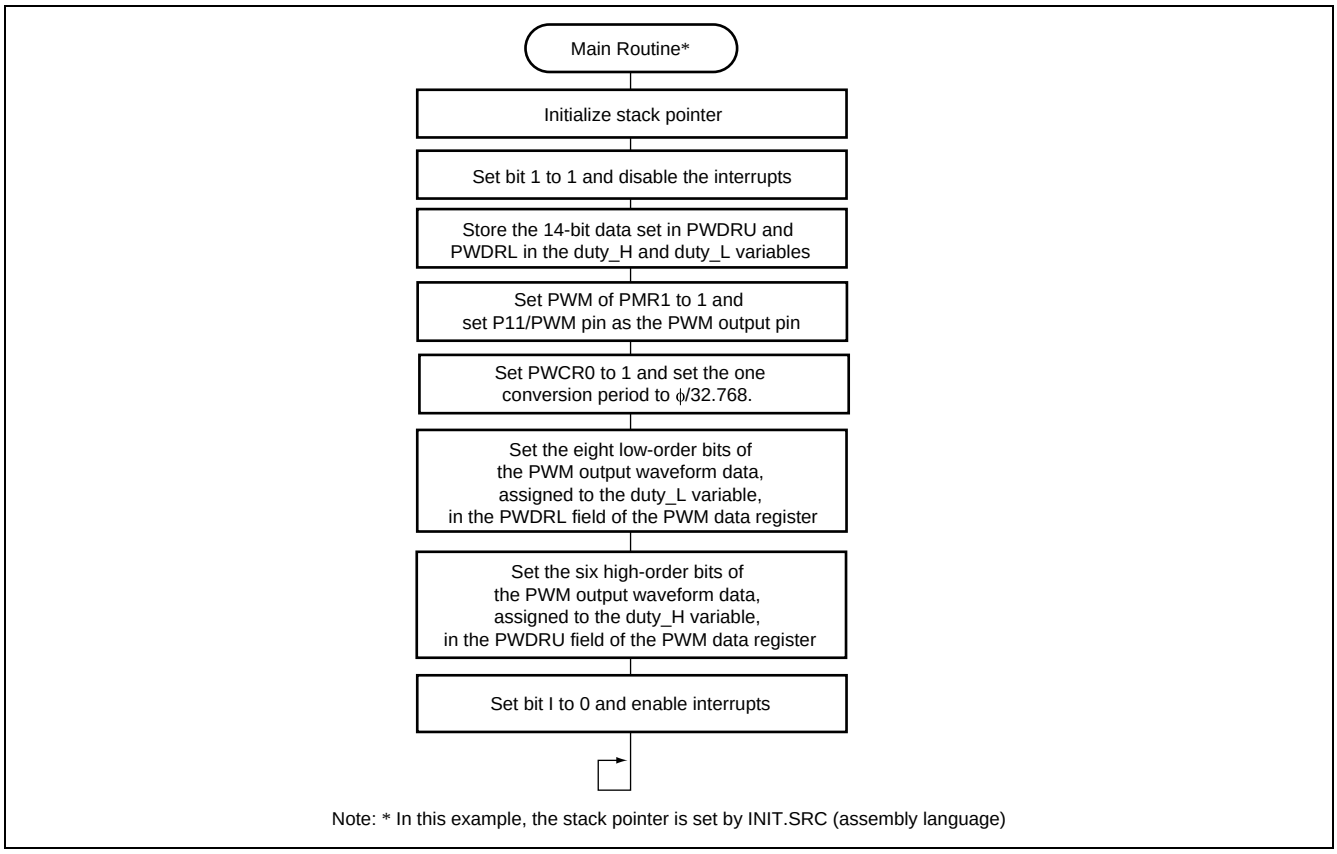

Figure 5.1 Main Routine

6. Program Listing

INIT.SRC (Program List)

```
            .EXPORT   _INIT
            .IMPORT   _main
 ;
        .SECTION  P,CODE
 _INIT:
        MOV.W     #H'FF80,R7
        LDC.B     #B'10000000,CCR
        JMP       @_main
 ;
       .END
```

```
/************************************************************/
/*                                                          */
/*  H8/300HN Series -H8/3687-                               */
/*  Application Note                                        */
/*                                                          */
/* 'Variable Duty-Cycle Pulse Output by 14-Bit PWM Function' */
/*                                                          */
/*  Function                                                */
/*  :14-bit PWM                                             */
/*                                                          */
/*  External Clock : 5 MHz                                  */
/*  Internal Clock : 5 MHz                                  */
/*  Sub Clock      : 32.768 kHz                             */
/*                                                          */
/************************************************************/

#include    <C:\ch38\include\machine.h>

/************************************************************/
/*  Symbol Definition                                       */
/************************************************************/

struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define     PWDRL*(volatile unsigned char *)0xFFBC        /* PWM Data Register L   */
#define     PWDRH*(volatile unsigned char *)0xFFBD        /* PWM Data Register H   */
#define     PWCR *(volatile unsigned char *)0xFFBE        /* PWM Control Register  */

#define     PMR1 *(volatile unsigned char *)0xFFE0        /* Port Mode Register 1  */
#define     PMR1_   BIT (*(struct BIT *)0xFFE0)           /* Port Mode Register 1  */
#define     PWM  PMR1_BIT.b2                              /* PWM Pin Function      */

#pragma     interrupt  (setdata)
```

```
/*******************************************************/
/* Function Definition                                 */
/*******************************************************/
extern    void    INIT ( void );                        /* SP Set               */
void      main         ( void );
extern    void    _INITSCT();
/*******************************************************/
/*    RAM define                                       */
/*******************************************************/
unsigned char    duty_H  ;                              /* Duty Setting Buffer High */
unsigned char    duty_L  ;                              /* Duty Setting Buffer Low  */

/*******************************************************/
/*   Vector Address                                    */
/*******************************************************/
#pragma    section        V1                           /* VECTOR SECTION SET */
void (*const VEC_TBL1[])(void) = {                     /* 0x00 - 0x0f */
    INIT                                               /* 00 Reset           */
};

#pragma    section                                     /* P                  */
/*******************************************************/
/*    Main Program                                     */
/*******************************************************/
void main ( void )
{
   _INITSCT();
    set_imask_ccr(1);                                  /* Interrupt Disable                        */
    duty_H = 0x30;                                     /* Initialize 14-Bit PWM Output Pulse Data */
    duty_L = 0x00;
    PWM    = 1;                                        /* Initialize PWM Output Pin Function      */
    PWCR   = 0xFF;                                     /* Initialize PWM Input Clock              */
    PWDRL  = duty_L;                                   /* Set 14-Bit PWM Output Pulse Data Higher */
    PWDRH  = duty_H;                                   /* Set 14-Bit PWM Output Pulse Data Lower  */
    set_imask_ccr(0);                                  /* Interrupt Enable                        */
    while(1){
    ;
  }
}
```

Link Address Designation

Section Name	Address
CV1	H'0000
P	H'0100
V	H'FB80