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SH7280 Group

12-Bit A/D Converter: Example of Settings for Conversion in Single-cycle Scan Mode

Introduction

This application note describes an example of settings for the 12-bit A/D converter in single-cycle scan mode as an example of application of the A/D converter of the SH7285.

Target Device

SH7285

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1. Preface

1.1 Specifications

- A/D conversion in single-cycle scan mode by the 12-bit A/D converter
- Three rounds of A/D conversion are performed on analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored in RAM.

1.2 Module Used

- 12-bit A/D converter (12-bit A/D)

1.3 Applicable Conditions

- MCU SH7285/SH7286/SH7243
- Operating frequency Internal clock: 100 MHz
Bus clock: 50 MHz
Peripheral clock: 50 MHz
- C compiler SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01 from Renesas Technology
- Compiler options -cpu = sh2a -include = "\$(WORKSPDIR)\inc"
-object = "\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr = auto
-chginclpath -errorpath -global_volatile = 0 -opt_range = all
-infinite_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1 -nologo

1.4 Related Application Note

None

2. Description of the Sample Application

The sample program employs the single-cycle scan mode of the 12-bit A/D converter to perform three rounds of A/D conversion on input channels 0 to 3 (AN0 to AN3), and then stores converted data in RAM.

2.1 Operational Overview of Module Used

The operating modes of the 12-bit A/D converter are single-cycle scan mode and continuous scan mode. In single-cycle scan mode, A/D conversion is performed once on each of one or more specified channels and then ends. The ADST bit is automatically cleared to 0. In continuous scan mode, A/D conversion is performed sequentially by software on one or more specified channels until the ADST bit is cleared to 0.

Additionally, channels 0 to 2 have dedicated sample-and-hold circuits, so multiple channels are capable of simultaneous sampling.

Table 1 gives an overview of the module used in this sample application (i.e. the A/D converter) and figure 1 is a block diagram of 12-bit A/D converter. For details on the 12-bit A/D converter, see the section on the A/D converter in the *SH7280 Group Hardware Manual*.

Table 1 Overview of the Module (A/D Converter) Used in the Sample Application

Item	Description
Resolution	12 bits
Minimum conversion time	1.0 μ s per channel ($P\phi = 50$ MHz)
Number of modules	2 (SH7285, SH7243), 3 (SH7286)
Input channels	8 (SH7285, SH7243), 12 (SH7286)
Operating modes	Single-cycle scan mode Continuous scan mode
Sample-and-hold function	Common to 0 to 3 channels: 1 circuit Common to 4 to 7 channels: 1 circuit Common to 8 to 11 channels: 1 circuit Dedicated for individual channels: 1 circuit each for ch0 to ch2 (3 in all)
Sources for activation of A/D conversion	Software: Setting of the ADST bit Timer: TRGAN, TRG0N, TRG4AN, and TRG4BN signals from the MTU2 module TRGAN, TRG4AN, and TRG4BN signals from the MTU2S module External trigger: ADTRG

Example of Settings for Conversion in Single-Cycle Scan Mode

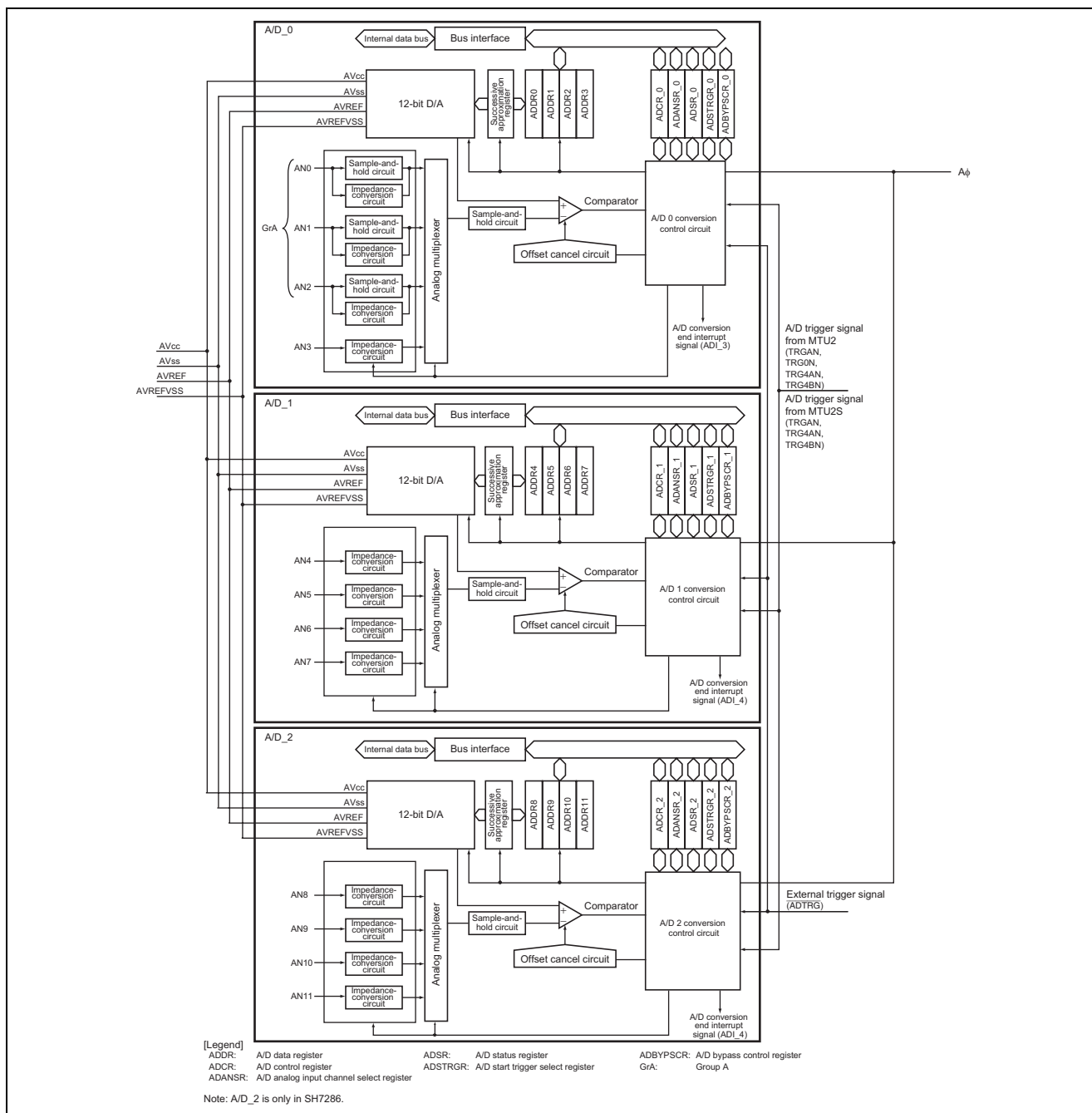


Figure 1 Block Diagram of the 12-Bit A/D Converter

2.2 Procedure for Setting Module Used

Figure 2 shows an example of the initialization sequence of A/D conversion in single-cycle scan mode. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual*.

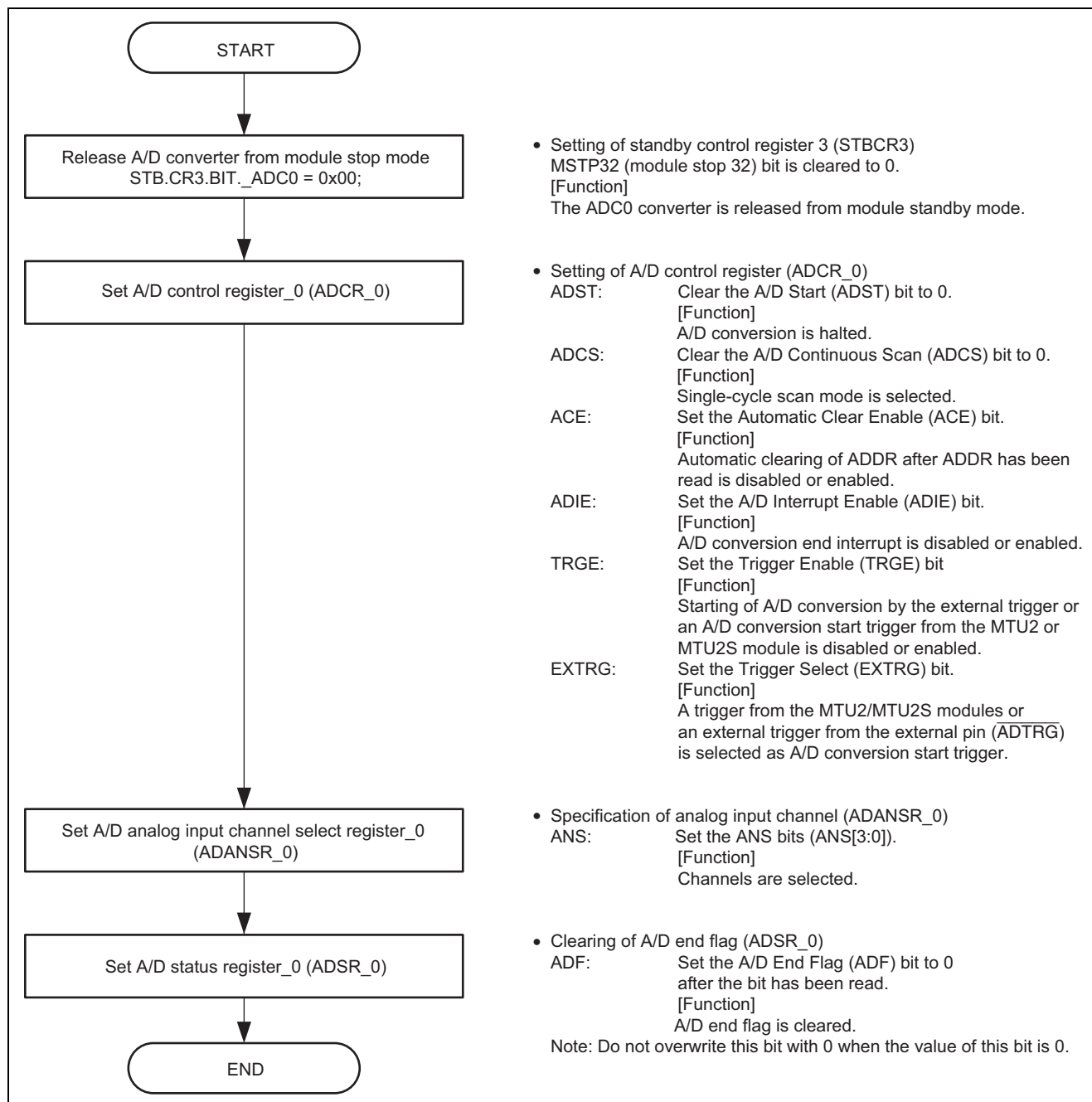


Figure 2 Initialization Sequence for 12-Bit A/D Conversion

2.3 Operation of the Sample Program

In this sample program, A/D conversion in single-cycle scan mode is performed on channels 0 to 3 (AN0 to AN3). The A/D converter is activated by software and converted data are stored in RAM. This processing is repeated three times.

Table 2 gives a description of RAM usage in this sample program.

Table 2 Variables Used in the Sample Program

Variable Name	Description	Area	Name of Employing Module
unsigned short Ad_data[AD][CH]	Array for storing A/D-converted data (2 bytes/datum)	On-chip RAM	io_ad_1cyc_scan (unsigned short*ad_buf)

2.4 Sequence of Processing by the Sample Program

Table 3 gives settings for registers used in the sample program and figure 3 shows the flow of handling the sample program.

Table 3 Register Settings Used in Sample Program

Register Name	Address	Setting	Description
A/D control register_0 (ADCR_0)	H'FFFF E800	H'00	ADST = 0: Halts A/D conversion ADCS = 0: Single-cycle scan mode ACE = 0: Disables automatic clearing of the ADDR ADIE = 0: Disables A/D conversion end interrupt TRGE = 0: Disables starting of A/D conversion by an external trigger or by the MTU2 and MTU2S modules
		H'80	ADST = 1: Starts A/D conversion

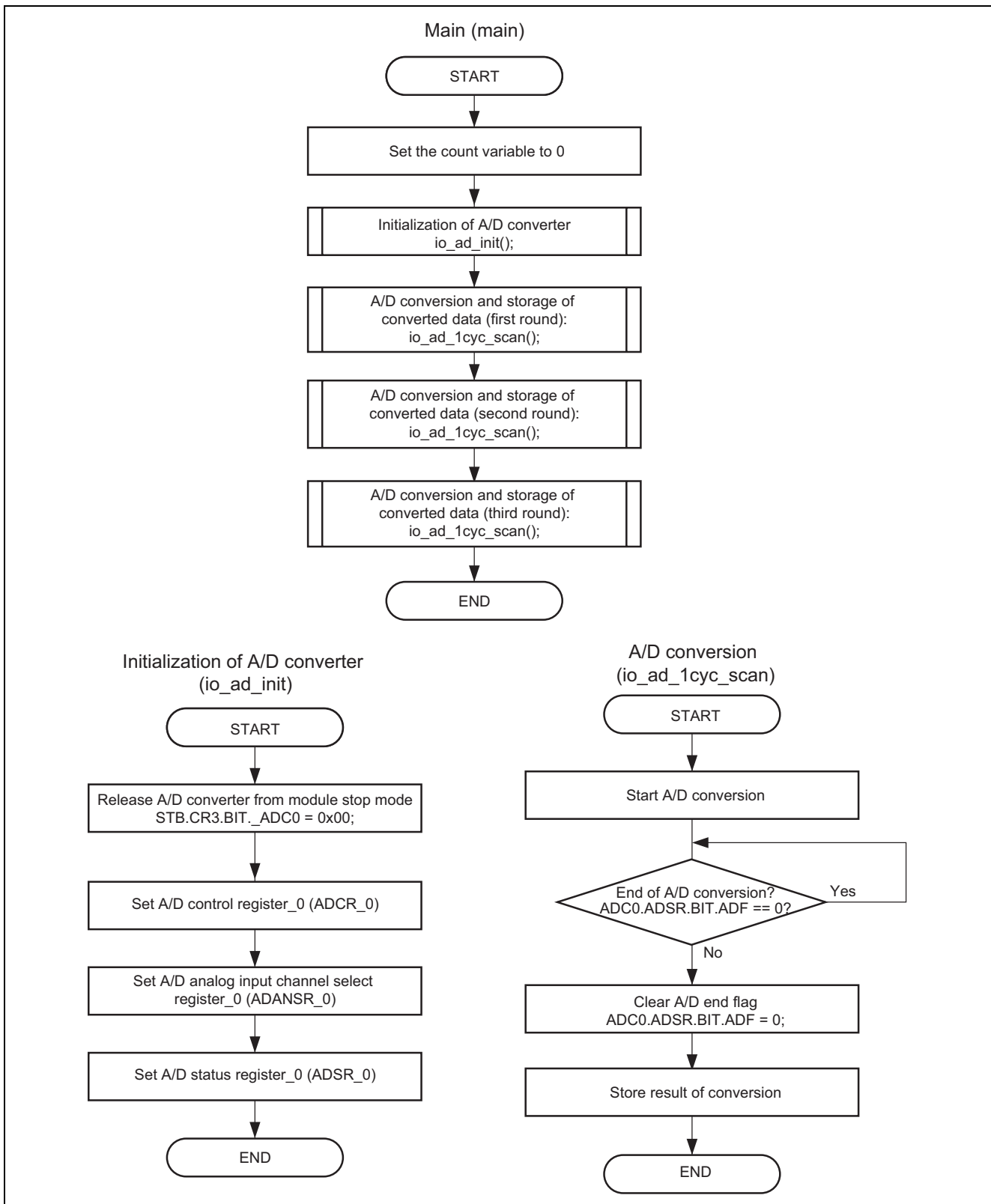


Figure 3 Flow of Handling the Sample Program

3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```

1      /*"FILE COMMENT"*****
2      *
3      *      System Name : SH7285 Sample Program
4      *      File Name   : main.c
5      *      Contents   : Sample program for A/D conversion in single-cycle scan mode
6      *      Version    : 1.00.00
7      *      Model     : M3A-HS85
8      *      CPU       : SH7285
9      *      Compiler  : SHC9.1.1.0
10     *      note      : A/D conversion in single-cycle scan mode is performed by the A/D
11     *                  converter. Three rounds of A/D conversion on analog input channels 0
12     *                  to 3 (AN0 to AN3) proceed, and the converted data are stored in RAM.
13     *
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21     *
22     *      history   : 2008.02.26 ver.1.00.00
23     *"FILE COMMENT END"*****/
24     #include <machine.h>
25     #include "iodefine.h"      /* SH7285 iodefine */
26
27     /* ==== prototype declaration ==== */
28     void main(void);
29     void io_ad_init(void);
30     void io_ad_lcyd_scan(unsigned short *ad_buf);
31
32     /* ==== symbol definition ==== */
33     #define AD 3
34     #define CH 4
35
36     /* ==== RAM allocation variable declaration ==== */
37     unsigned short Ad_data[AD][CH];
38

```

2. Sample Program Listing: main.c (2)

```

39  /*"FUNC COMMENT"*****
40  * Outline      : main
41  *-----
42  * Include      : #include "iodefine.h"
43  *-----
44  * Declaration  : void main(void);
45  *-----
46  * Function     : AD translation with 1 cycle scan mode
47  *-----
48  * Argument     : void
49  *-----
50  * Return Value: void
51  *-----
52  * Notice      : non
53  /*"FUNC COMMENT END"*****/
54 void main(void)
55 {
56     unsigned char count;
57     count = 0;
58
59     /* ==== Initial Setting of ADC ==== */
60     io_ad_init();
61
62     /* ==== A/D convert ==== */
63     io_ad_1cyc_scan(&Ad_data[count][0]);
64     count++;
65     io_ad_1cyc_scan(&Ad_data[count][0]);
66     count++;
67     io_ad_1cyc_scan(&Ad_data[count][0]);
68
69     while(1){
70         /* loop */
71     }
72 }
73
74 /*"FUNC COMMENT"*****
75 * Outline      : Initial setting of ADC
76 *-----
77 * Include      : #include "iodefine.h"
78 *-----
79 * Declaration  : void io_ad_init(void);
80 *-----
81 * Function     : Initial setting of ADC
82 *-----
83 * Argument     : void
84 *-----
85 * Return Value: void
86 *-----
87 * Notice      : non
88 /*"FUNC COMMENT END"*****/
89

```

3. Sample Program Listing: main.c (3)

```

90 void io_ad_init(void)
91 {
92     /* ==== Release of power down mode(ADC0) ==== */
93     STB.CR3.BIT._ADC0 = 0x00;
94
95     /* ==== Setting of ADC ==== */
96     /* ---- A/D Control Register(ADCR) ---- */
97     ADC.ADCR.BYTE = 0x00;
98     /* 7   = b'0   : A/D End Flag                               */
99     /* 6   = b'0   : Single-cycle scan                         */
100    /* 5   = b'0   : Automatic clearing of the ADDR
101                    after being read is disabled              */
102    /* 4   = b'0   : Generation of A/D conversion end
103                    interrupt is disabled                      */
104    /* 3-2 = b'0   : reserve                                    */
105    /* 1   = b'0   : A/D conversion start by the external trigger
106                    or an A/D conversion start trigger from
107                    the MTU or MTU2S is disabled              */
108    /* 0   = b'0   : A/D converter is started by the A/D conversion
109                    start trigger from the MTU2 or MTU2S      */
110
111    /* ---- A/D Analog Input Channel Select Register(ADANSR) ---- */
112    ADC.ADANSR.BYTE = 0x0f; /* AN0-AN3 */
113
114    /* ---- A/D Status Register(ADSR) ---- */
115    if(ADC0.ADSR.BIT.ADF == 0x01){
116        ADC0.ADSR.BIT.ADF = 0x00; /* ADF clear */
117    }
118 }
119
120 /*"FUNC COMMENT"*****
121 * Outline      : A/D convert
122 *-----
123 * Include      : #include "iodefine.h"
124 *-----
125 * Declaration  : void io_ad_lcyc_scan(unsigned short *ad_buf);
126 *-----
127 * Function     : The clearance of an ADF flag, storing of conversion data
128 *-----
129 * Argument     : void
130 *-----
131 * Return Value: void
132 *-----
133 * Notice      : non
134 *"FUNC COMMENT END"*****/
135 void io_ad_lcyc_scan(unsigned short *ad_buf)
136 {
137     ADC.ADCR.BIT.ADST = 1; /* A/D conversion start */
138
139     while(ADC.ADSR.BIT.ADF == 0){
140         /* A/D conversion completion waiting */
141     }
142
143     ADC.ADSR.BIT.ADF = 0; /* ADF clear */
144     *ad_buf++ = ADC.ADDR0; /* AN0 */
145     *ad_buf++ = ADC.ADDR1; /* AN1 */
146     *ad_buf++ = ADC.ADDR2; /* AN2 */
147     *ad_buf++ = ADC.ADDR3; /* AN3 */
148 }
149 /* End of File */

```

4. Documents for Reference

- Software Manual
SH-2A, SH2A-FPU Software Manual
The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
SH7280 Group Hardware Manual
The most up-to-date version of this document is available on the Renesas Technology Website.

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