AN-1083
SPI Parallel to Serial Converter

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Introduction

The Serial-Parallel Interface (SPI) bus is a synchronous serial communication interface specification made popular by Motorola before it spun off to Freescale and then acquired by NXP. Typical applications include SDIO and LCD. GreenPAK4 includes a SPI slave macro-cell. The purpose of this application note is to demonstrate the SPI macro-cell's parallel to serial (P2S) mode configuration. AN-1065 covers serial to parallel (S2P) mode configuration. Specific to GreenPAK4, P2S applications include converting ADC or FSM counter data into standard SPI serial data for system-level communication. Please note the SPI macro-cell cannot send and receive serial data in the same application; it is set up either in S2P or P2S mode.

P2S Converter Design

A P2S design is shown in figure 1 and its SPI macro-cell's properties are shown in figure 2. This example is built in SLG46620. The FSM0 counter is used as a parallel input source for demonstration purposes only. In figure 1, the thicker orange line signifies an 8-bit bus going into the SPI macro-cell. Several notes to point out:

1. P2S mode doesn't support sampling on the leading (1st) clock edge (CPHA=0); make sure sampling occurs on the trailing (2nd) clock edge by setting CPHA = 1. S2P mode supports CPHA=0.

2. Master Input Slave Output (MISO) outputs data either at SPI clock (SCLK)'s rising edge or falling edge. This is configured by setting the base value of the clock to either "0" or "1" respectively under "Clock polarity" (CPOL) in properties.

3. Either one or two bytes can be converted at a time; this example converts one byte at a time.

4. The ADC, PWM, and FSM data can sync with the SPI clock even when they are not from the same clock source. The data sync options accomplish this by stopping the respective clocks while the parallel data is loaded into the SPI macro-cell. There will be no runt pulses since clocks are gated.

5. SPI macro-cell can accept parallel data either from the FSM counter or ADC macro-cell.

6. MISO can only route to pin 10 (pin 12 in SLG46140); make sure it is configured as a digital output.

7. The "INTR" pin pulses high for one clock period each time data after transmission completes. When CPOL=0, this pulse starts at the 8th/16th falling clock edge. Likewise when CPOL=1, interrupt starts at the 8th/16th rising clock edge.

P2S Converter Operation

The P2S Design in figure 1 uses FSM0 counter as its input. This is for demonstration purpose only since it is easy to set FSM0's value. In this example, FSM0's counter data is set at 169, or 1010,1001 in binary. The SPI macro-cell grabs this value and converts it to serial format, outputting the MSB first.

For proper P2S operation, please observe below steps in sequence:

1. Enable SPI macro-cell by pulling nCSB pin low.

2. SCLK's 1st edge should occur at least 250ns after nCSB is pulled low. Unexpected behavior can occur if nCSB and SCLK edges are concurrent.

3. After data transmission is complete on MISO, SPI's INTR pin will pulse high.

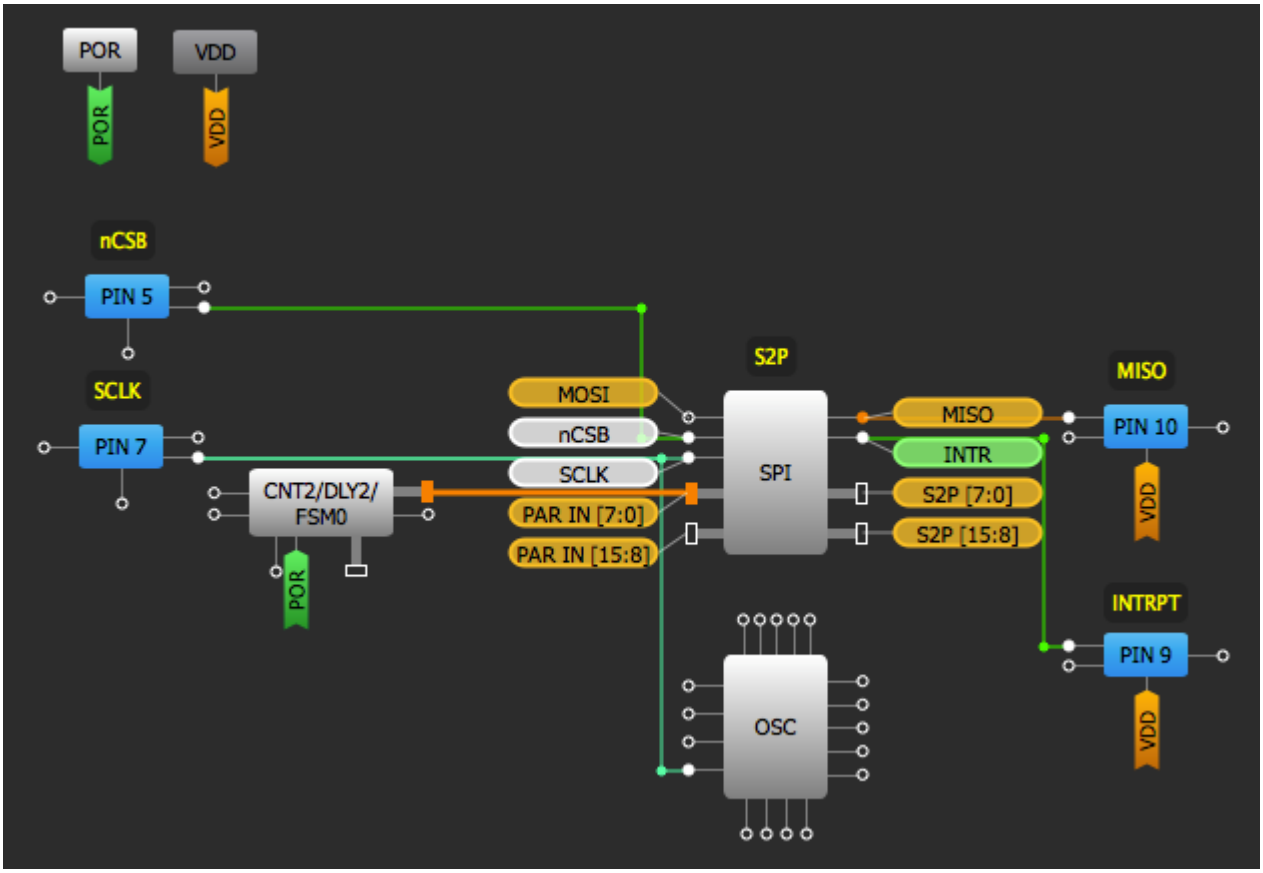

Figure 1. P2S Converter Design

4. Stop SCLK at least 250ns after INTR rising edge; MISO will output repeated data if SCLK is not stopped.

5. Disable SPI macro-cell by pulling nCSB pin high at least 250ns after last SCLK edge.

Figure 4 shows proper SPI timing waveform with CPOL=0. Channel 3 is the serial output MISO. Notice that it is outputting 10101001 with respect to the rising edge of SCLK.

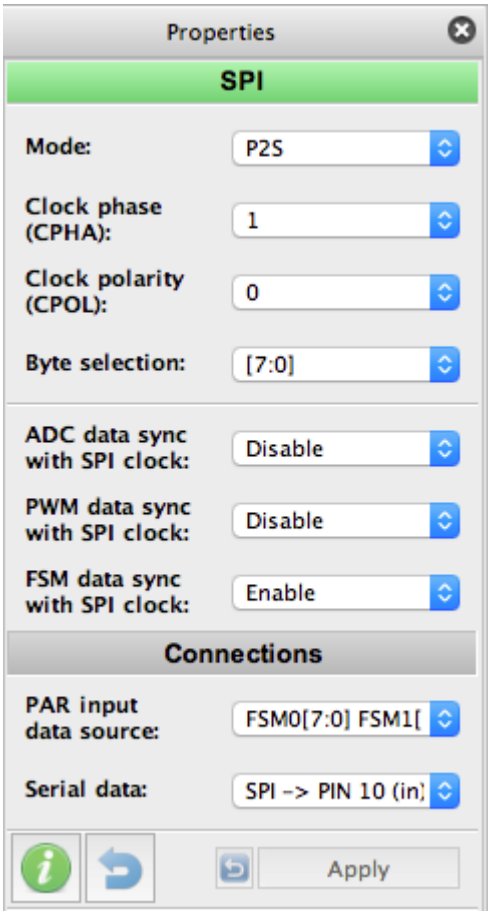

Figure 2. P2S Configuration

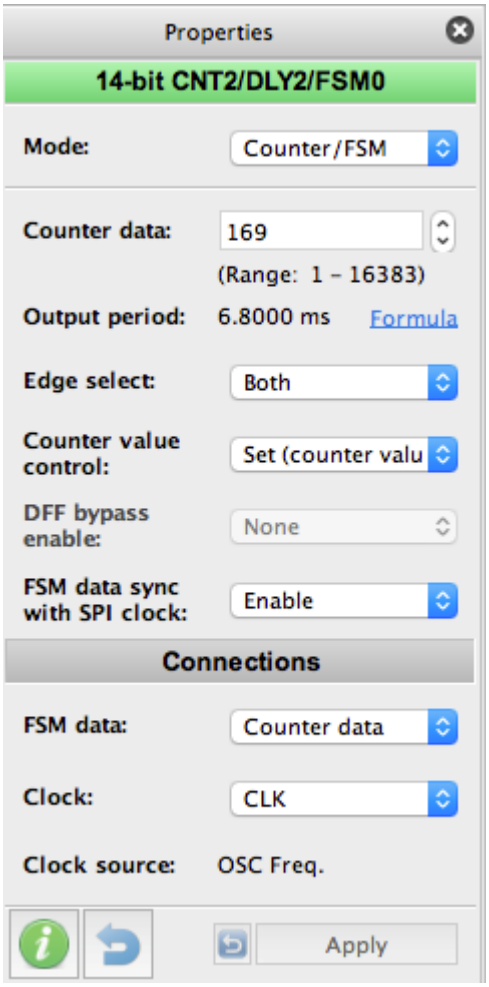

Figure 3. FSM0 Properties

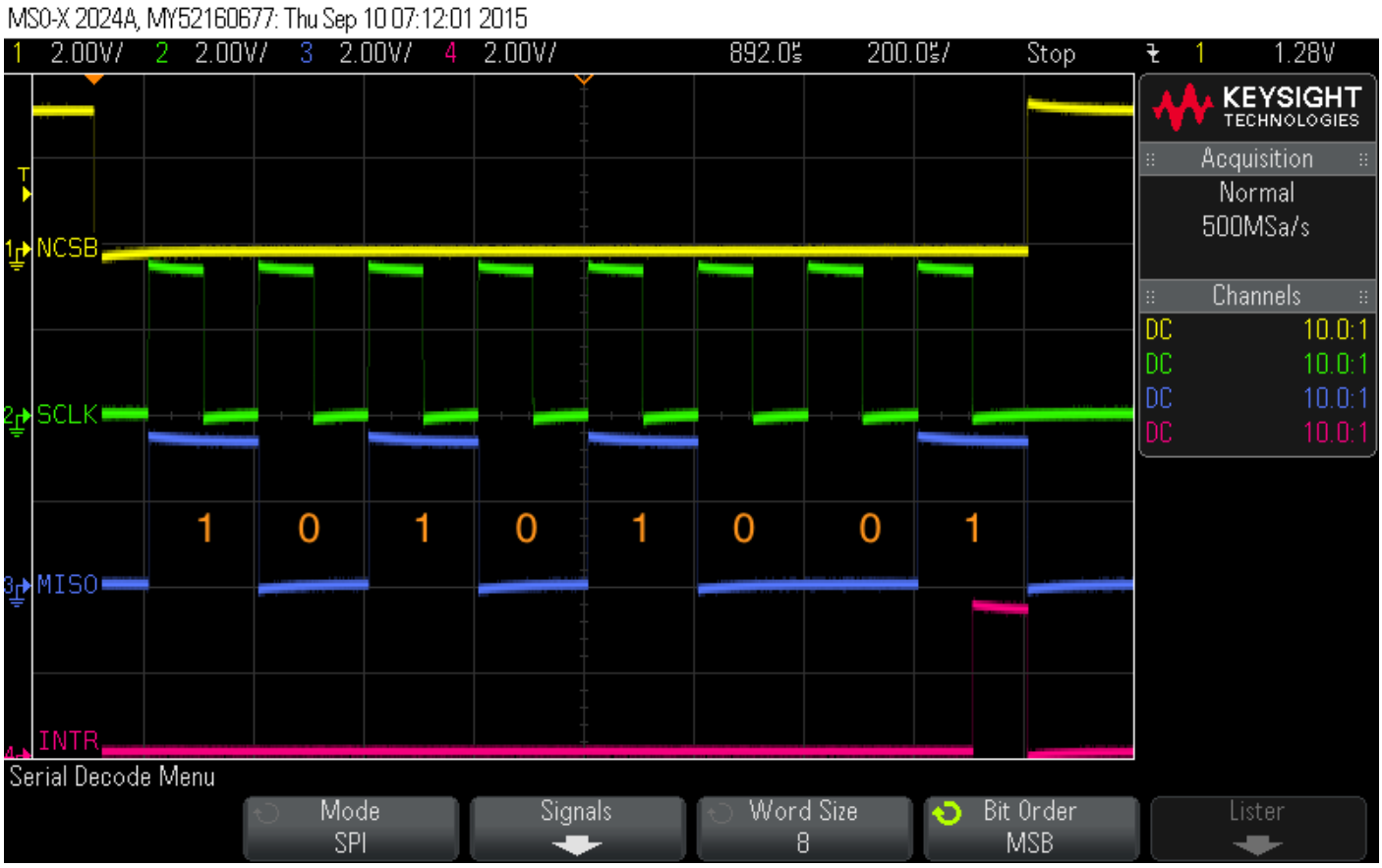

Figure 4. SPI Timing Waveform with CPHA=1 and CPOL=0

For completeness' sake, figure 5 shows proper SPI timing waveform with CPOL=1. Notice that MISO is outputting 10101001 with respect to the falling edge of SCLK.

Possible Applications

Let's take sensor timing for example. Window comparators are often used to count time between tripped thresholds. This data can be recorded in the FSM counter, and then outputted as serial data via the SPI macro-cell.

often used when ADC or counter data needs

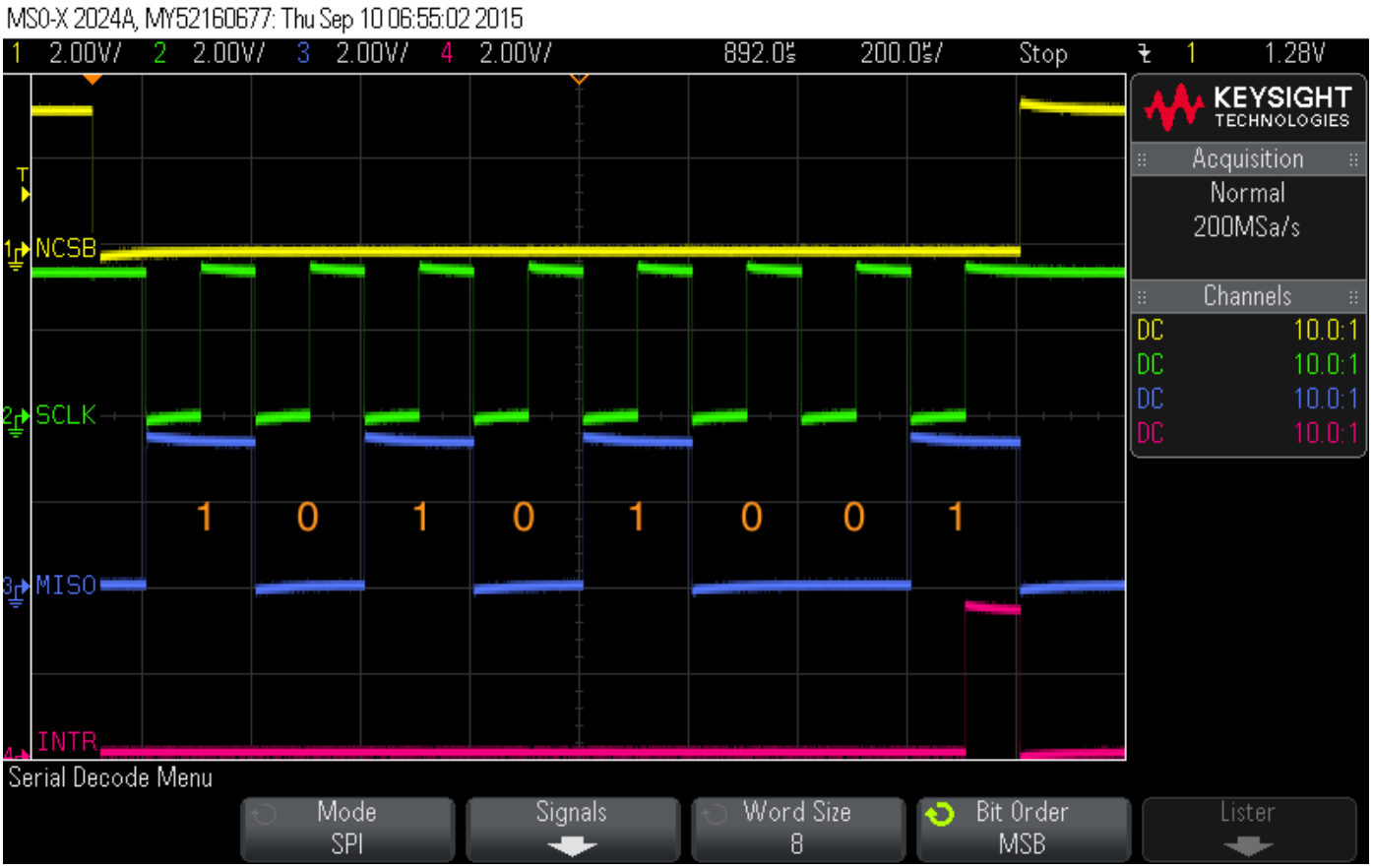

Figure 5. SPI Timing Waveform with CPHA=1 and CPOL=1

to be written to another chip in the system via SPI.

Conclusion

GreenPAK4's SPI block provides a convenient communication interface for the GreenPAK to other chips in the system. The P2S mode is

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