Pulse Width Stretcher
SLG46140

This application note shows how the SLG46140 GreenPAK device can be used to stretch the duration width of an input pulse. The output pulse will have a duration width that will be integer N times the duration width of the input pulse. This application note comes complete with design files which can be found in the References section.

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1. References

For related documents and software, please visit:

https://www.renesas.com/eu/en/products/programmable-mixed-signal-asic-ip-products/greenpak-programmable-mixed-signal-products

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] Pulse Width Stretcher.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

2. GreenPAK Design

The GreenPAK design using the SLG46140 device for the pulse width stretcher is shown in Figure 1.

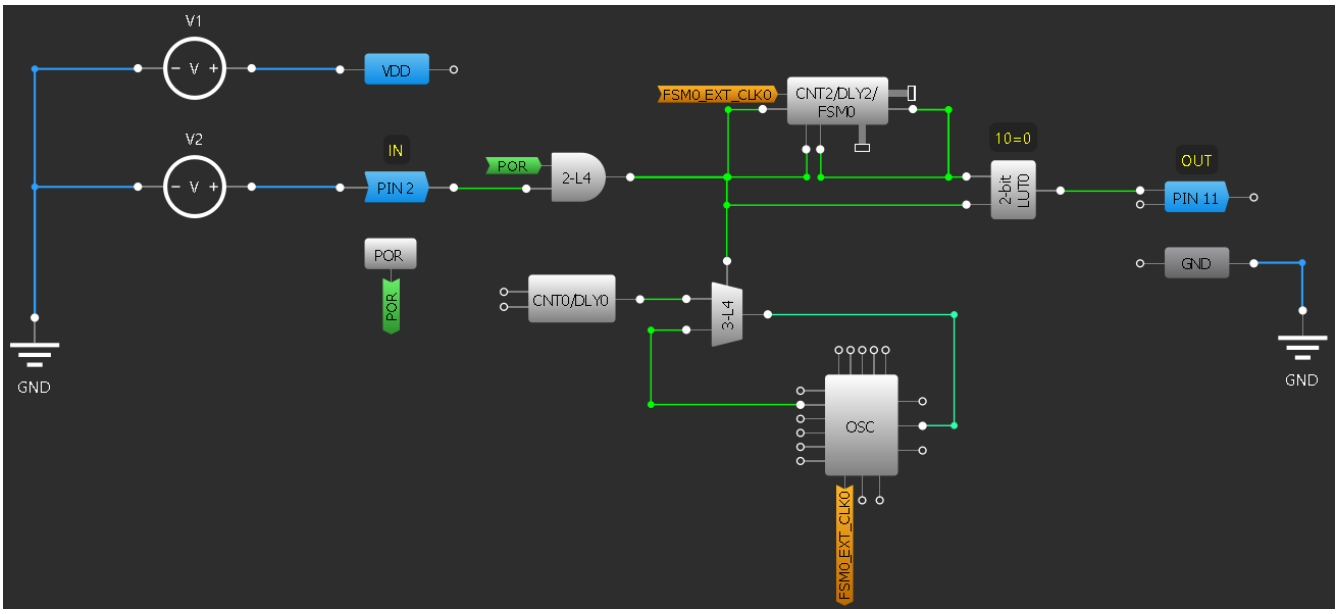

Figure 1. Pulse Width Stretcher GreenPAK design

The circuit operation concept is described in the following steps:

- While the input IN (PIN 2) is held low, the output OUT (PIN 11) is held low.
- When the input IN goes to a digital high level, the CNT2/DLY2/FSM0 counter is reset and the output OUT goes to a high level too. The CNT2/DLY2/FSM0 resets at the input signal rising edge and the counter output goes to a low level.
- While the input IN is at a high level, the counter CNT2/DLY2/FSM0 up counts at a frequency defined by the OSC output.
- When the input IN falls down, the counter CNT2/DLY2/FSM0 starts to down count at a lower frequency defined by the counter CNT0/DLY0 (CLK divided by (COUNTER DATA + 2)). The output OUT is held at a high level while the CNT2 counts down.
- The CNT2/DLY2/FSM0 counts down until zero. When it reaches zero, the output OUT goes to a low level and the counter output goes to a high level.

The LUT 2-L4 is an AND port used as an enabler, allowing the input signal just after the completion of the internal POR sequence. The LUT 3-L4 is used as a multiplexer. It switches the clock frequency used by the CNT2/DLY2/FSM0 counter accordingly to the value of the input signal IN. And the LUT 2-L0 is configured to output low (0) just when the CNT2 output is high (1) and the input signal IN is low.

The configuration of the CNT2/DLY2/FSM0 counter, CNT0/DLY0, and OSC are shown in Figure 2.

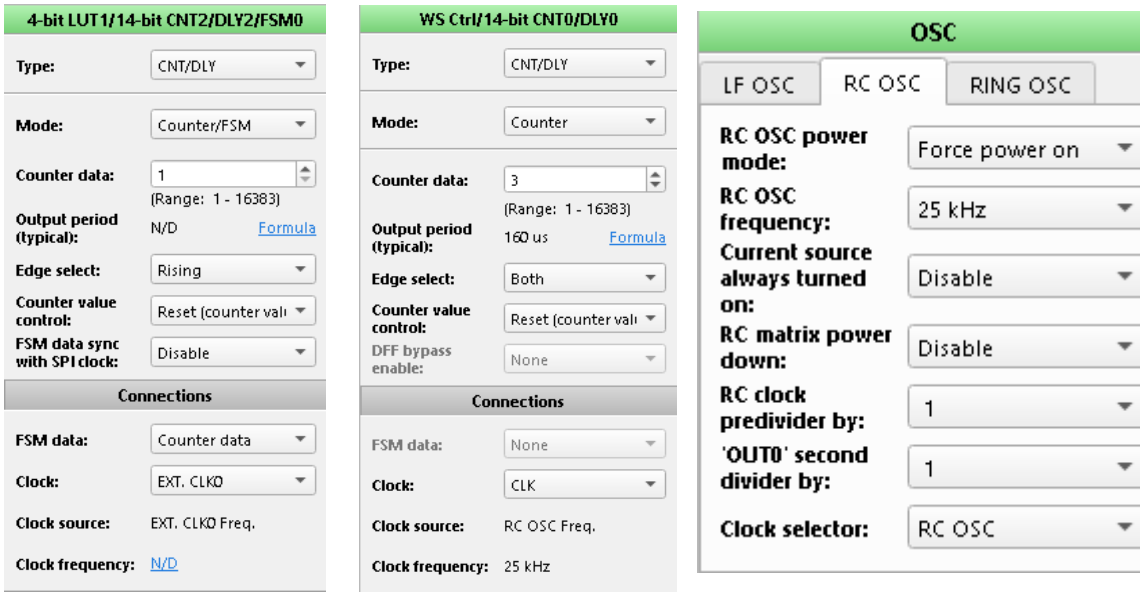

Figure 2. Components configuration from left to right: CNT2/DLY2/FSM0; CNT0/DLY0; OSC

3. Design Behavior Under Different Pulse Conditions

The design described in the last section will multiple the pulse width duration by an integer N in normal conditions. But, under boundary conditions, the behavior will be different and output pulse width will be different too. The pulse width has a minimum (T_{min}) and maximum (T_{max}) duration that is defined by the oscillator (OSC) frequency and by the CNT2/DLY2/FSM0 counter limit. These values are defined by:

$$T_{min} = \frac{1}{F_{OSC}}$$

$$T_{max} = \frac{2^{14}}{F_{OSC}}$$

Where F_{OSC} is the oscillator frequency

Considering these limit timings is possible to define four different operation cases, defined as:

1. Normal case, where $T_{min} < T_{IN} < T_{max}$;
2. Input pulse width too large, where $T_{IN} > T_{max}$;
3. Input pulse width too short, where $T_{IN} < T_{min}$;
4. Input pulse period too short (a second pulse is shot in the input while the stretched output is high).

In the next sub-sections, a test case with circuit simulation and, implementation measurements, for each operation case is discussed. In each test case, it is shown how to calculate the output pulse width.

3.1 Normal Case

If $F_{OSC} = 25kHz$, then $T_{min} = 40\mu s$ and, $T_{max} = 665.36ms$. , then
Consider $T_{IN} = 10ms$ and $CNT3\ Data = 5$

In this case, the output pulse width duration (T_{OUT}) will be:
$T_{OUT} = T_{IN} * (CNT3\ Data + 2) = 10ms * (5 + 2) = 70ms$

Figure 3 shows the implementation test result for this operation case. In Figure 4 the respective simulation result is shown.

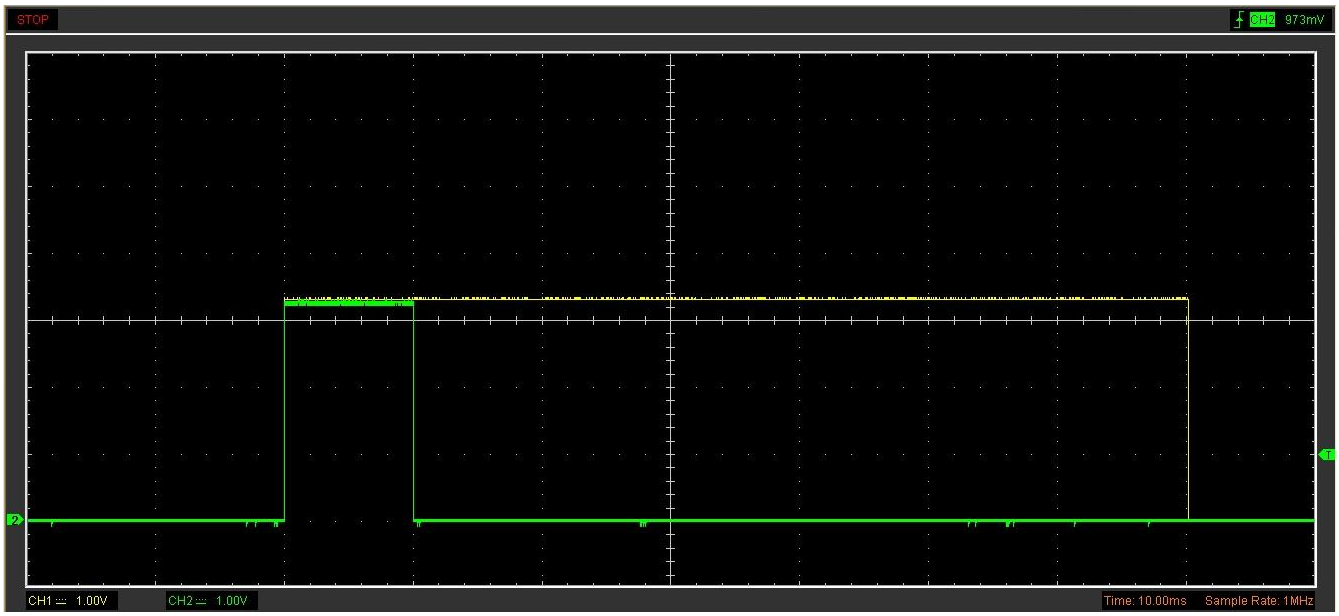

Figure 3. Normal case test - Channel 1 (CH1 - Yellow) is the output signal and Channel 2 (CH2 - Green) is the input signal. Time division is 10ms per division

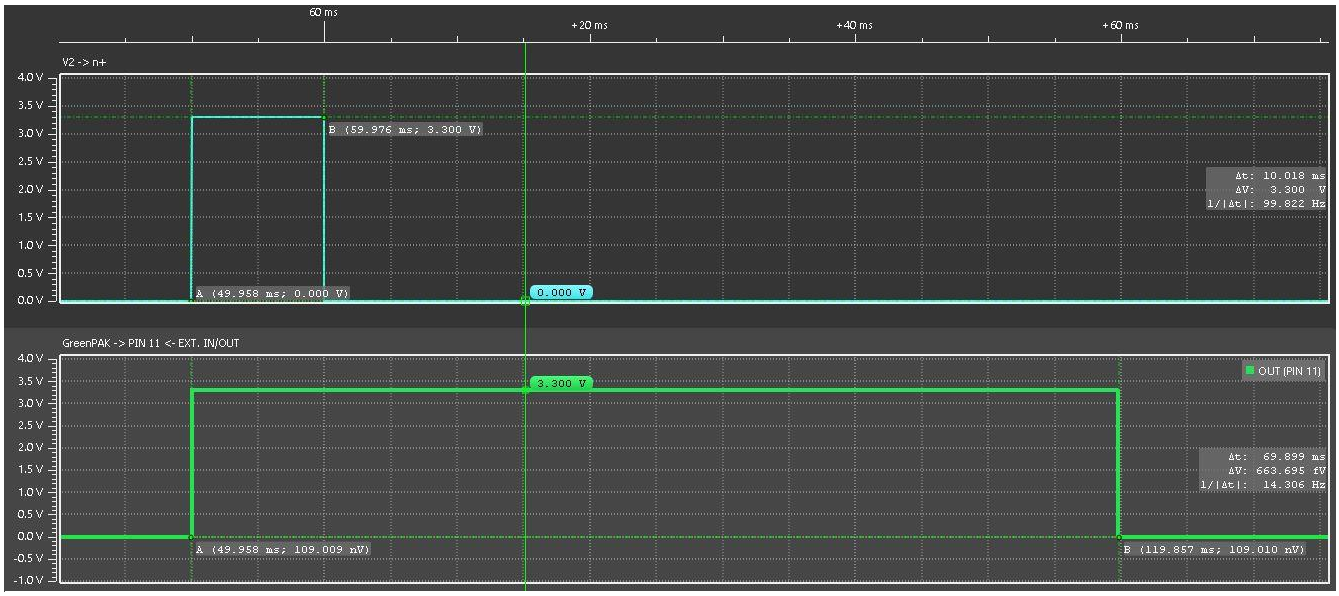

Figure 4. Normal simulation case - Input signal is on top and, output signal is on bottom

3.2 Input Pulse Width Too Large

If $F_{OSC} = 2MHz$, then $T_{min} = 500ns$ and, $T_{max} = 8.192ms$, then
Consider $T_{IN} = 10ms$ and $CNT3\ Data = 4$

In this case, the output pulse width duration (T_{OUT}) will be:

$$T_{OUT} = T_{IN} + \frac{CNT2\ bitrate * (CNT3\ Data + 1)}{F_{OSC}} = 10ms + \frac{16384 * (4 + 1)}{2MHz} = 50.96ms$$

Figure 5 shows the implementation test result for this operation case. Figure 6 shows the respective simulation.

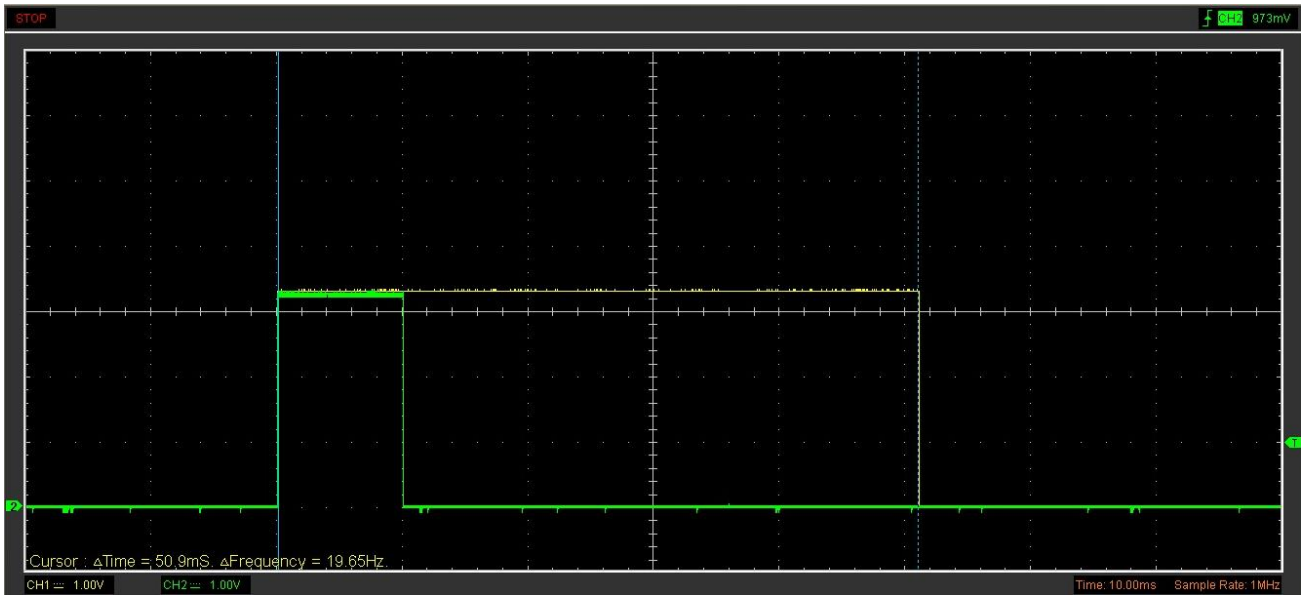

Figure 5. Pulse width is too large test case - Channel 1 (CH1 - Yellow) is the output signal and Channel 2 (CH2 - Green) is the input signal. Time division is 10ms per division. The cursor shows the measured output pulse width duration

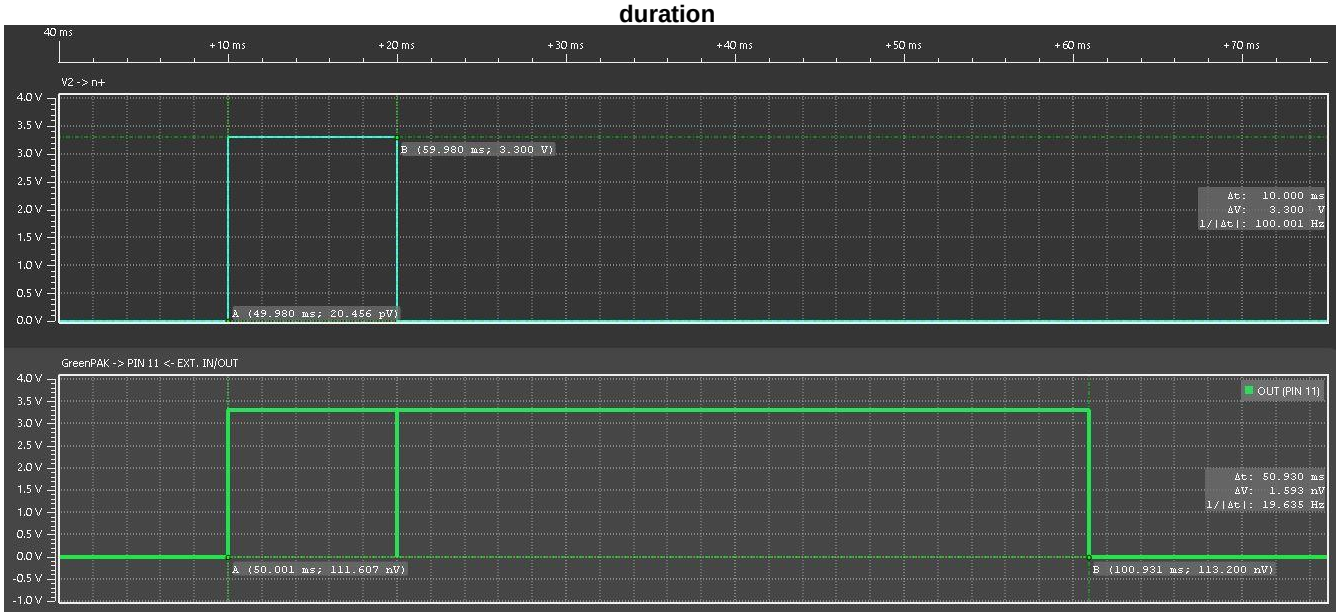

Figure 6. Pulse width is too large simulation case - Input signal is on top and, output signal is on bottom

3.3 Input Pulse Width Too Short

If $F_{OSC} = 25kHz$ and if $CLK/12$ is used by the counters instead of $CLK\ OSC$ output, then $T_{min} = 480\mu s$ and $T_{max} = 7.86432s$.

Consider $T_{IN} = 100\mu s$ and $CNT3\ Data = 4$

In this case, the output pulse width duration (T_{OUT}) will be:
$T_{OUT} = T_{IN}$

Figure 7 shows the implementation test result for this operation case and, Figure 8 shows the respective simulation.

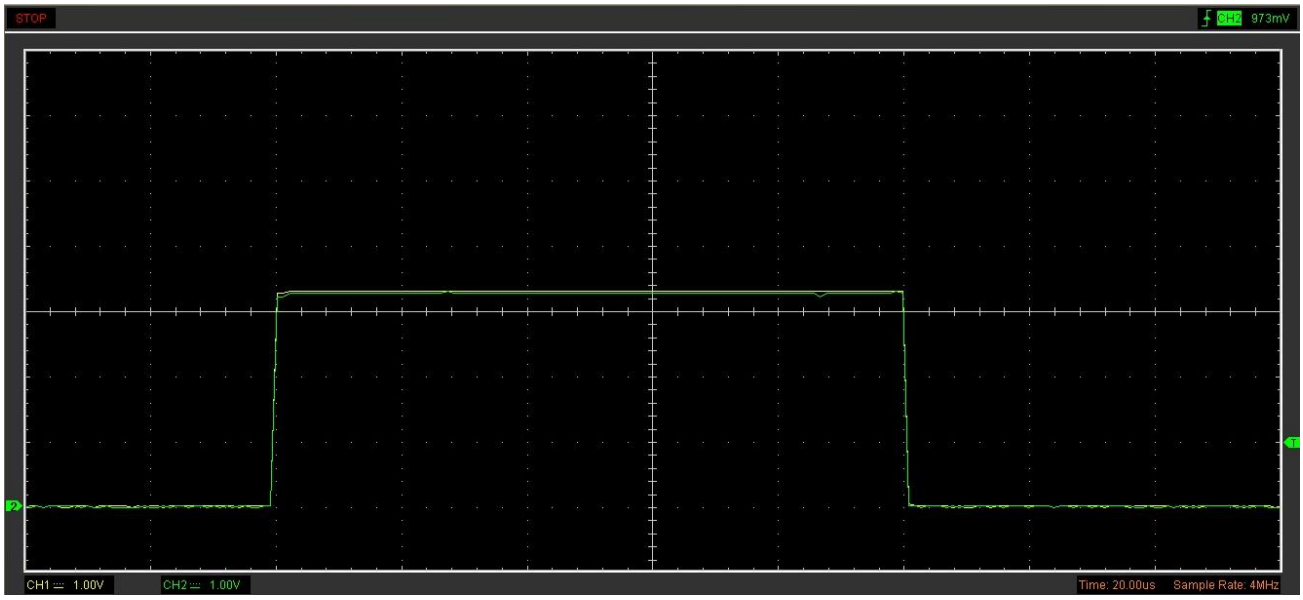

Figure 7. Pulse width is too short test case- Channel 1 (CH1 - Yellow) is the output signal and Channel 2 (CH2 - Green) is the input signal. Time division is 10ms per division

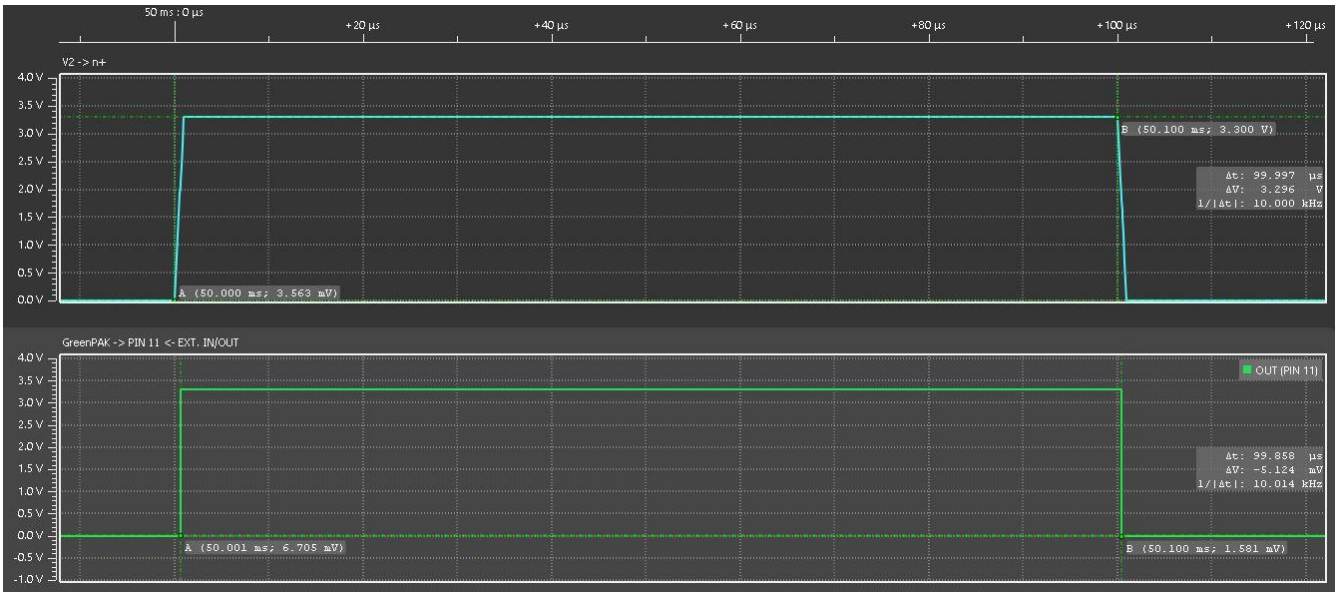

Figure 8. Pulse width is too short simulation case - Input signal is on top and, output signal is on bottom

3.4 Input Pulse Period Too Short

If $F_{OSC} = 25kHz$, then $T_{min} = 40\mu s$ and, $T_{max} = 665.36ms$, then
Consider $T_{IN} = 10ms$ and $CNT3\ Data = 3$. Consider the input pulse period of 30ms.

In this case, the output pulse width duration (T_{OUT}) will be:
$T_{OUT} = T_{INP} * (N - 1) + T_{IN} * (CNT3\ Data + 2) = 30ms * (2 - 1) + 10ms * (3 + 2) = 80ms$

Where T_{INP} is the input pulses period and N is the pulses quantity

Figure 9 shows the implementation test result for this operation case and, Figure 10 shows the respective simulation.

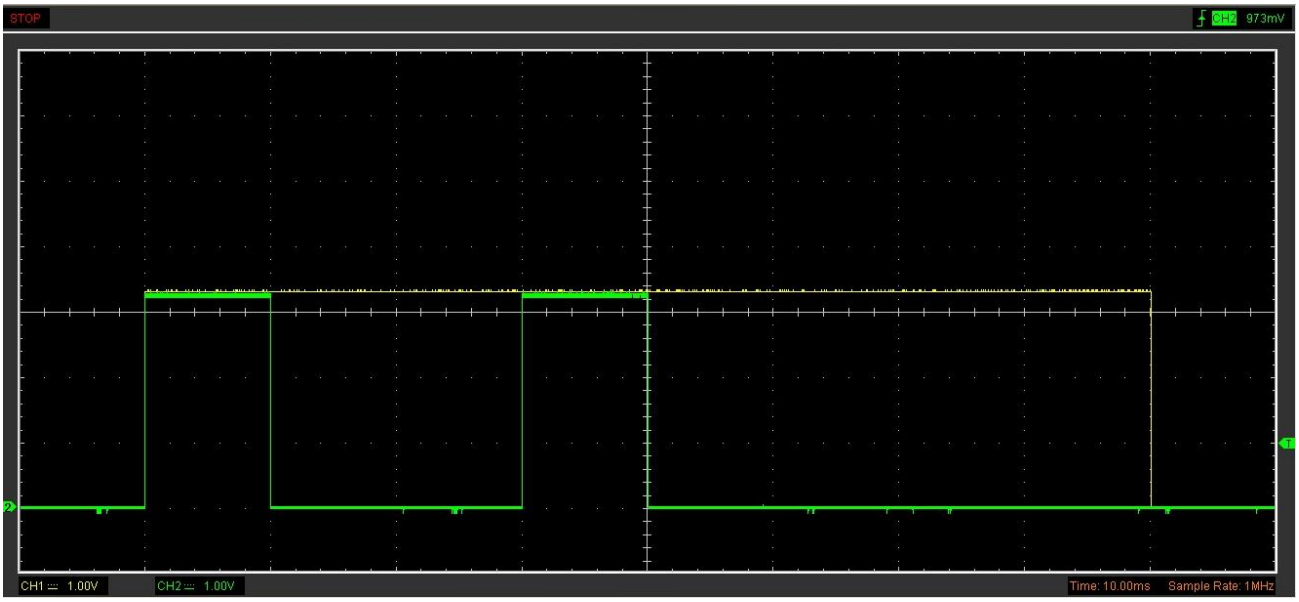

Figure 9. Pulse period is too short test case- Channel 1 (CH1 - Yellow) is the output signal and Channel 2 (CH2 - Green) is the input signal. Time division is 10ms per division

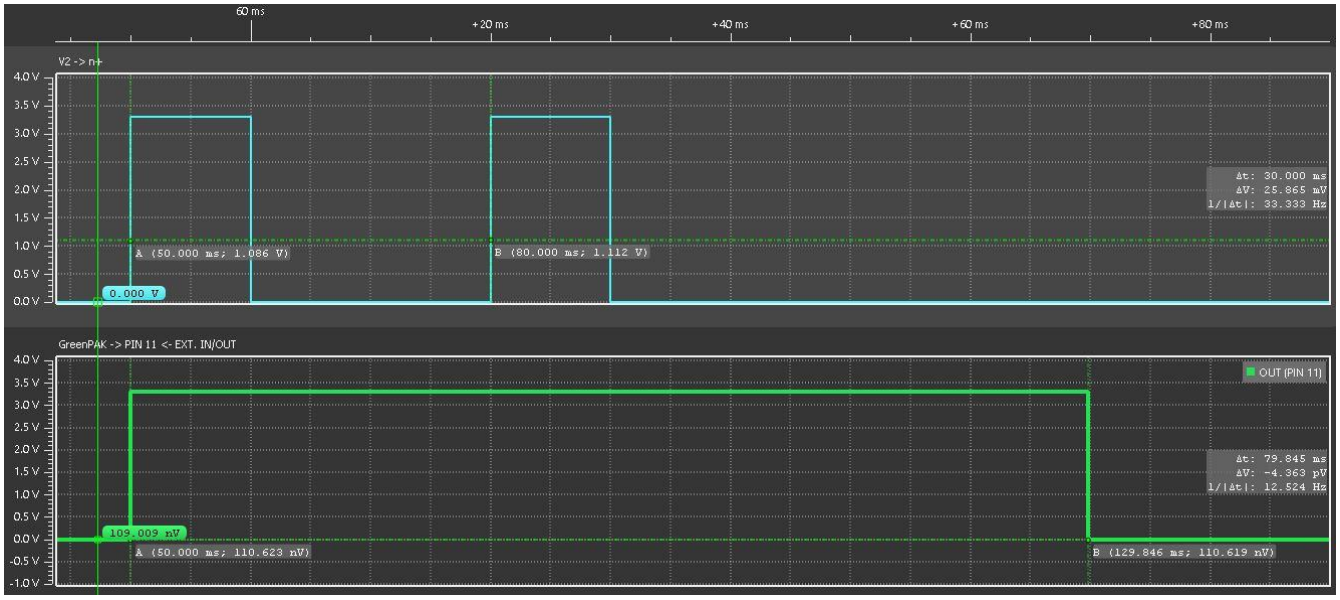

Figure 10. Pulse period is too short simulation case - Input signal is on top and, output signal is on bottom

4. Conclusion

In this application note the implementation of a pulse width stretcher using the GreenPAK device SLG46140 is discussed. The design does not require any additional components and can be easily modified to accomplish specific application requirements.

5. Revision History

Revision	Date	Description
1.00	4/20/2015	New application note (SLG46400)
2.00	09/23/2022	Application note review for another device (SLG46140).

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