

RL78 Family

R20AN0122EJ0102

Rev.1.02

Sound Playback/Compression System (Original ADPCM Codec)

Oct 01, 2015

M3S-S2-Tiny: Introduction Guide

Introduction

This document explains M3S-S2-Tiny for the RL78 Family V.3.04 Release 00 (hereafter referred to as "S2 library").

The S2 library for the Renesas Microcomputer is written in optimized assembler.

Please refer to the User's Manual to understand how to use the software library. User's Manual is in this application note.

And, we prepared Sound Playback/Compression demonstration software for the [YRDKRL78G14](#) as sample application program for S2 library.

Please refer to the following URL for details.

http://www.renesas.com/products/tools/middleware_and_drivers/tiny_soft/adpcm/m3s_s2_tiny/app_notes.jsp

(Document No.: R20AN0194)

Target Device

RL78 Family

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1. Structure of M3S-S2-Tiny

Table 1 S2 library product files

name	Description
r20an0122ej0102_rl78_s2.pdf	Introduction Guide (this document)
workspace	
Document(doc)	
English(en)	
r20uw0079ej0100_s2.pdf	S2 library User's Manual
r20an0122ej0102_rl78_s2.pdf	Introduction Guide (this document)
r21an0002ej0100_adpcm_tool.pdf	ADPCM_TOOL Instruction Manual
Japanese(ja)	
r20uw0079jj0100_s2.pdf	S2 library User's Manual
r20an0122jj0102_rl78_s2.pdf	Introduction Guide
r21an0002jj0100_adpcm_tool.pdf	ADPCM_TOOL Instruction Manual
IAR (IAR)	
Library(lib)	
adpcm_decoder_rl78.s87	S2 library for RL78 Family assembler tuning ver.
adpcm_encoder_rl78.s87	Library source file
adpcm_table_rl78.s87	
r_s2_version.c	S2 common source file
r_adpcm.h	S2 library header file
r_stdint.h	
r_mw_version.h	
CS+ for CA, CX (CS+ for CA)	
Library(lib)	
adpcm_decoder_rl78.asm	S2 library for RL78 Family assembler tuning ver.
adpcm_encoder_rl78.asm	Library source file
adpcm_table_rl78.asm	
r_s2_version.c	S2 common source file
r_adpcm.h	S2 library header file
r_stdint.h	
r_mw_version.h	
CS+ for CC (CS+ for CC)	
Library(lib)	
adpcm_decoder_rl78_ccrl.asm	S2 library for RL78 Family assembler tuning ver.
adpcm_encoder_rl78_ccrl.asm	Library source file
adpcm_table_rl78_ccrl.asm	
r_s2_version.c	S2 common source file
r_adpcm.h	S2 library header file
r_stdint.h	
r_mw_version.h	
Tool(tool)	
ADPCM_TOOL	ADPCM Convert program for Windows PC

2. Library specification

Library specification can be seen in user's manual included in installer. Installer can be downloaded in Renesas Electronics Web site.

3. For CS+ for CA, CX

3.1 Development Environment

Please use the same or a later version of the toolchain listed below:

[Software]

-Integrated Development Environment

CS+ for CA,CX V3.00.01

-C compiler

CA78K0R V1.71

-Code Generator tool

CS+ for CA,CX Code Generator for RL78 V2.07

3.2 S2 Library ROM / RAM / stack size

[ROM/RAM size]

— S2 library for the RL78 Family assembler tuning version.

ROM : about 900 byte

RAM : 0 byte (Upper layer program needs about 30byte for work area.)

Stack size : 20 byte

3.3 Notes

- Please specify the "near" symbol to pointer argument in all memory models.

4. For CS+ for CC

4.1 Development Environment

Please use the same or a later version of the toolchain listed below:

[Software]

-Integrated Development Environment

CS+ for CC V3.01.00

-C compiler

CC-RL V1.01

-Code Generator tool

CS+ for CC Code Generator for RL78 V2.07

4.2 S2 Library ROM / RAM / stack size

[ROM/RAM size]

— S2 library for the RL78 Family assembler tuning version.

ROM : about 900 byte

RAM : 0 byte (Upper layer program needs about 30byte for work area.)

Stack size : 22 byte

4.3 Notes

- Please specify the "near" symbol to pointer argument in all memory models.

5. For IAR Embedded Workbench

5.1 Development Environment

Please use the same or a later version of the toolchain listed below:

[Software]

-Integrated Development Environment and C compiler

IAR Embedded Workbench for Renesas RL78 version 2.10.1

-Code Generator tool

Applilet3 for RL78 V1.09.00

[board]

The sample program that uses S2-IAR version is in the following Application note.

Document title: Sound Playback/Record demonstration software for RL78/G14 CPU board

(Document number: R20AN0194)

Please download the sample code clicking following URL.

http://www.renesas.com/products/tools/middleware_and_drivers/tiny_soft/adpcm/m3s_s2_tiny/app_notes.jsp

5.2 S2 Library ROM / RAM / stack size

[ROM/RAM size]

— S2 library for the RL78 Family assembler tuning version.

ROM : about 900 byte

RAM : 0 byte (Upper layer program needs about 30byte for work area.)

Stack size : 22 byte

5.3 Notes

5.3.1 For about argument of pointer

Please specify the "near" symbol to pointer argument in all memory models.

5.3.2 For about tentative measure for IAR compile bug

The compiler used in the development setting in this library is reported some bugs from IAR.

Please refer to the following IAR website that shows details.

IAR systems : New versions and product updates

<https://www.iar.com/iar-embedded-workbench/renesas/r178/product-news/>

And, Renesas issues technical update for about IAR compiler.

Renesas : IDEs and Project Managers

http://www.renesas.com/products/tools/ide/Technical_Update.jsp

Document title : Operating Precautions IAR Embedded Workbench for RL78 V2.xx

Document No. : R20UT3407

This library is applied tentative measure for this issue.

· Some instructions that have one operand of type imm[BC] can in some cases generate wrong offsets to BC if the offset is a constant (not a label). [EW25763]

This tentative measure has effective for user used compiler version.

- User uses V2.10.1
Needed tentative measure. Please use this library in "no change".
- User uses version other than the above
There is a possibility that a compiler is fixed.
Not needed tentative measure. Please delete the tentative measure code.
Please update library code like following.

adpcm_encoder_rl78.s87 :line 131-162

```
_R_adpcm_initEnc:

    push bc
    push de

    movw bc, ax
    clrwx

;    movw    0800H[bc], ax        ;Source code for IARRL78 V2.10.1
    movw    0008H[bc], ax        ;Source code for IARRL78 V2.1x or Later
versions

;    mov     a, #2    ;Source code for IARRL78 V2.10.1
;    mov     0A00H[bc], a    ;Source code for IARRL78 V2.10.1
    mov     000AH[bc], #2    ;Source code for IARRL78 V2.1x or Later versions

    movw ax, #2*2
    addw ax, #LWRD(adpcm_stepsizeTable)
    movw de, ax
    movw ax, [de]
;    movw    0C00H[bc], ax        ;Source code for IARRL78 V2.10.1
    movw    000CH[bc], ax        ;Source code for IARRL78 V2.1x or Later
versions

    pop de
    pop bc

    ret
```

6. Library version information

Ver	change
3.04	Supported CS+ for CC.
3.01	Supported IAR Embedded Workbench.
3.00	first release

Website and Support

Renesas Electronics Website

<http://www.renesas.com/>

Inquiries

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Revision History

Rev.	Date	Description	
		Page	Summary
1.02	Oct.01.2015	—	Changed CubeSuite+ to CS+ for CA,CX Supported CS+ for CC. Deleted sample program.
1.01	Sep.01.2014	—	Release with V.3.01 Release 00
1.00	Nov.25.2011	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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