Date: May 30, 2018

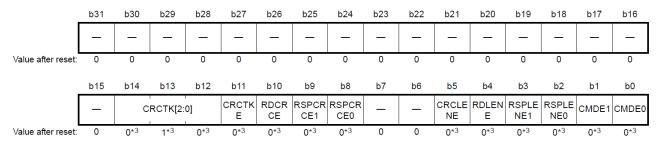# RENESAS TECHNICAL UPDATE

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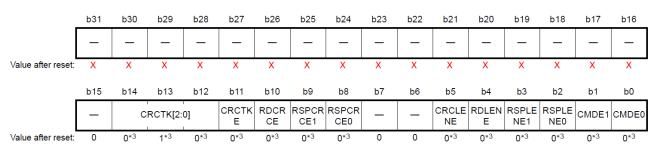| Product Category	MPU/MCU		Document No.	TN-SY*-A032A/E	Rev.	1.00
Title	Revised information about the reserved bit of the SD_ERR_STS1 register in SDHI		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7G2, S5D9, S5D5, S3A7, and S3A3 MCU Groups	Lot No.	Reference Document	S7G2 Rev.1.30 (R01UM0001EU0130), S5D9 Rev.1.10 (R01UM0004EU0110), S5D5 Rev.1.10 (R01UM0009EU0110), S3A7 Rev.1.30 (R01UM0002EU0130), S3A3 Rev.1.10 (R01UM0006EU0110)		
		All lots				

Description for the reserved bit of the SD_ERR_STS1 register in SD/MMC Host Interface (SDHI) will be updated in the next revision of the affected User's Manual.

1. SD/MMC Host Interface (SDHI), n.2.17 SD Error Status Register 1 (SD_ERR_STS1)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CRCTK[2:0]			CRCTKE	RDCRCE	RSPCRCE1	RSPCRCE0	—	—	CRCLENE	RDLENE	RSPLENE1	RSPLENE0	CMDE1	CMDE0
Value after reset:	0	0^{*3}	1^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0	0	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}

Bit	Symbol	Bit name	Description	R/W
b31 to b15	—	Reserved	These bits are read as 0.	R

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CRCTK[2:0]			CRCTKE	RDCRCE	RSPCRCE1	RSPCRCE0	—	—	CRCLENE	RDLENE	RSPLENE1	RSPLENE0	CMDE1	CMDE0
Value after reset:	0	0^{*3}	1^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0	0	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}	0^{*3}

Bit	Symbol	Bit name	Description	R/W
b15	—	Reserved	This bit is read as 0.	R
b31 to b16	—	Reserved	These bits are read as undefined.	R

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