Summary
This document describes how to use the normal transfer mode of the data transfer controller (DTC) to transfer A/D conversion results to the conversion result storage area located in RAM.

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1. **Overview of DTC Operation**

When a DTC activation request is generated, the DTC control data is loaded into the DTC module based on the address read from the DTC vector table entry assigned to the activation source. The transfer counter, transfer source address, and transfer destination address are updated and written back to the DTC control data area. After the writing of data finishes, control data (transfer counter, transfer source address, and transfer destination address) are updated and written back.

1.1 **Normal Mode and Repeat Mode**

DTC transfer has two modes: normal mode and repeat mode.

1.1.1 **Normal Mode**

In normal mode 1 to 256 bytes of data are transferred for each activation when 8-bit transfer is used, and 2 to 512 bytes of data are transferred when 16-bit transfer is used. The transfer count can be set to any value between 1 and 256. Data is transferred and the transfer count is decremented each time the activation source is generated until the specified transfer count reaches 0. When the transfer count value is 0, DTC transfer activation is disabled, and after the data transfer ends a DTC transfer-end interrupt is generated.

1.1.2 **Repeat Mode**

In repeat mode 1 to 255 bytes of data are transferred for each activation. The transfer count can be set to any value between 1 and 255. Data is transferred and the transfer count is decremented each time the activation source is generated until the specified transfer count reaches 0. The transfer counter and repeat area address are initialized, and the transfer operation is repeated. If interrupt generation is enabled, a DTC transfer-end interrupt is generated after completion of the transfer that brings the transfer count to 0.
Figure 1.1 is a flowchart of DTC transfer internal operation in normal mode and repeat mode.

Note 1. 1 is added for 8-bit transfers and 2 is added for 16-bit transfers.

Remarks:  

\[ i = 0 \text{ to } 5, \quad j = 0 \text{ to } 23 \]
DTC Usage Example (Normal Transfer): A/D Converter

From Figure 1.1 Flowchart of DTC Transfer Internal Operation (1/2)

1

Interrupts enabled? (RPTINT = 1)

Yes

Read data from transfer source (RAM, SFR, or ROM)

Reads data from the address indicated in DTSARj (transfer source address).

Write data to transfer destination (RAM or SFR)

Writes to the address indicated in DTDARj (transfer destination address).

Update transfer counter, transfer source address, and transfer destination address

Transfers the value in the DTRLDj (transfer count reload register) to DTCCTj, initializes the transfer count, and initializes the transfer source or transfer destination address selected as the repeat area (writes 00H to the lower 8 bits in DTSARj or DTDARj).

Write-back DTC control data

Writes back DTC module register information to the transfer source control data area (RAM).

The peripheral function interrupt selected as the DTC transfer activation source is generated.

No (RPTINT = 0)

Write 0 (activation disabled) to the bit in DTCENi register corresponding to the DTC activation source

Disables DTC transfer activation.

Read data from transfer source (RAM, SFR, or ROM)

Reads data from the address indicated in DTSARj (transfer source address).

Write data to transfer destination (RAM or SFR)

 Writes to the address indicated in DTDARj (transfer destination address).

Update transfer counter, transfer source address, and transfer destination address

Transfers the value in the DTRLDj (transfer count reload register) to DTCCTj, initializes the transfer count, and initializes the transfer source or transfer destination address selected as the repeat area (writes 00H to the lower 8 bits in DTSARj or DTDARj).

Write-back DTC control data

Writes back DTC module register information to the transfer source control data area (RAM).

Remarks:  \( i = 0 \) to 5, \( j = 0 \) to 23

To Figure 1.1 Flowchart of DTC Transfer Internal Operation (1/2)

Figure 1.1 Flowchart of DTC Transfer Internal Operation (2/2)
2. Specifications

A usage example combining the DTC, A/D converter, and timer array unit (TAU) channel 0 (TAU00) and channel 1 (TAU01) is presented below.

TAU00 (2 ms) and TAU01 (1 ms) count in coordinated fashion, and the A/D converter uses the TAU01 interrupt request signal as the trigger to start A/D conversion. The DTC uses A/D conversion end as the DTC activation source and stores the A/D conversion result in RAM. Thereafter the processing is repeated.

Figure 2.1 is a connection diagram showing the pins used, Table 2.1 lists the peripheral functions used and their applications, Figure 2.2 is a configuration diagram of the peripheral functions used, and Figure 2.3 shows the DTC transfer timing.

In the application described in this document AVREFP, AVREFM, ANI2, ANI3, ANI4, and ANI5 are used.

**Figure 2.1 Connection Diagram of Pins Used**
Table 2.1 Peripheral Functions Used and Their Applications

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Application</th>
</tr>
</thead>
</table>
| DTC | Transfers the A/D conversion results to RAM at A/D conversion end.  
- DTC activation source: A/D conversion end  
- Transfer source address: ADCR register  
- Transfer destination address: RAM  
- Transfer count: 4  
- Operating mode: Repeat mode  |
| A/D converter | Performs A/D conversion on the analog input signals from pins ANI2 to ANI5.  
- 10-bit resolution  
- Hardware trigger no-wait mode (source: INTTM01 signal)  
- Scan mode (4-pin)  
- One-shot conversion mode  |
| TAU00 | Constant-period timer  
- Internal timer mode (2 ms)  
- Used as master channel.  |
| TAU01 | Generates A/D conversion trigger (INTTM01 signal).  
- One-count mode (1 ms)  
- Used as slave channel.  |

![Figure 2.2 Configuration Diagram of Peripheral Functions Used](image)

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### Notes
- **Figure 2.2** shows the configuration diagram of the peripheral functions used in the DTC usage example. The diagram illustrates the connection between the A/D converter, DTC, ADCR register, and RAM, along with the trigger signals from INTTM00 and INTTM01. The diagram also highlights the transfer-end interrupt at DTC transfer-end.
Notes: TCR00: Timer counter register 00
- INTTM00 signal: TAU00 count-end/capture-end interrupt request signal
- TCR01: Timer counter register 01
- INTTM01 signal: TAU01 count-end/capture-end interrupt request signal
  (Used as A/D conversion-start trigger.)
- ADCR: 10-bit A/D conversion result register
- DTC activation request: A/D conversion end interrupt signals for each pin
- FFB00H to FFB07H: RAM area (conversion result storage area) indicated by DTDAR0
  (DTC transfer destination address in DTC control data area)
- DTCCO: DTC transfer count register 0 in DTC control data area
- ADIF: A/D conversion end interrupt flag
- DTCCN16: DTCCN16 bit in DTCCN1 register
  The TAU count clock is CK02 (8 MHz).

Figure 2.3 DTC Transfer Timing
3. Setting Procedures of Peripheral Functions

The setting procedures of the peripheral functions (DTC, A/D converter, TAU00, and TAU01) are described in this section.

3.1 Peripheral Function Initialization Procedure

Initialization of the peripheral functions (DTC, A/D converter, TAU00, and TAU01) is described below. Figure 3.1 shows the peripheral function initialization procedure.

Start
DI (disable interrupts)
Initialize DTC
Initialize A/D converter
Initialize TAU00 and TAU01
EI (enable interrupts)
End

See 3.2, DTC Setting Procedure
See 3.3, A/D Converter Setting Procedure
See 3.4, TAU00 and TAU01 Setting Procedure

Figure 3.1 Peripheral Function Initialization Procedure
## 3.2 DTC Setting Procedure

The DTC transfers the A/D conversion results to the conversion result storage area in RAM, using the end of A/D conversion as the activation source.

Figure 3.2 shows the DTC initialization procedure.

### Figure 3.2 DTC Initialization Procedure

<table>
<thead>
<tr>
<th>Start</th>
<th>DTC control data area in the RAM</th>
<th>DTC vector table area and DTC control data area in the RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initialize FFD00H to FFDFFH</td>
<td>FFDFFH</td>
<td>FFDFFH</td>
</tr>
<tr>
<td>PER1.DTCEN = 1</td>
<td>FFD48H</td>
<td>FFD48H</td>
</tr>
<tr>
<td>DTCENi = 00H (i = 0 to 5)</td>
<td>FFD47H</td>
<td>FFD47H</td>
</tr>
<tr>
<td>DTCBAR = FDH</td>
<td>FFD46H</td>
<td>FFD46H</td>
</tr>
<tr>
<td>Address FFD09H = 40H</td>
<td>FFD45H</td>
<td>FFD45H</td>
</tr>
<tr>
<td>DTCCT0 (FFD42H) = 01H</td>
<td>FFD44H</td>
<td>FFD44H</td>
</tr>
<tr>
<td>DTBLSD (FFD43H) = 04H</td>
<td>FFD43H</td>
<td>FFD43H</td>
</tr>
<tr>
<td>DTSAR0 (FFD44H) = FF1EH</td>
<td>FFD42H</td>
<td>FFD42H</td>
</tr>
<tr>
<td>DTDAR0 (FFD46H) = FFB00H</td>
<td>FFD41H</td>
<td>FFD41H</td>
</tr>
<tr>
<td>DTDAR1 (FFD48H) = FB00H</td>
<td>FFD40H</td>
<td>FFD40H</td>
</tr>
<tr>
<td>Reserved area</td>
<td>FFB40H</td>
<td>FFB40H</td>
</tr>
<tr>
<td></td>
<td>FFB2EH</td>
<td>FFB2EH</td>
</tr>
<tr>
<td></td>
<td>FFD09H</td>
<td>FFD09H</td>
</tr>
<tr>
<td></td>
<td>FFD00H</td>
<td>FFD00H</td>
</tr>
</tbody>
</table>

- Sets the DTC base address. (FFD00H)
- DTC vector address : FFD00H
- DTC control data area start address : FFD40H
- Sets the start address of DTC control data 0 in DTC vector table source number [9] (A/D conversion end).
- Lower byte of DTC control data 0 address (FFD40H) is stored.
- Makes setting to DTC control register 0.
- 16-bit, repeat transfer, repeat mode interrupt generation enabled
- Sets the DTC transfer size (2-byte).
- Sets the DTC transfer count (4 times).
- Sets the transfer source address.
- (Lower two bytes of ADCR register address (FFF1EH) are stored.)
- Sets the transfer destination address.
- (Lower two bytes of RAM address (FFB00H) are stored.)

<table>
<thead>
<tr>
<th>DTC control data area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower two bytes of RAM address</td>
</tr>
<tr>
<td>Lower two bytes of ADCR register address</td>
</tr>
<tr>
<td>16-bit selected as data size</td>
</tr>
<tr>
<td>(Lowest 6 bits of RAM address)</td>
</tr>
<tr>
<td>(Lowest 6 bits of ADCR register address)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DTC vector table area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower two bytes of RAM address</td>
</tr>
<tr>
<td>Lower two bytes of ADCR register address</td>
</tr>
<tr>
<td>16-bit selected as source number</td>
</tr>
<tr>
<td>(Lowest 6 bits of RAM address)</td>
</tr>
<tr>
<td>(Lowest 6 bits of ADCR register address)</td>
</tr>
</tbody>
</table>

- DTC control data 0 set as source number [9] (A/D conversion end)
3.3 A/D Converter Setting Procedure

The following settings are used to perform A/D conversion of the analog input signals on pins ANI2 to ANI5. Figure 3.3 shows the initialization procedure for the A/D converter.

Start

PER0.ADCEN = 1

Supplies the input clock to the A/D converter.

ADPC = 07H

Analog input port settings

Sets the upper and lower limit values for the conversion results

PM3.PM3[4:3] = 11B
PM8.PM8[3:0] = 1111B

Sets analog input pins to input mode.

ADM0 = 70H

A/D converter operating mode settings (ADM0 register)

ADCS : 0B (A/D converter operation stop selected)
ADMD : 1B (scan mode selected as conversion channel selection mode)
FR[2:0] : 110B (t осн/4 selected as conversion clock)
LV[1:0] : 00B (normal 1 selected as conversion mode)
ADCE : 0B (A/D comparator operation stop selected)

ADM1 = A0H

A/D converter operating mode settings (ADM1 register)

ADTMD[1:0] : 10B (hardware trigger no-wait mode selected)
ADSCM : 1B (one-shot conversion mode selected)
ADTRS[1:0] : 00B (TAU01 selected as hardware trigger)

ADM2 = 60H

A/D converter operating mode settings (ADM2 register)

ADREFP[1:0] : 01B (AVREFP selected as + side reference voltage source)
ADREFM : 1B (AVREFM selected as - side reference voltage source)
ADRCK : 0B (generation of interrupt signal (INTAD) when ADLL register ≤ ADCR register ≤ ADUL register when checking conversion results selected)
AWC : 0B (SNOOZE mode function not used)
ADTYP : 0B (10-bit selected as A/D conversion resolution)

ADUL = FFH
ADLL = 00H

Sets the upper and lower limit values for the conversion results.

ADS = 02H

Analog input channel settings

ADISS: 0B, ADS[4:0]: 00010B (scan 0 (ANI2) to scan 3 (ANI5))

A/D stabilization wait time A (5 µs)

Wait for stabilization (5 µs) when changing ADM2.ADREFP[1:0] to 10B (+ side reference voltage source supplied from internal reference voltage (1.45 V)).

ADM0.ADCE = 1

Enables A/D voltage comparator operation.

A/D stabilization wait time B (1 µs)

After setting the ADCE bit to 1, it is necessary to wait for stabilization (1 µs) before setting the ADM0.ADCS bit to 1 (A/D converter operation enabled).

PR11H.ADPR1 = 0
PR01H.ADPR0 = 1

A/D conversion end interrupt priority setting

01B (level 1)

MK1H.ADMK = 0

Enables the A/D conversion end interrupt handler.

IF1H.ADIF = 0

Clears the A/D conversion end interrupt request signal.

End

Figure 3.3 A/D Converter initialization Procedure
3.4 TAU00 and TAU01 Setting Procedure

The timer array unit (TAU) is used as a PWM function. TAU00 is set as the master channel and TAU01 as the slave channel, and a PWM signal is generated with a period of 2 ms and 50% duty. Note that PWM waveforms are not used in this example.

Figure 3.4 shows the initialization procedure for TAU00 and TAU01.

![Figure 3.4 TAU00 and TAU01 Initialization Procedure](image-url)

Start

Supplies the input clock to the TAU0.

**TAU0 timer clock selections**

- CK00: fCLK
- CK01: fCLK/2
- CK02: fCLK/4
- CK03: fCLK/8

**TAU0 timer operating mode settings**

- CKS00[1:0]: 01B (CK02 selected as fMCK)
- CCS00: 0B (fMCK selected as count clock (fTCLK))
- STS00[2:0]: 000B (software trigger selected as start trigger)
- CIS00[1:0]: 00B (falling edge selected as valid edge of T100 pin signal)
- MD00[3:1]: 000B (interval timer mode selected)
- MD00: 0B (interrupt not generated at count start)

**TAU01 timer operating mode settings**

- CKS01[1:0]: 01B (CK02 selected as fMCK)
- CCS01: 0B (fMCK selected as count clock (fTCLK))
- SPLIT01: 0B (16-bit timer, operates as slave channel)
- STS01[2:0]: 100B (master channel interrupt signal used as start trigger)
- CIS01[1:0]: 00B (falling edge selected as valid edge of T101 pin signal)
- MD01[3:1]: 100B (one-count mode selected)
- MD01: 1B (start trigger enabled and interrupts generated during count operation)

Selects the TAU00 and TAU01 timer inputs (initial value).

Disables TAU00 and TAU01 timer output.

Sets the TAU00 count value (2 ms).

Sets the TAU01 count value (1 ms).

**TAU00 interrupt priority setting**

10B (level 2)

Enables the TAU00 interrupt handler.

Clears the TAU00 interrupt request signal.

Disables the TAU01 interrupt handler.
3.5 Procedure for Enabling Peripheral Functions (DTC Transfer Start)

After initializing the peripheral functions (DTC, A/D converter, TAU00, and TAU01), the operation is enabled (started). Figure 3.5 shows the procedure for enabling the operation of the peripheral functions (DTC transfer start).

![Diagram]

**Figure 3.5 Procedure for Enabling Peripheral Functions (DTC Transfer Start)**

3.6 DTC Transfer-End Interrupt Handler

It is possible to generate an interrupt corresponding to the end of a DTC transfer (the A/D conversion end interrupt in the example described in this document).

Figure 3.6 shows the DTC transfer-end interrupt (A/D conversion end interrupt) handler.

The contents of the upper 10 bits (b15 to b6) of the A/D conversion results stored in memory after the DTC transfer are shifted to the lower 10 bits (b9 to b0). Then, DTC transfer operation is re-enabled.

![Diagram]

**Figure 3.6 DTC Transfer-End Interrupt (A/D Conversion End Interrupt) Handler**
4. Important Points

4.1 DTC Transfer Cycle Count

When using the DTC under the specifications indicated in the usage example presented in this document, the DTC transfer cycle count is nine clock cycles per transfer. See Table 4.1 for details.

Table 4.1 DTC Transfer Clock Cycle Count (Transfer Source: A/DCR Register, Transfer Destination: RAM, Repeat Mode)

<table>
<thead>
<tr>
<th>Vector Read</th>
<th>Control Data</th>
<th>Data Read</th>
<th>Data Write</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Read</td>
<td>Write-Back</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>9</td>
</tr>
</tbody>
</table>

Note: See Table 4.2 for the control data write-back clock cycle count, Table 4.3 for the data read clock cycle count, and Table 4.4 for the data write clock cycle count. The settings used in the example presented in this document are indicated in Table 4.2 to Table 4.4 by the white unshaded cells.

Table 4.2 Clock Cycle Count Necessary for DTC Control Data Write-Back

<table>
<thead>
<tr>
<th>DAMOD</th>
<th>SAMOD</th>
<th>RPTSEL</th>
<th>MODE</th>
<th>Transfer Source</th>
<th>Transfer Destination</th>
<th>DTCTj</th>
<th>DTRLDj</th>
<th>DTSARj</th>
<th>DTDARj</th>
<th>Clock Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Write-back</td>
<td>Write-back</td>
<td>—</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>0</td>
<td>Incremented</td>
<td>Fixed</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>—</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>Fixed</td>
<td>Incremented</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>—</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>0</td>
<td>Incremented</td>
<td>Incremented</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>3</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>Repeat</td>
<td>Fixed</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>—</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>Repeat</td>
<td>Incremented</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>3</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Fixed</td>
<td>Repeat</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>—</td>
<td>2</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Incremented</td>
<td>Repeat</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>Write-back</td>
<td>3</td>
</tr>
</tbody>
</table>

Note: X: 0 or 1, ——: no write-back, j = 0 to 23

Table 4.3 DTC Data Read Clock Cycle Count

<table>
<thead>
<tr>
<th>RAM</th>
<th>Flash Memory</th>
<th>SFR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Code Flash</td>
<td>Data Flash</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

Note: A wait (1 clock cycle) is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

Table 4.4 DTC Data Write Clock Cycle Count

<table>
<thead>
<tr>
<th>RAM</th>
<th>Flash Memory</th>
<th>SFR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Code Flash</td>
<td>Data Flash</td>
</tr>
<tr>
<td>1</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Note: A wait (1 clock cycle) is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.
4.2 DTC Usage Notes

- Do not use a DTC transfer to access DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCTm, HDTRLDm, HTSARm, and HTDARm) or the DTC control data area, DTC vector table area, or the general-register (FEE0H-FEFFH) space in RAM. Also, when using self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function, do not access the memory areas associated with those functions.

- Write to or change the DTCENi register only when the interrupt sources for which the DTC activation is enabled in the target register, and the interrupt sources set as activation-enabled will not be generated.

- Do not use the memory areas associated with the general-register (FEE0H-FEFFH) space, self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function as the DTC control data area or DTC vector table area.

- Only make changes to the DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCTm, HDTRLDm, HTSARm, and HTDARm), the registers assigned to the DTC control data area (DTCCRj, DTBLj, DTCTj, DTRLDj, DTSARj, and DTDARj), and the DTC vector table area when all DTC activation sources are set as activation-disabled (corresponding bits in DTCENi register cleared to 0).

- Make initial settings (write random values) to the DTC control data area and DTC vector table area in the RAM. The DTC vector table area (64 bytes including reserved areas) must not be used as general-purpose RAM by user programs. Note that portions of the DTC control data area (192 bytes) that are not used by the DTC can be used as general-purpose RAM.

- Do not overwrite DTCBAR more than once.

- When a DTC transfer-pending instruction (call or return instruction, unconditional or conditional branch instruction, instruction for accessing code flash memory, instruction for accessing interrupt-related registers (IFxx, MKxx, and PRxx) or PSW, instruction for accessing the data flash, or multiply, divide, or multiply-and-accumulate instruction except for the MULU instruction) is executed, the DTC transfer does not take place and the request is put on hold. Also, no DTC transfer takes place during a PREFIX instruction and for a period equal to one instruction immediately following it.

- If a data flash access instruction is executed during the period equal to one instruction after the activation of a DTC data transfer, a wait of three clock cycles occurs due to the specifications of the internal bus.

- The DTC transfer is put on hold when an access is made to an SFR requiring a wait (CAN or LIN register, or the TRJ0 register of timer RJ).

- From the point at which a DTC activation source is generated until the point at which the DTC transfer completes, the same activation source should not be generated again.

- If there is a conflict between DTC activation sources, the priorities of the activation sources are considered. The source with the higher priority (based on the source number) takes effect, and the source with the lower priority is put on hold.

- In repeat mode, the lower byte of the address (setting value) of the repeat area must have a value of 00H. Also note that the transfer count and reload transfer count will differ according to the transfer data size.
  - 8-bit transfer: 01H to FFH (1 to 255 times)
  - 16-bit transfer: 01H to 7FH (1 to 127 times)
Website and Support

Renesas Electronics Website
http://www.renesas.com/

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