Optimizing Sensor Modules: Why AnalogPAK SLG47011 Excels as the Ideal Sensor Controller

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Abstract

This white paper is written to emphasize the crucial role of sensors in the current market as well as highlight the requirements and challenges of sensor device designs. In this paper, we explain the structure of SLG47011 and why its blocks are a perfect choice for sensor solutions. Besides the theory, the author presents real-life examples of diverse sensor applications. Additionally, you can find in this paper the basic principles of sensor connections and signal processing.

Contents

Terms and Definitions

ADC	Analog-to-Digital Converter
CH	Channel
CNT	Counter
DAC	Digital-to-Analog Converter
DCMP	Digital Comparator
DFF	D Flip-Flop
DLY	Delay
IC	Integrated Circuit
IN	Input
LUT	Look-up Table
MathCore	Mathematical Core
PGA	Programmable Gain Amplifier

Introduction

Sensors are electronic devices that produce an output signal they read from the environment. They allow the detection of a change in various environmental indexes such as temperature, pressure, light, sound, motion, and chemicals as well as converting them into electrical signals. These signals can then be used to measure, record, and monitor these phenomena.

Sensors are used in a wide range of industries; some examples are included below:

- Consumer electronics: smartphones, computers, TVs, air conditioners
- Automotive industry: ABS, airbags, parking sensors
- Medical equipment: electrocardiograms, devices for pressure measuring
- Industrial machines: process control, labor protection
- Agriculture: soil monitoring, irrigation
- Construction: smart buildings, security systems
- And many more

The sensor market is growing rapidly due to the expanding demand for sensors in vehicles, connected devices, the rising adoption of IoT, and many others. According to various market research reports, the sensor market size was valued at approximately USD 217.84 billion in 2023. It is expected to reach USD 422.7 billion by 2028, with a compound annual growth rate (CAGR) of around 22% from 2024 to 2028 (Technavio).

Designers of sensor devices face many challenges. ICs that are used to process signals from sensors must meet many requirements to satisfy the needs of the market. These requirements include:

- High performance: ASICs must be able to process signals from sensors in real time with low latency, high accuracy, and relevant safety protocols. This is important for applications such as process control and safety systems.
- Low power consumption: ICs should consume as little power as possible, especially when used in portable or battery-powered devices.
- Noise: ICs must be noise-resistant to provide clear signals. This is important for applications where sensors are exposed to harsh environmental conditions.
- Integration: ICs should be easily integrated with other electronic components. This is important to reduce the cost and complexity of the systems.
- Programmability: ICs must be programmable so that they can be used in a variety of applications and allow a high level of customization.
- Cost: ICs must be affordable so that they can be used in a wide range of devices.

The brand new Renesas AnalogPAK™ SLG47011 - provides a customizable and complex solution for sensor signal conditioner applications, that allows to meet all the requirements described above.

This white paper will show the SLG47011 internal structure and how it fits the sensor applications. Moreover, real-life application examples with a Wheatstone bridge pressure sensor, a thermocouple, a PT1000 sensor, an internal temperature sensor, and a PIR sensor will be given, along with the principles of each sensor connection and signal processing will be explained.

SLG47011: Capabilities for Sensor Solutions

The SLG47011 belongs to a new AnalogPAK sub-family of a wide family of GreenPAK™ Programmable Mixed-Signal Products with embedded high-performance analog blocks that can be configured and controlled by customer-defined logic functions to implement various scenarios. All macrocells are placed in one tiny package IC to achieve a high integration level of common analog and digital components at a low cost for your mixed-signal project. New flexible user-defined power-saving modes for all macrocells ensure better energy-saving. Moreover, the chip consumes only ~ 0.6 uA in sleep mode.

It is worth starting with the blocks that ensure high-quality reception of signals from sensors for their further processing – PGA and ADC. The highly configurable low offset Programmable Gain Amplifier (PGA) macrocell of the SLG47011 allows the selection of different amplifier modes and configurations that better suit input signal requirements.

The 14-bit successive approximation register Analog-to-Digital Converter (SAR ADC) macrocell provides a sampling rate of up to 1 Msps in 14-bit mode and 2.35 Msps in 8-bit mode. Differential or single-ended modes could be chosen depending on design needs. In addition to this, there is a possibility of adding an auto-calibration for better signal accuracy.

The SLG47011 has four versatile Data Buffers designed to store or process data from the ADC or CNT/DLY. It's possible to choose among Storage, Moving Average, or Oversampling modes as well as their length and initial data settings. These features let store data from ADC for further processing. Besides, the Averaging function can be used to filter out the noise by connecting the buffers in a daisy chain.

Let's switch to the memory possibilities of SLG47011. The Memory Table macrocell is a memory block that houses 4096 12-bit words with a 12-bit address and data port. Together with the MathCore, any kx+b efficient function may be implemented to eliminate offset and gain errors or just represent data in other suitable forms for further manipulations. This Mathematical Core block supports four mathematical operations: addition, subtraction, multiplication, division (right shift), and their combinations. Input sources for the MathCore can be ADC channels, Memory Table output, Data Buffer outputs, or constants from registers.

One more significant block that will help create a solution for the sensor is the Multichannel Digital Comparator macrocell with Hysteresis (DCMP). It compares up to four digital channels with synchronous or sequential result appearance.

To present the obtained results in analog form, the 12-bit Digital-to-Analog Converter (DAC) can be used. In addition to the blocks described above, there are also a PWM block, a Power Controller, a Width Converter, and a large set of logic (LUT, flip flops, Counters, Delays, and so on).

Let's see how to use all these described blocks to create a custom sensor solution.

Examples

1. Wheatstone Bridge Pressure Sensor

In this application, the SLG47011 is used as the Signal Conditioner for a Wheatstone Bridge Pressure Sensor with offset and gain error compensation over temperature. See the block diagram in Figure 1.

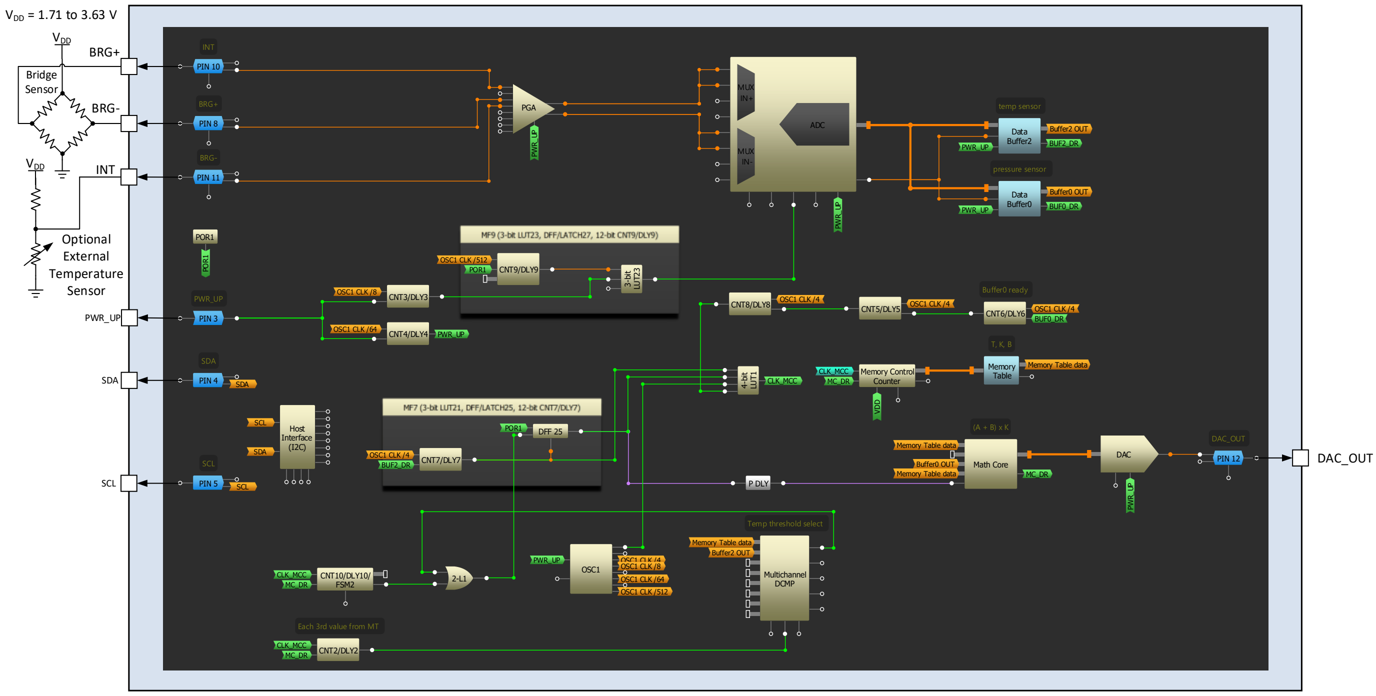

Figure 1. Wheatstone Bridge Pressure Sensor Block Diagram

In this application, it is necessary to compensate for the temperature impact on the gain error and offset errors, as they change with temperature. Thus, ten temperature thresholds from - 40 to 85 ̊C are considered. Consequently, there are ten values of temperature thresholds and ten corresponding values of K (gain error) and B (offset). After determining the coefficients, they are recorded in the Memory Table.

Signals from the Pressure Sensor BRG+ and BRG- come to PGA, the differential voltage on the sensor is measured and multiplied by 32, and then this signal goes to Channel 1 of the ADC. The output of the voltage resistive divider with a thermistor (NTC XH103 10 k) goes to the PGA (1x gain) and Channel 0 of the ADC.

During the sampling of the Channel 1 (pressure sensor), the corresponding temperature threshold is selected by comparing the data from Buffer 2 with temperature thresholds from the Memory Table by Multichannel DCMP. For each threshold T, there are corresponding gain error K and offset B* (B – corrected value) coefficients, which are selected as soon as the temperature threshold is found. Then this sampled data “A” (from the pressure sensor) is compensated in the Math Core, and the output is K x A + B*. In our case (A + B) x K, where B = B*/K. After the compensation, data goes to a 12-bit DAC which outputs analog voltage to the physical PIN (GPIO8) directly.

2. Thermocouple with Automatic Cold Junction Compensation

Using the SLG47011 IC it is possible to build a thermocouple ADC with integrated cold junction compensation. Thanks to its collection of internal macrocells, the device has all the required parts which eliminate any external components, see the block diagram in Figure 2.

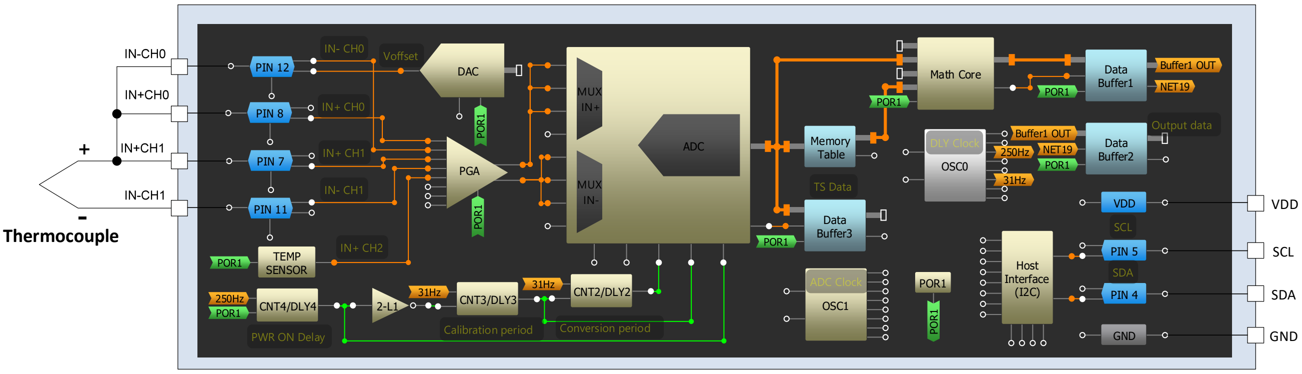

Figure 2. Automatic Cold Junction Compensation Block Diagram

The DAC macrocell provides a voltage of internal Vref/2 for the PGA in differential mode. Three of four PGA channels are used. Two channels 0 and 1 (PINs 8, 12, and 7, 11 respectively) are set to a Differential input Instrumentation amplifier mode with 32x gain. Channel 0 is used for calibration which reduces PGA offset and noise error. Channel 1 is used for thermocouple measurement.

Channel 2 is used to input the internal Temperature Sensor voltage for Cold Junction Compensation. It is set to Single-ended input with 1x gain. The temp sensor is inside the IC, so it must be placed close to the cold junction, ensuring that both temperatures are equal.

In this design, the Memory Table is set to ROM mode in which data from ADC channel 2 is converted to the Memory Table address. Output data of the Memory Table will be the contents of the pre-written addressed cell. MathCore is used to add data from the ADC channel 1 to data from the Memory Table (values from the thermocouple and TS, thus compensating the cold junction). The result of this mathematical operation goes through the averaging process (Data Buffers 1 and 2) and can be accessed via the I²C /SPI host interface.

The device is meant to operate at ambient temperature in the range of 0 to 80°C.

3. PT1000 Interface

The PT1000 sensor contains a pure platinum element that has a resistance of 1kΩ at 0°C. This resistance increases with increasing temperature.

Figure 3 shows the block diagram of the PT1000 Interface. The PT1000 sensor is connected in series with a 1kΩ ±0.1% resistor forming a resistive voltage divider. The voltage from the divider is supplied to Channel 0 and Channel 1 IN+ of the PGA and ADC. DAC Vref Buffer provides a voltage of $V_{DD}/2$ and goes to Channel 1 of PGA and ADC with 1x gain.

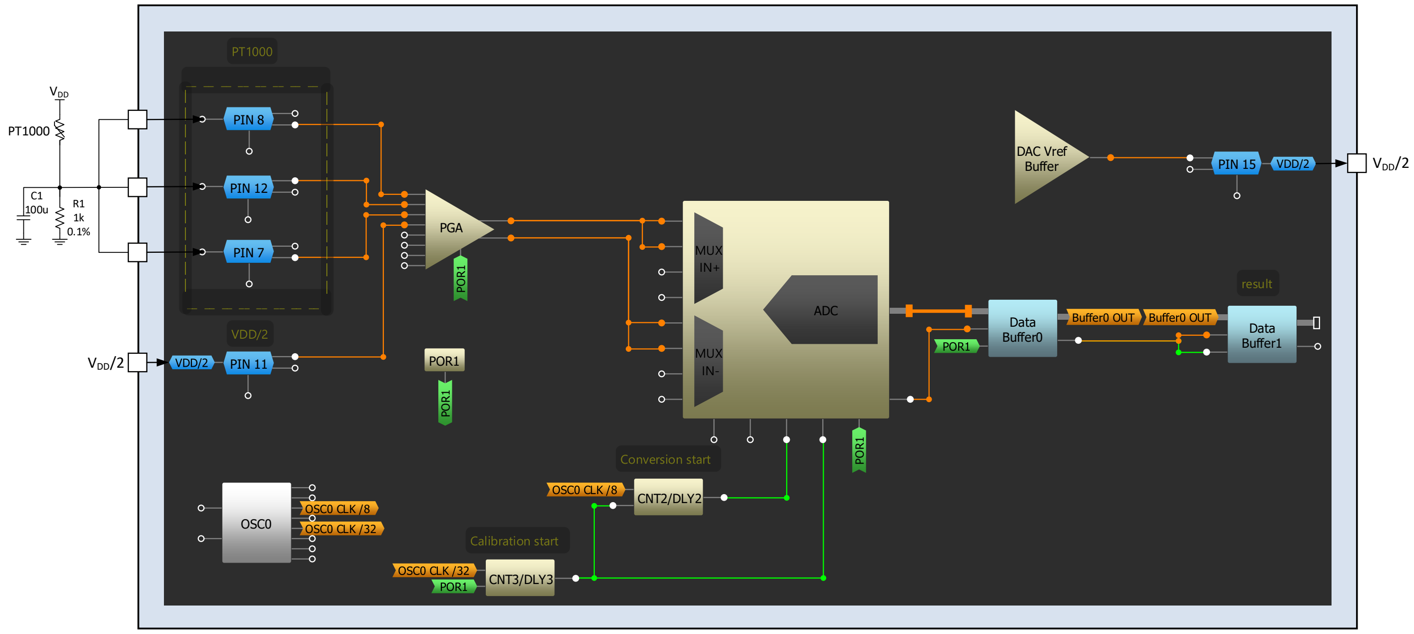

Figure 3. PT1000 Interface Block Diagram

Channel 0 is used for calibration which reduces PGA offset and noise error.

Channel 1 is used for temperature measurement. Since the resistance of the sensor changes with temperature, the measured voltage on the resistive divider also changes. Thus, the ADC output will be the difference between VDD/2 and voltage on the resistive divider.

The resistance versus temperature ratio for PT1000 sensors is standardized and this ratio can be used to convert the measured voltage to a temperature value.

4. Precision Internal Temperature Sensor

The internal Temperature Sensor is used to measure the temperature in this design. See the block diagram in Figure 4.

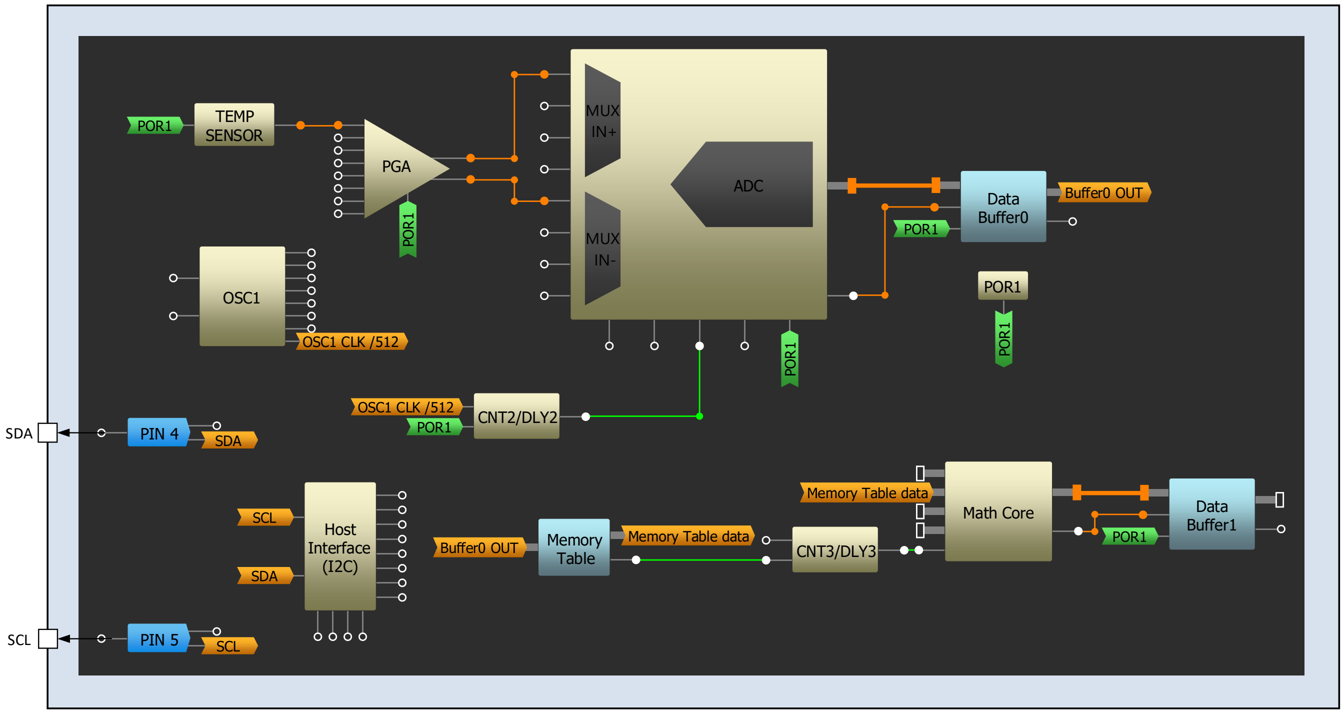

Figure 4. Internal Temperature Sensor Block Diagram

The Memory Table macrocell is filled with average voltage-temperature dependence converted to 12-bit format so that the word address corresponds to the appropriate temperature value.

The Temp Sensor is connected to IN+ CH0 of PGA which is configured as a single-ended input with 1x gain. ADC samples the measured value and sends its output to Data Buffer 0 in Moving Average mode for noise filter. Then, this data is used as an address of the Memory Table.

Thus, the temperature value is obtained and can be compensated in the MathCore. The MathCore formula is kx+b, where x is the temperature before compensation, k = 1, and b – is offset between the measured and ideal trimming temperatures. Please note that all values in the MathCore and Memory table are multiplied by 10 to be integers. Thus, the offset of 0.7 °C is equal to the coefficient b of 7 in the MathCore.

After compensation, the data goes to Data Buffer1 for the final noise-canceling stage.

4. Analog PIR Sensor Interface

The PIR Sensor is an electronic sensor that measures infrared (IR) light radiating from objects in its field of view. The block diagram in Figure 5 shows the working principle of Signal Conditioner for PIR Sensors.

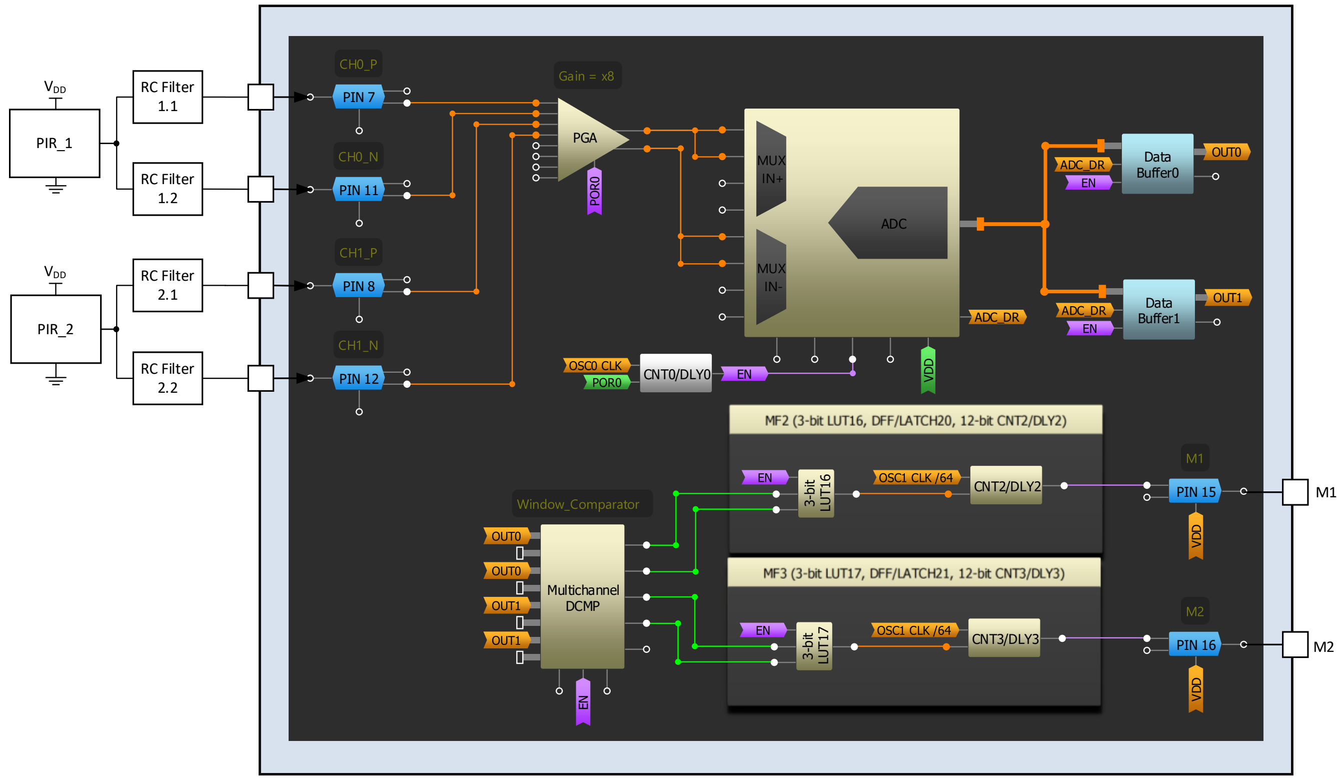

Figure 5. Signal Conditioner for PIR Sensors Block Diagram

SLG47011 allows the connection of two PIR sensors. The output of each sensor is connected to two RC filters, which are tuned to different frequencies - high and low filters. Signals from these filters are connected to the ADC differential channel (PGA bypass). Thus, the difference between both signals is measured and further filtered in the Buffer. Next, the signal from the Buffer is sent to two channels of the Multichannel DCMP. A static threshold is selected for each channel depending on the required sensitivity of the sensor - upper and lower. If the signal does not fit into the so-called no movement window - motion is detected. Then, this signal with additional internal logic is applied to the M1 output (M2 for the second sensor).

Conclusion

The use of SLG47011 elevates signal processing and data management sensor applications. Its resource variety allows multiform sensor connections - single-ended or differential - and internal calibration implementation. The SLG47011 part provides diverse signal manipulation options such as noise filtering by Buffer, signal comparing by DCMP, function implementation by Memory Table and MathCore, and many others.

By consolidating multiple functions onto a single chip, SLG47011 streamlines design, minimizes board size, cuts power consumption, and decreases component cost – all these factors are crucial for sensor applications.

The SLG47011 embodies efficiency and innovation, empowering sensor projects allowing them to reach new heights of performance and cost-effectiveness.

Revision History

Revision	Date	Description
1.00	11/6/2024	Initial release.