The Linux PTP Hardware Clock Subsystem for 5G O-RAN White Box Hardware

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Abstract

This whitepaper reviews the Linux PTP Hardware Clock (PHC) subsystem infrastructure and the uses of the PHC as an interface to both software-based and hardware-based servos that provide the Telecom synchronization interfaces required to meet ITU-T network limits for 5G Radio Access Network (RAN).

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Introduction

With the transition from time-division multiplexing (TDM) to packet switched networks (PSNs), the transport of time/synchronization over a packet network became a necessity. IEEE 1588 (IEEE Std 1588™-2019[0]), also known as Precision Time Protocol (PTP), is becoming the main protocol to transport precision time, phase, and frequency over packet networks. IEEE 1588 defines a protocol to distribute synchronization over packet networks; it is a precise protocol with features and options that address a wide range of applications.

5G Radio Access Network (RAN) requires a new approach to designing and building networks. Work by organizations like the O-RAN Alliance and Telecom Infra Project (TIP) is now resulting in specifications for white box implementations that can address the performance requirements of 5G RAN. One area being looked at is network synchronization for frequency, phase, and time distribution. More stringent requirements for increased antenna and base station density has caused timing synchronization and accuracy to become a critical capability.

So open-source solutions must include hardware of specific requirements, while minimizing any proprietary or customized software specific to a silicon vendor. Most white box systems are based on the Linux kernel distribution so finding a timing solution that fits this open-source software model is desirable; and it is achieved by using silicon hardware that supports the Linux PTP Hardware Clock infrastructure.

Telecom 1588 Profiles for Phase/Time Synchronization

IEEE 1588 defines a protocol, the Precision Time Protocol (PTP), that enables accurate synchronization over PSNs. It also provides for profiles that allow customization of PTP to fit the needs of specific industries or applications and to support interoperability among devices using the same profile.

ITU-T G.8275.1

ITU-T G.8275.1[0] defines the “Precision Time Protocol Telecom Profile for Phase/Time Synchronization with Full Timing Support from the Network”. It defines the options and attributes from IEEE 1588 to be used to deliver phase/time synchronization to the end application. This profile addresses the case where the Telecom Grandmasters and Telecom Slave Clocks will be used in networks where there is full support for the PTP protocol in all intermediate node, such as Telecom Boundary Clocks or Transparent Clocks, between the PTP master and the PTP slave; in other words, PTP aware networks. It also defines the case where physical layer frequency support is provided, such as Synchronous Ethernet Clocks; the case without physical layer frequency support (specifically, PTP only) is for further study by the ITU-T.

ITU-T G.8275.2

ITU-T G.8275.2[0] defines the “Precision Time Protocol Telecom Profile for Phase/Time Synchronization with Partial Timing Support from the Network”. It defines the options and attributes from IEEE 1588 that deliver phase/time synchronization to the end application. This profile addresses the case where the Telecom Grandmasters and Telecom Slave Clocks are used in networks where there is partial, assisted, or no support for the PTP protocol in the intermediate node between the PTP master and the PTP slave, in other words, PTP unaware or partially aware networks. It focuses on the case without physical layer frequency support (specifically, PTP only), but the profile also defines the case where physical layer frequency support is provided.

See the white paper ITU-T Profiles for IEEE 1588[0] for details on all the ITU-T Profiles.

Telecom Interfaces for Phase/Time Synchronization

The IEEE 1588 does define the protocol and profiles for PTP, but it does not specify synchronization performance requirements; and it does not specify clock recovery servo, filtering, or algorithms. For telecom, synchronization interfaces need to meet ITU-T network limits for clock wander. These limits apply to interfaces synchronized by PTP over a Packet Switched Network (PSN).

ITU-T G.8262

ITU-T G.8262[0] specifies the timing characteristics for synchronous equipment slave clock. It outlines the synchronous Ethernet (SyncE) equipment clock (EEC) and synchronous Optical Transport Network (OTN) equipment clock (OEC), or generic term Synchronous Equipment Clock (SEC), performance requirements for timing devices used in synchronizing network equipment that uses the physical layer to deliver frequency synchronization.

ITU-T G.8262.1

ITU-T G.8262.1[0] specifies the timing characteristics for enhanced synchronous equipment slave clock. It outlines the enhanced synchronous Ethernet equipment clock (eEEC) and enhanced synchronous OTN equipment clock (eOEC), or generic term enhanced Synchronous Equipment Clock (eSEC), performance requirements for timing devices used in synchronizing network equipment that supports synchronous clocks, involved in time and phase transport. It is assumed this is used as the frequency transport for meeting G.8273.2 classes C and D.

ITU-T G.8273.2

ITU-T G.8273.2[0] specifies the timing characteristics for telecom boundary clocks and telecom time slave clocks. It outlines the telecom boundary clock (T-BC) and time slave clock (T-TSC) performance requirements for full timing support (FTS) from the network with physical layer assistance. The short-term effects of Packet Delay Variation (PDV) over aware networks is reduced by low-pass filtering techniques, such as those commonly used for physical layer synchronization.

ITU-T G.8273.3

ITU-T G.8273.3[0] specifies the timing characteristics for telecom transparent clocks. It outlines the telecom transparent clock (T-TC) performance requirements for full timing support (FTS) from the network with physical layer assistance, such as SyncE. During failures in the synchronous Ethernet network, a T-TC may operate with a frequency deviation of 2ppm for a short period of time.

ITU-T G.8273.4

ITU-T G.8273.4[0] specifies the timing characteristics for telecom boundary clocks and telecom time slave clocks for use with partial timing support from the network. It outlines the T-BC-A and T-TSC-A performance requirements for assisted partial timing support (APTS) from the network with Global Navigation Satellite System (GNSS) co-located with the APTS clock (APTSC). It also specifies the T-BC-P and T-TSC-P performance requirements for partial timing support (PTS) from the network with optional physical layer assistance. Packet Delay Variation (PDV) over unaware networks is the major cause of wander on IEEE 1588 based clocks. PDV tolerant IEEE 1588 clock recovery servos are required to limit wander due to PDV in PSNs architected for phase/time distribution. This is because longer-term PDV processes with mean delays that shift over long periods of time become problematic for simple low-pass filtering.

PTP Hardware Clock Infrastructure

The Linux PTP Hardware Clock (PHC) Infrastructure presents a standardized method for developing PTP user-space programs and using the ancillary features of PTP hardware clocks. This Infrastructure was first introduced in v3.0 (July 2011), allowing for controlling of the clock (time, phase, and frequency) and providing timestamps on PTP even messages using the socket option for packet timestamping (SO_TIMESTAMPING). The same device/driver may offer both (specifically, simple NIC de-vice), but for 5G, this is typically split between the network interface timestamping capability and a network timing equipment clock that physically synthesizes the clock.

See PTP Hardware Clock Infrastructure for Linux[0] for additional details on the PHC Infrastructure.

PHC APIs

The applicable PHC driver creates a character device for its hardware clock. The character device allows for user space applications to open a file descriptor, as a POSIX clock id, that may call clock_gettime, clock_settime, and clock_adjtime to implement a basic clock servo. As well, ancillary clock features may be supported, such as period output signals, time stamp external events, or low-pass filter access.

Additional details: https://www.kernel.org/doc/html/latest/driver-api/ptp.html

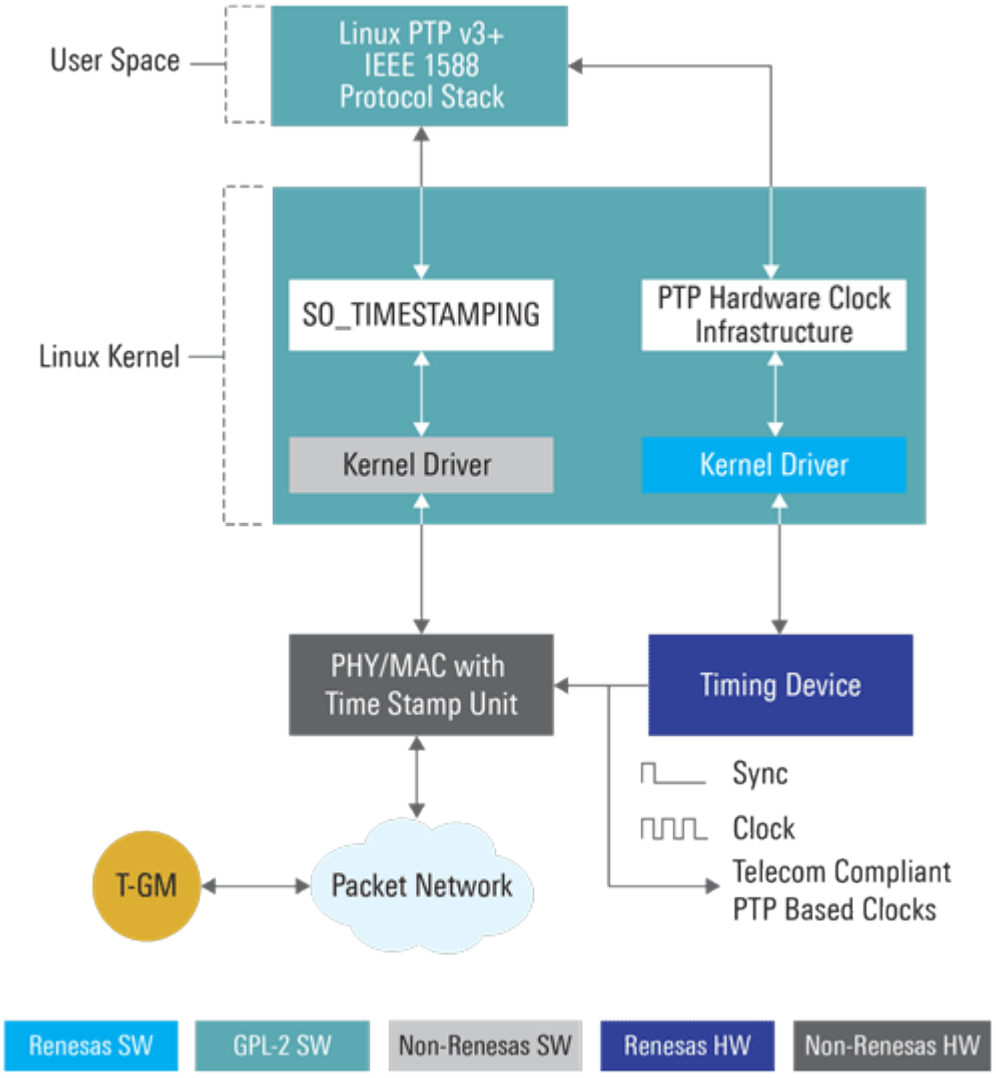

Figure 1. High-Level Overview

PHC Socket Option

The socket option for packet timestamping (SO_TIMESTAMPING) generates timestamps on reception, transmission, or both event packets. The option supports multiple timestamp sources including hardware, which is generally part of the network interface driver.

Additional details: https://www.kernel.org/doc/Documentation/networking/timestamping.txt

Network Timing

Although IEEE 1588 defines a timing protocol that achieves precision timing, it does not describe the process for regenerating the local PTP clock, and key clock attributes should be defined for the equipment clock including the noise generation, noise transfer, and other characteristics.

Fortunately, the International Telecommunication Union (ITU) continues to develop recommendations for network-based clock distribution. Wireless application is the main driver for developing new recommendations to meet synchronization requirements that include phase/time distribution and frequency.

Device Clock Connections within the Equipment

Network timing devices can synthesize many different clock frequencies. Prominently used for physical layer clocking, they are now also being used for generating clocks traceable to the PTP time source, including the PTP reference clock required for the PTP timestamping units (TSU) and a 1PPS measurement clock (per G.8273.2).

The MAC/PHY device with the integrated TSU must support a PTP reference clock input. This input can be a clock that directly clocks the counter (specifically, 125MHz or 250MHz) or a clock for an internal PLL (specifically, 25MHz or 50MHz) that clocks the counter. One should avoid a MAC/PHY device that uses the physical layer reference clock for its TSU, because the physical layer network filtering and packet layer network filtering are different for Telecom. The exception is if this is the T-TSC, as it is terminating both network clocks, the T-TSC is treated as a single clock domain (specifically, single refclk to MAC/PHY).

The MAC/PHY device with the integrated TSU should also support a time stamp external event input (PTP_CLK_REQ_EXTTS). This support simplifies the mechanism required to ensure the primary PHC (specifically, centralized timing device) and the associated PTP TSU (or TSUs for BC) are synchronized for PTP ToD. Because the network timing device must already provide the 1PPS measurement clock, this same clock is sent to the TSU as either a periodic or aperiodic 1PPS signal.

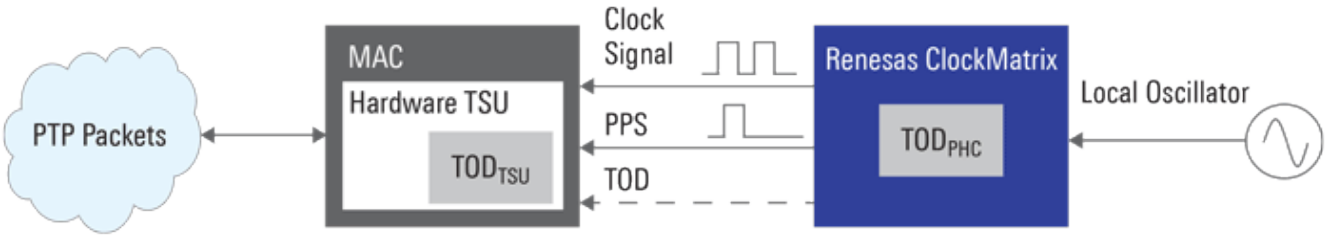

Figure 2. Device Clock Connections

Meeting Requirements of the Equipment Clock

The ITU-T defines a framework for transferring phase/time based on packet-based methods, specifically, using IEEE 1588. The ITU-T publishes recommendations for this framework, and the requirements for the Telecom equipment clock must be followed to ensure interoperability of the equipment produced by different manufacturers and to achieve a satisfactory network performance.

Equipment for 5G O-RAN generally supports a 1PPS + TOD time interface. This interface is defined by ITU-T G.8271[0] in Annex A as a one pulse-per-second (1PPS) time and phase synchronization interface specification.

To get an external time input into the T-BC or T-TSC, use the 1PPS ITU-T V.11 interface described in A.1. For an external monitor interface, as required by G.8273.2 and G.8273.4, generally a dedicated output phase/time reference is used, such as a one pulse per second (1PPS) interface, and as described in A.2 of ITU-T G.8271, a 1PPS 50Ω phase synchronization measurement interface.

- The minimum requirements for telecom boundary clocks and telecom time slave clocks in network elements are in G.8273.2. These recommendations address the distribution of phase/time synchronization with full timing support (FTS) using the related profile defined in G.8275.1.
- The minimum requirements for assisted partial timing support (APTS) and partial timing support (PTS) architectures in network elements are in G.8273.4. These recommendations address the unicast distribution of phase/time synchronization with assisted partial timing support (APTS) or partial timing support (PTS) using the related profile defined in G.8275.2.

The above recommendations include noise generation, noise tolerance, noise transfer, and transient response for both telecom boundary clocks (T-BCs) and telecom time slave clocks (T-TSCs). G.8273.2 is developed based on time transport through precision time protocol (PTP) and frequency transport through ITU-T G.8262 Option 1. For T-BC and T-TSC classes C and D, frequency transport is through ITU-T G.8262.1. G.8273.2 is developed based on time transport through precision time protocol (PTP). The use of synchronous equipment clocks is optional for PTS but not used for APTS.

A key consideration is that the G.8273.2 recommendation does not modify the physical layer reference chain behavior. For this reason, the two equipment clock domains, time and frequency, must remain mutually exclusive. No assumptions on the coherent traceability of their clocks nor the congruency of the time versus frequency transport should be made. For this reason, the ITU-T adapted a co-located model for the T-BC and T-TSC for physical layer assistance.

For FTS architecture, there are many benefits of using a hardware low-pass filter. The most important is that most network timing devices used in equipment have been designed for telecom network synchronization (specifically, same filter technology used for SyncE and locking to a 1PPS signal from GNSS). Because it is implemented in hardware, it is not affected by software loading or interrupts, and its compliance to G.8273.2 for noise transfer is a mathematical certainty. The hardware filter is tolerant to loss of packets and network variation (or jitter) and are highly programmable, which allows the configuration of the cut-off frequency bandwidth, damping factor for gain peaking management, and phase slope limiting when switching between GMs.

For PTS or APTS architecture, the packet delay variation (PDV) on the PTP timing packets require more sophisticated packet filtering for meeting the necessary wander limits. A partial list of causes of PDV in a switching node includes processing, statistical multiplexing, buffering, port contention, and dropped packets. A partial list of causes of PDV for a network includes route diversity and misordered packets. PDV is mitigated in a network by deploying boundary clocks at switching nodes, but this requires an adaptive technical assistance to recover the PTP clock. More details about the effects of PDV is found in “Limiting IEEE 1588 Slave Clock Wander Caused by Packet Delay Variation”[0].

Renesas provides a PDV filter as part of its PTP Clock Manager software that is included with its network synchronization devices. The software interfaces with a PTP stack as described in Use of an External Telecom Servo.

Linux PTP Support for Telecom Profiles

The Linux PTP Project[0] is an implementation of the Precision Time Protocol (PTP) according to IEEE standard 1588 for Linux. It is licensed under the GNU General Public License v2 (GPLv2) and maintained by the Network Time Foundation (NTF)[0]. As a user-space program, it uses the PHC subsystem, SO_TIMESTAMPING, and PHC interfaces to be hardware agnostic. The Linux PTP modular design allows for the addition of new BMCA state machines (specifically, ITU-T Telecom Profiles), network transports, external filters (specifically, the PHC adjphase for hw-filter), and/or external servos (specifically, Renesas PTP Clock Manager). This makes it an optimal fit for O-RAN and the open white box architecture.

As of Linux PTP V2.0 (release August 2018), the addition of the ITU-T Profile support allowed for Linux PTP to be considered seriously as a Telecom PTP stack solution, allowing for migrating from some proprietary PTP stack solutions that are in the market today for Telecom systems. Linux PTP runs as a user-space service as ptp4l; allowing for configuration from a file (.cfg) or through the 1588 Management channel using a UNIC Domain Socket (UDS). The project also includes a management interface program call PTP Management Channel or pmc. It also includes an optional service to discipline the Linux system clock called phc2sys.

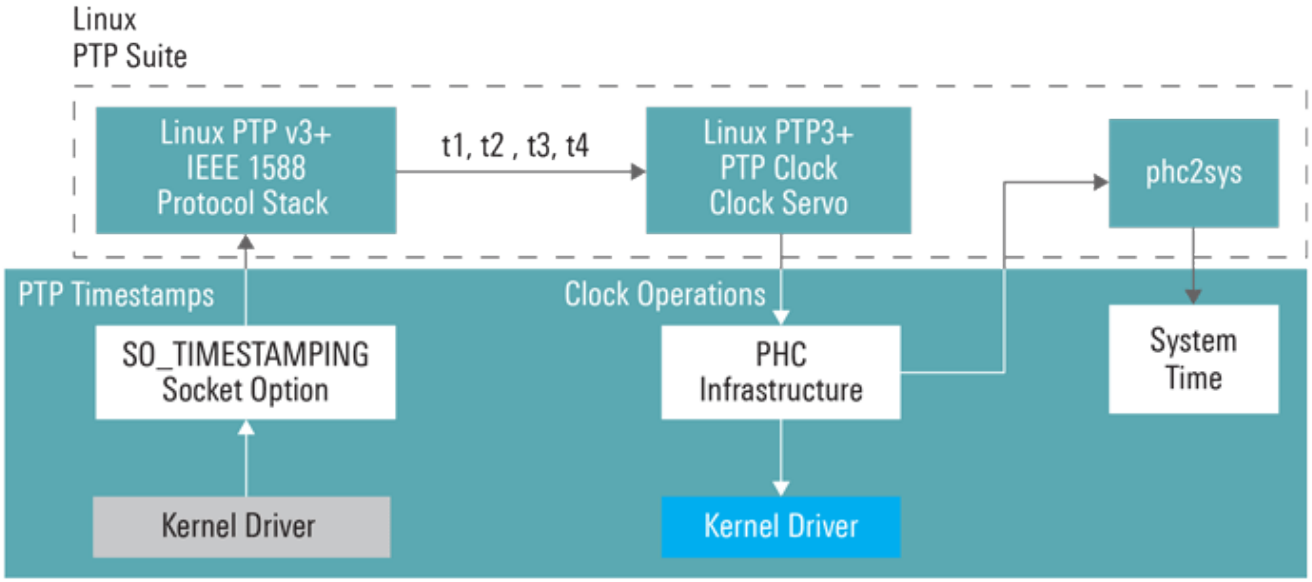

Figure 3. Linux PTP and the PHC Infrastructure

The latest release of Linux PTP (V3.0, released July 2020) adds some substantial new functionality on top of V2.0 release. Three key functional blocks are (1) support for a new state, SERVO_LOCKED_STABLE, (2) a new optional service to discipline the PHC to external timestamps signals or to a “master” PHC, and (3) implementation of the Slave Event Monitoring channel, per IEEE 1588-2019.

The new state SERVO_LOCKED_STABLE allows for support of the PHC filter by using the PHC adjphase API as introduced in Linux v5.8. This allows for the PTP stack to meet not just the ITU-T G.8275.1 Profile but also the equipment clock when used with a ITU-T G.8273.2 compliant network synchronization timing device, such as the Renesas ClockMatrix family of devices. With the introduction of a master PHC device for clock control, the synchronization of the timestamper (OC) or timestampers (BC) is necessary. This is provided by the ts2phc service.

The ts2phc service is a full software implementation of a filter/servo similar to the phc2sys. However, when the filtering of the PTP clock occurs in the master PHC device, it would not be desired to have a second stage filter to the timestampers, especially, to the slave PTP port. Therefore, when ptp4l is controlling a master PHC, the ts2phc servo should be disabled. As a result, only ToD synchronization (specifically, offsets > 1ns) are maintained by ts2phc, as the PTP reference clock to the TSU manages the phase and frequency synchronization.

Renesas provides a complete guide on how to use the PHC Infrastructure with Linux PTP and Renesas timing devices. See Linux PTP Using PHC Adjust Phase Reference Manual[0] for more details.

Use of an External Telecom Servo

One limitation of the Linux PTP servo is support for the full Telecom clock state machine (such as holdover). For this reason, it may be desirable to support an external servo running in user-space. For example, the Renesas PTP Clock Manager for Linux, pcm4l. The PCM contains a full clock state machine to support Free-Run, Acquiring, Locked, Holdover-In-Specification, and Holdover-Out-Of-Specification PTP clock modes (per ITU-T G.8275.1 Appendix V and G.8275.2 Appendix IV). This includes the management of the PTP port state transition

from UNCALIBRATED to SLAVE while it transitions from Acquiring to Locked modes to support the (optional) synchronization uncertain indication.

Because the filtering and servo is external from ptp4l, there should be a method to provide the raw PTP timestamps from the PTP stack to the external filter/servo. This is done through the 1588 Slave Event Monitoring channel (as defined in the latest IEEE standard revision) that was introduced in Linux PTP V3.0. Renesas coordinates the release of its latest PTP Clock Manager V4.0 to support this extension of its PTP stack adapter. This coordination allows for a complete 1588 solution for any of the ITU-T Telecom Profiles and associated equipment clock recommendations.

Contact Renesas for more details on obtaining the PTP Clock Manager software licensing.

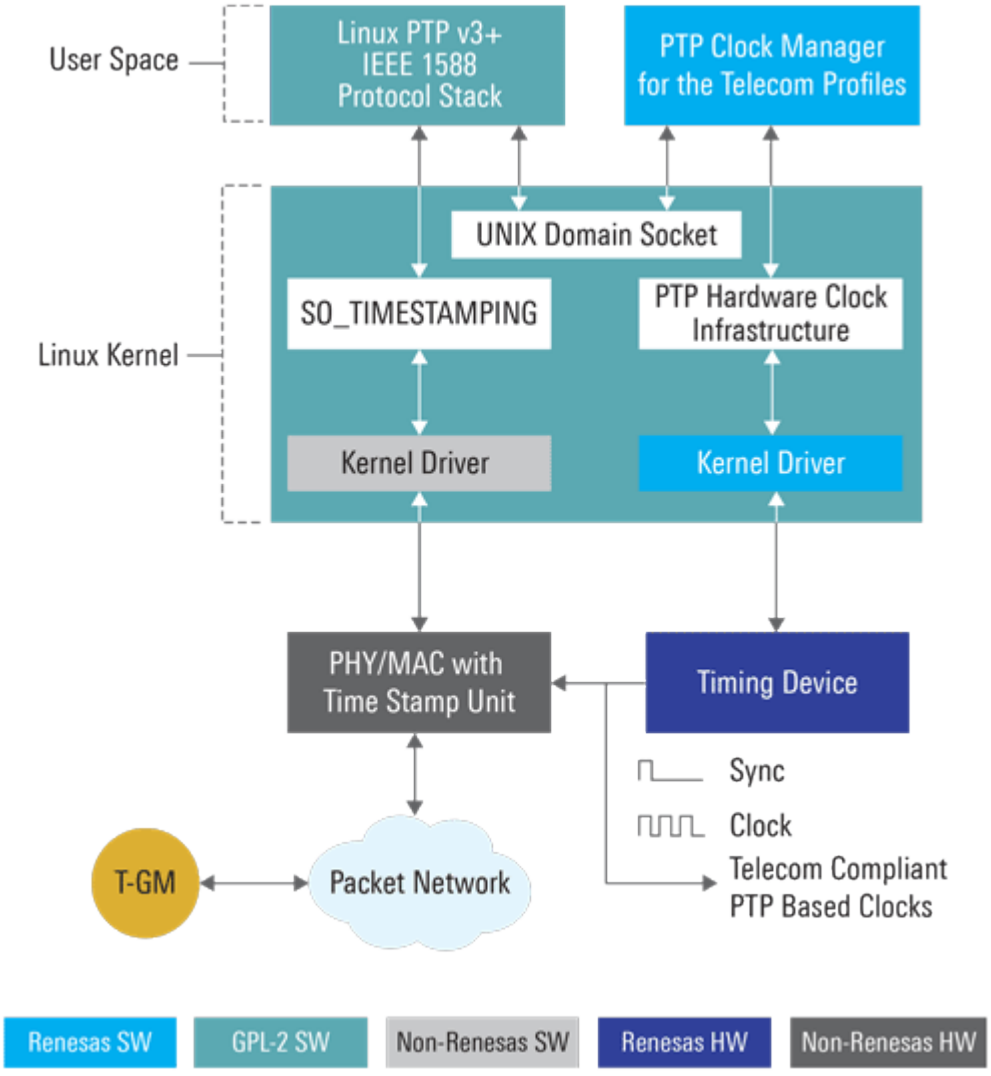

Figure 4. Renesas PTP Clock Manager High Level Overview

Example: Data Centre virtual Distribution Unit (vDU)

A growing opportunity for ORAN is in the data center to support the virtualization of the Base-Band Unit (BBU). In fact, the OTII (Open Telecom IT Infrastructure) has published a 1U Server Technical Specifications[0], which defines a PCIe slot that adds network clock synchronization including 1588/GNSS. See section 5.2.6 of the specification for full details on the server clock synchronization.

To meet the requirements of high-precision time for wireless synchronization of base stations, the server must consider supporting GNSS and/or network clock synchronization. To support this, the OTII specification recommends that the PCIe slot reserves pins to allow for the distribution of this high-precision time, such as 1PPS signals, thereby reducing the complexity of the installation. In addition, the specification recommends reserving two RS422 connectors to support cascaded clock synchronization.

Table 1. Redefined PCIe Connector Pins

Pin Number	Original Pin Name	Redefined Pin Name	Signal Format	Signal Direction to NIC	Description
A19	RSVD	NIC_1588V2_PPS_OUT	3.3V LVCMOS	I	1588 1PPS output signal
A32	RSVD	NIC_1588V2_PPS_IN	3.3V LVCMOS	O	1PPS input signal
A50	RSVD	SLOT1_SLOT2_PPS	3.3V LVCMOS	I/O	1PPS signal between two PCIe slots
B30	RSVD[1] PWRBRK#[2]	SYNC_CLK_OUT	3.3V LVCMOS	I	Synchronization reference clock output signal (optional)
B12	RSVD[1] CLKREQ#[2]	UART_TOD_TXD	3.3V LVCMOS	O	TOD serial output signal[3]
B82	RSVD	UART_TOD_RXD	3.3V LVCMOS	I	TOD serial input signal[3]

1. PCI Express® Card Electromechanical Specification Revision 3.0.
2. PCI Express® Card Electromechanical Specification Revision 4.0.
3. Only Slot 2.

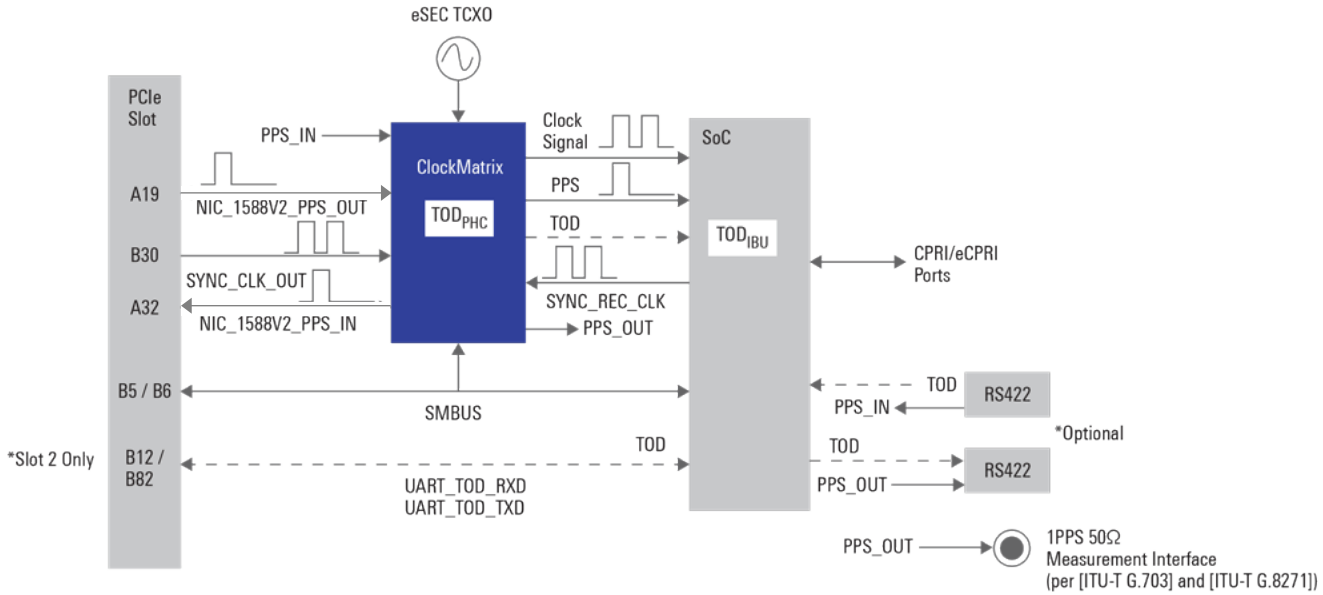

Figure 5. vDU NIC Card Connector

The use of the PHC Infrastructure simplifies the timing distribution within the server, especially with the established 1PPS trigger signals, which allows for multi-PCIe NIC support and support of the open GrandMaster architectures as being proposed by the Open-Compute Platform Timing Appliance Project (OCP-TAP).

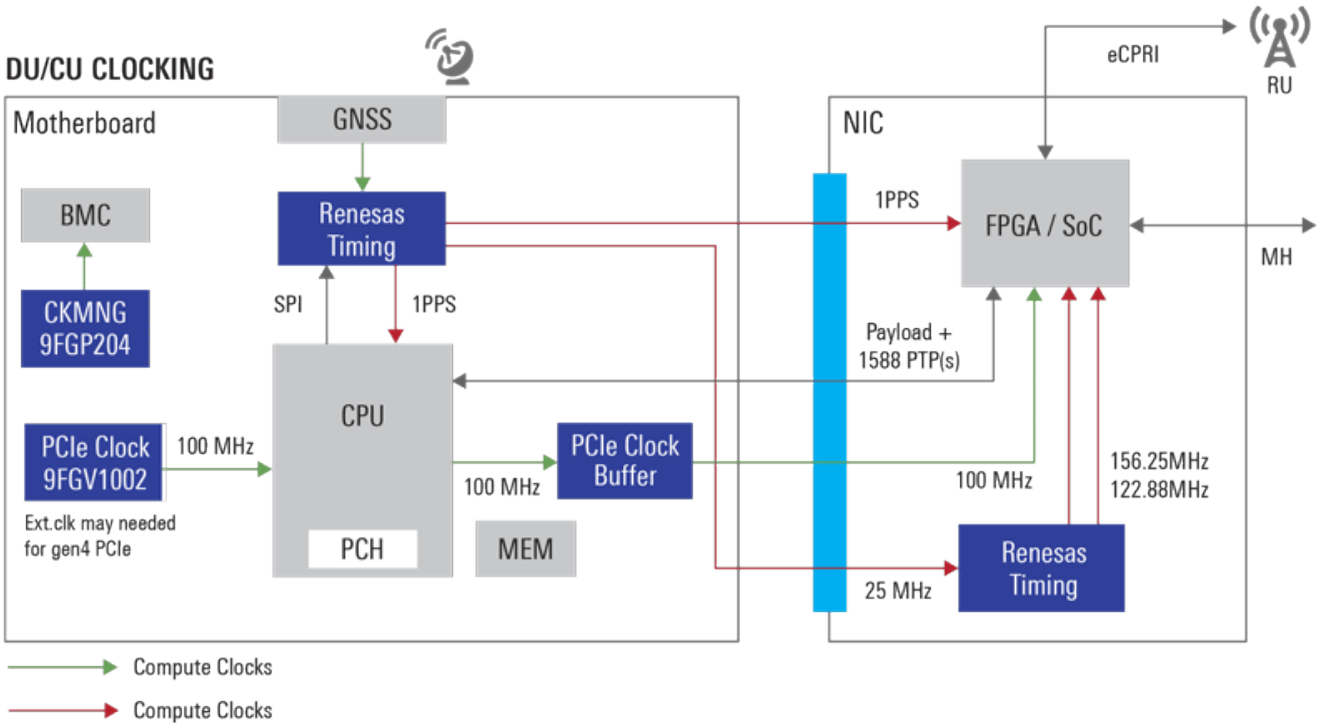

Figure 6. High-Level Overview of a O-RAN vDU

References

1	IEEE Std 1588TM-2019, IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, IEEE Instrumentation and Measurement Society, Published June 16, 2019 (https://standards.ieee.org/content/ieee-standards/en/standard/1588-2019.html)
2	ITU-T profiles for IEEE 1588, Renesas White Paper (https://www.renesas.com/us/en/document/whp/itu-t-profiles-ieee-1588)
3	Limiting IEEE 1588 Slave Clock Wander Caused by Packet Delay Variation, Renesas White Paper (https://www.renesas.com/us/en/document/whp/limiting-ieee-1588-slave-clock-wander-caused-packet-delay-variation?language=en)
4	Linux Kernel Support for IEEE 1588 Hardware Timestamping. (https://www.renesas.com/document/whp/linux-kernel-support-ieee-1588-hardware-timestamping?language=en)
5	Linux PTP Using PHC Adjust Phase Reference Manual, Document Release 4.0.0 (August 7, 2020) (https://www.renesas.com/document/man/linux-ptp-using-phc-adjust-phase-reference-manual-v40169477?language=en)
6	The Linux PTP Project (linuxptp.sourceforge.net)
7	Network Time Foundation (nwtime.org)
The following ITU-T Recommendations can be downloaded from the ITU web site at (www.itu.int/rec/T-REC-G/e.)	
8	Recommendation ITU-T G.8262/Y.1362 Amendment 1 (03/2020), Timing characteristics of synchronous equipment slave clock.
9	Recommendation ITU-T G.8262.1/Y.1362.1 Amendment 1 (08/2019), Timing characteristics of enhanced synchronous equipment slave clock.
10	Recommendation ITU-T G.8271.
11	Recommendation ITU-T G.8275.1/Y.1369.1 (03/2020), Precision time protocol telecom profile for phase/time synchronization with full timing support from the network.
12	Recommendation ITU-T G.8275.2/Y.1369.2 (03/2020), Precision time protocol telecom profile for phase/time synchronization with partial timing support from the network.
13	Recommendation ITU-T G.8273.2/Y.1368.2 Amendment 1 (03/2020), Timing characteristics of telecom boundary clocks and telecom time slave clocks.
14	Recommendation ITU-T G.8273.3/Y.1368.3 Amendment 1 (11/2018), Timing characteristics of telecom transparent clocks.
15	Recommendation ITU-T G.8273.4/Y.1368.4 (03/2020), Timing characteristics of telecom boundary clocks and telecom time slave clocks for use with partial timing support from the network.
16	OTII 1U server technical specifications Version 2020 1.0, Open Data Center Standards Promotion Committee (2020-06-03).

Revision History

Revision	Date	Description
1.02	Sep 2, 2021	Updated Table 1 and Figure 5.
1.01	Mar 9, 2021	Updated Figure 4.
1.00	Mar 1, 2021	Initial release.

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