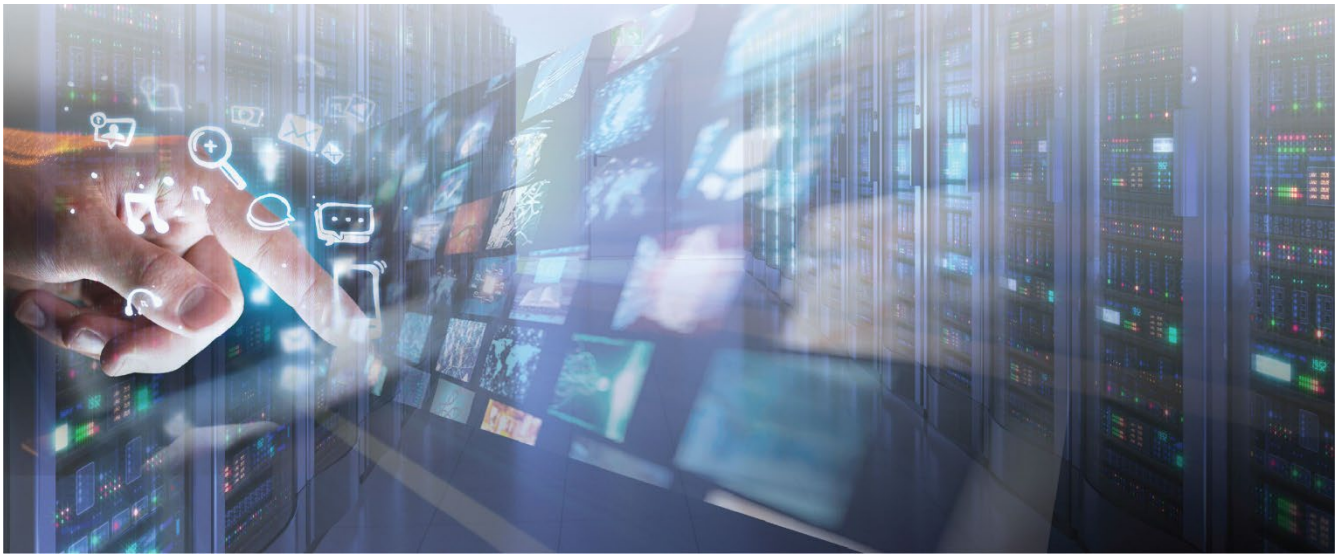
FemtoClock™3 Product Family

112G PAM-4 SERDES Jitter Needs



Abstract

There are many advantages of using Renesas' ultra-high performance clock synchronizers to generate reference clocks needed for high-speed serial links using 112G PAM-4. This document explains a methodology for deriving reference clock jitter requirements, and the advantages of using the Renesas FemtoClock™3 family of low-phase-noise frequency clock synthesizers & jitter attenuators for clocking such a system are outlined.

1. Introduction

The world of data communication is constantly evolving, with new technologies being developed to improve the speed and efficiency of data transfer. We're seeing a few trends that are driving the performance of high-speed SERDES. Below are some examples:

- PCI Express® (PCIe®) starting from legacy, moving into PCIe 4.0 with 16G, PCIe 5.0 with 32G, and, as the spec evolves, PCIe 6.0 with 64G support.
- The high-compute cloud sector that constantly increases performance requirements, looking at 400G and far beyond.
- 5G Wireless Infrastructure, including O-RAN

But with this new technology comes new challenges, and one of the key challenges of designing with a high-speed SERDES is on clock distribution (analog clock tree). Renesas FemtoClock™3 devices are advanced, high-performance clock-frequency synthesizers. Employing a simple, low-cost, fundamental-mode quartz crystal as the low-frequency reference these devices synthesize high-quality, low-jitter clock signals with less than 75 fs of RMS phase noise, up to 1GHz. The RC3 series also offers a jitter attenuation mode along with network synchronization where it can take a noisy reference in and still provide 100fs jitter on its outputs; all while performing ITU-T G.8262.1 enhanced Synchronous Ethernet Equipment Clock (eEEC) wander filtering when using a low-cost, fundamental-mode temperature-compensated crystal oscillator (TCXO) as the reference.

To ensure compliance with industry standards and optimal system performance, it is essential to carefully design and test 112G PAM-4 SERDES links to meet the required jitter specifications. This also includes careful attention to system layout, clocking and synchronization.

2. Coding Schemes

Before we look at clock jitter requirements for 112G SERDES, let's look at two coding schemes that are widely used in SERDES designs today: Non-Return to Zero (NRZ) and Pulse-Amplitude Modulation.

2.1 Non-Return to Zero

A traditional method of modulation is called Non-Return to Zero (NRZ), or also referred as Pulse-Amplitude Modulation 2-Level (PAM-2), that has two voltage levels representing logic "0" and logic "1". The voltage level remains constant through the bit interval so there is one eye in each unit interval; with the symbol being equal to the bit. NRZ is widely used in applications under 56G. At 56Gbps, the Nyquist frequency would be 56G/2=28Ghz.

In NRZ, the data stream 0011-0010-0011 would be coded as follows:

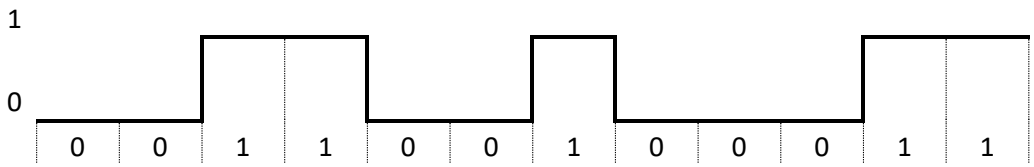


Figure 1. Example NRZ Data Stream

2.2 Pulse-Amplitude Modulation 4-Level

The Pulse-Amplitude Modulation 4-Level (PAM-4) method has four voltage levels for representing logic “00”, “01”, “10”, and “11”. The voltage level remains constant through the bit pair interval so there is one eye in each unit interval; with the symbol being equal to the bit pair. PAM-4 is widely used in applications at and over 56G. At 56Gbps PAM-4, the Nyquist frequency would be 56 / 4 = 14GHz.

In PAM-4, the same data stream 0011-0010-0011 would be coded in half the cycles compared to NRZ:

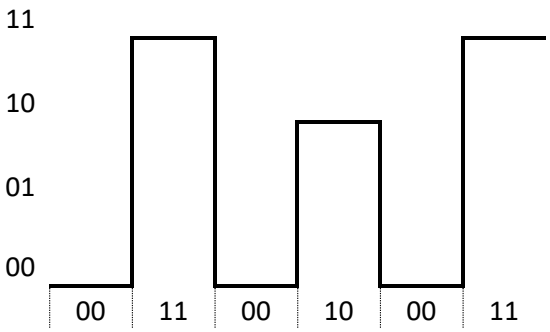


Figure 2. Example PAM-4 Data Stream

2.3 Why PAM-4 for High-Speed SERDES

PAM-4 is gaining traction due to channel loss at higher frequencies. While PAM-4 suffers from ~9.5dB SNR compared to NRZ, it has a huge advantage when inspecting insertion loss. The amount of loss a design can take and still function correctly determines its tolerance to length of the channel, package, quality of the channel materials, noises, returns, cross talk, etc. For example, to be compliant with the Ethernet standard (IEEE 802.3) for 56G, with 14GHz you're looking at an insertion loss of 33.35dB. The same 56G using NRZ would need a 28GHz clock, and the insertion loss would be around 62dB.

It is also essential that 112G PAM-4 SERDES meet all relevant industry standards and specifications, such as the Optical Internetworking Forum (OIF) and the Institute of Electrical and Electronics Engineers (IEEE).

- IEEE 802.3ck, IEEE 802.3cu, IEEE 802.3df and IEEE 802.3dj describe multi-lanes of 100 Gbps per lane for up to 1.6 T Ethernet using a PAM-4 encoding scheme. Several transmission media are supported for delivering 100 Gb/s, 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s operation.
- Similarly, OIF CEI-112G describes data transmission of 112 Gbps from Multi-Chip Modules (MCM) to optical networks over different trace and cable lengths, where the PAM4 modulation scheme becomes dominant.

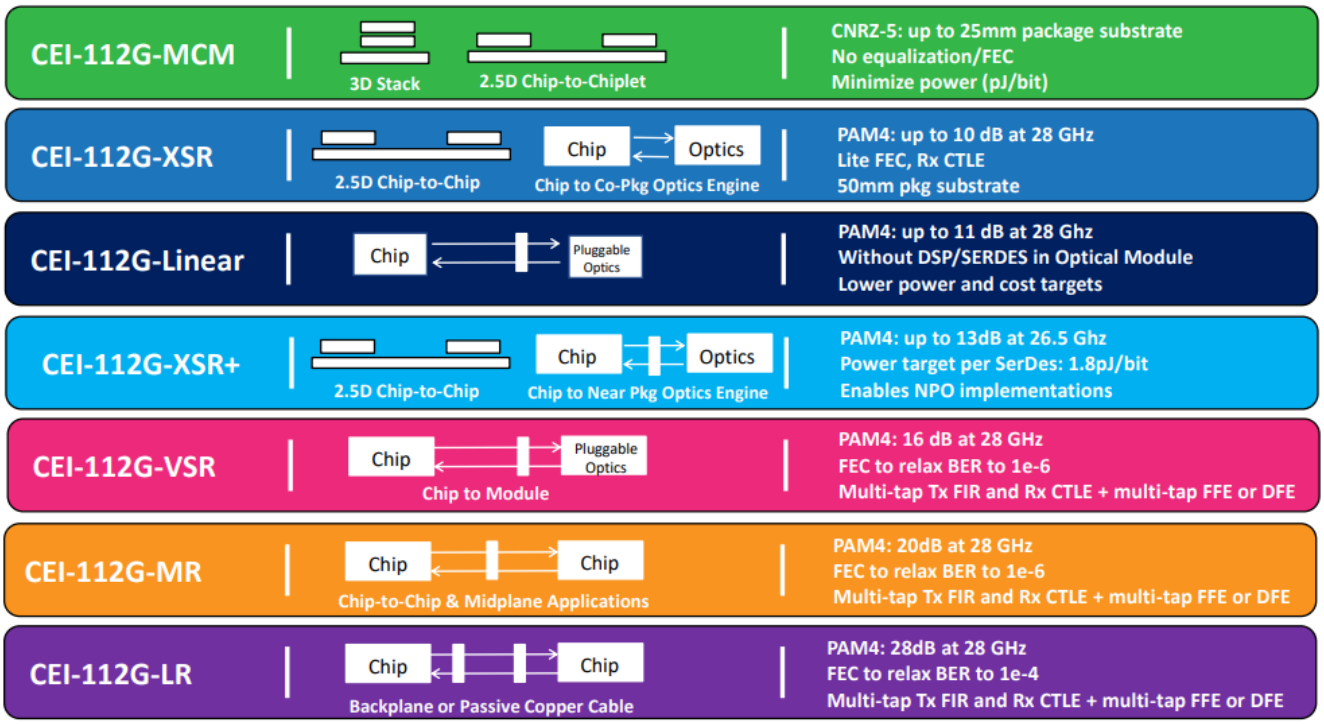


Figure 3. OIF CEI-112G Development Application Space

(Source: OIF_CEI-112G_Demo_OFC2022_presentation)

NRZ is easier to design, and it has a ~9.5dB better signal-to-noise ratio (SNR) compared to a 4-Level PAM (PAM-4). NRZ typically uses less power than PAM-4. However, with higher sampling rates, such as 112G, to get reasonable insertion loss it makes sense to go with PAM-4, even if more challenging to design. Challenges aside, NRZ becomes a less desirable option as rates go higher.

It is important to note that these maximum allowable jitter values are typically defined based on the specific application and operating conditions of the system and may vary depending on factors such as cable length, signal amplitude, and temperature. The allowable jitter for 112G SERDES PAM-4 links is typically specified by the same industry standards organizations. In addition, the actual allowable jitter values for a particular system may also depend on the requirements of the system designer or end user.

3. Deterministic Jitter

Compared to traditional NRZ, PAM-4 signaling is more sensitive to channel impairments such as noise, jitter, crosstalk, and non-linearity. Jitter is a type of signal distortion that occurs when the timing of a signal fluctuates, leading to errors in the transmission of data. In the case of 112G PAM-4 SERDES, jitter can have a significant impact on the performance of the system, making it essential to address the issue of jitter needs in order to ensure optimal performance.

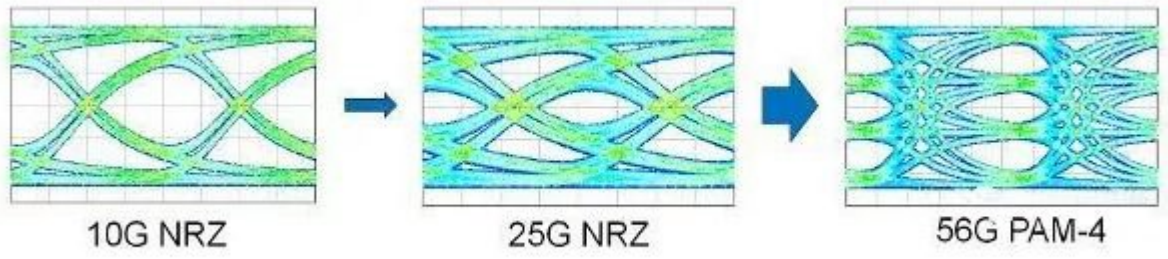


Figure 4. NRZ vs PAM-4 Eye Diagram

(Source: Fibre Mall PAM4 Signal Article)

The SERDES transmitter is usually the source of deterministic jitter. Therefore, having a very low transmit random jitter, typically no more than 100fs for 112G operation, is essential. Stringent 112G PHY interference tolerance/jitter tolerance (ITOL/JTOL) requirements present challenges related to signal integrity. For example, the eye diagram after 2km for 112G PAM-4 could look like Figure 5.

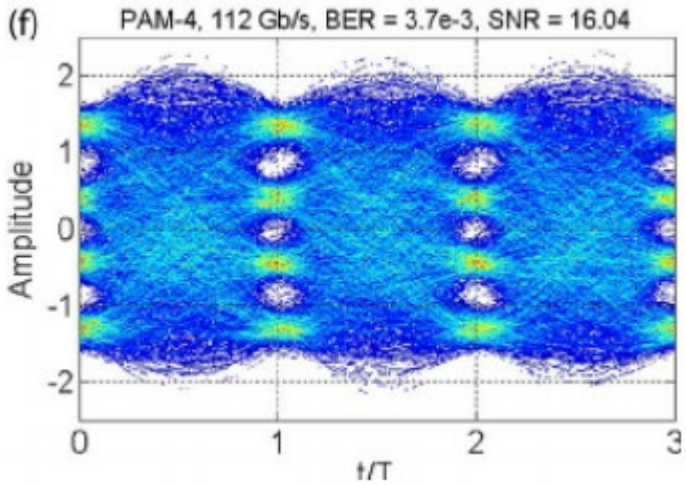


Figure 5. PAM-4 Eye Diagram After 2km

(Source: IEEE Photonics Society Article on 112-Gb/s Transmission System)

When going from 50G input lanes to 100G output lanes, a de-jitterizer function is needed. This is because 100G lane output jitter requirement for a specific frequency is half the peak-to-peak value at 50G.

3.1 Clocking Requirements for 112G PAM-4 Links

The overall allowable jitter in a serial link is dictated by the applicable standard, such as IEEE or OIF. Using 800GAUI-8 as an example, the maximum transmit jitter (RMS) should be no more than 0.023 * UI where 1 UI is the period of 53.125G (0.023RMS would translate to 0.23-0.25 p-p which is 25% of the eye). This equates to 433 fs RMS for the overall allowable transmit jitter. Based on different trace and cable lengths, Table 1 lists the reference clock needs in 112G PAM-4 links.

Table 1. Transmitter Output Jitter

Interface	Baud Rate	Transmitter Output Jitter	Description
CEI-112G-XSR-PAM4	Between 36 Gsym/s and 58 Gsym/s	0.0224*UI (RMS)	From OIF-CEI-05.1, section 24 “CEI-112G-XSR-PAM4 Extra Short Reach Interface”
CEI-112G-MR-PAM4		0.023*UI (RMS)	From OIF-CEI-05.1, section 26 “CEI-112G-MR-PAM4 Medium Reach Interface” and section 27 “CEI-112G-LR-PAM4 Long Reach Interface”
CEI-112G-LR-PAM4			
IEEE 802.3ck	25.78125 or 26.5625 GBd	0.023*UI (RMS)	From IEEE Std 802.3ck™-2022, IEEE Std 802.3cu™-2021, IEEE P802.3df™/D2.0
IEEE 802.3cu	26.5625 or 53.125 GBd		
IEEE 802.3df (800GAUI-8)	53.125 GBd		

However, only a portion of the overall allowable transmit jitter is allocated to the reference clock. For example, multiple switch ASIC vendors with 112G PAM-4 SerDes require a maximum reference clock jitter of 100 fs RMS over a frequency band of 12 kHz to 20 MHz. This reference clock requirement comes from a general rule-of-thumb of allocating up to 20% of the overall RMS jitter budget to the reference clock. The equation to determine $T_{j\text{-}refclk}$ is sqrt(T_{total}^2 - $T_{j\text{-}tx}^2$). Simplifying the equation for 20% budget, this results in dividing the transmitter output jitter (RMS) by sqrt(5). Table 2 lists the minimum reference clock needs for random jitter in 112G PAM-4 links.

Table 2. 112G Reference Clock Requirements

Interface	Reference Clock	Description
High Frequency Uncorrelated Unbounded Gaussian Jitter	0.009*UI (RMS)	This allocates about 15% of the overall allowable transmit jitter to the reference clock. UI is still the period of the baud rate, or 53.125 GBd. The reference clock is typically set to be 1/64th of the baud rate. However, most 112G SERDES or Switch ASICs use 312.5 MHz for a reference clock.
Single Side Band (SSB) Phase Noise	-131 dBc/Hz	@ 10kHz offset
	-137 dBc/Hz	@ 100kHz offset
	-143 dBc/Hz	@ 1MHz offset
	-158 dBc/Hz	@ ≥10MHz offset

3.2 112G Clocking with Renesas FemtoClock™3

The FemtoClock™3 family of devices are ultra-high performance clock generators, jitter cleaners, and clock synchronizers. The RC3 series have advanced reference clock selection and hitless switching feature to meet the stringent ITU-T requirements of communications infrastructure applications. The ultra-low jitter performance of these device minimizes bit error rates (BER) in applications involving high-speed serial links, such as 112G PAM-4 SERDES.

FemtoClock™3 features a single channel synchronizer that can synchronize to one of four differential or single-ended reference clock inputs. The synchronizer is accompanied by an Analog Phase Locked-Loop (APLL) domain that features Renesas’ new generation, ultra-low phase noise VCO and generates <60 fs rms typical jitter in the frequency band of 12 kHz to 20 MHz for a 312.5 MHz output; both of which exceed the 112G PAM-4 reference clock needs as specified in the standards and for the switch ASICs.

Figure 6 shows the phase noise plot of 312.5 MHz LVPECL output from the APLL. There are additional FOD domains that can be used to generate unrelated frequencies either locked to the reference clock input or the

free-run XO input and generates <120 fs, rms typical jitter. FemtoClock™3 can generate up to twelve high performance output clocks with up to four different frequencies.

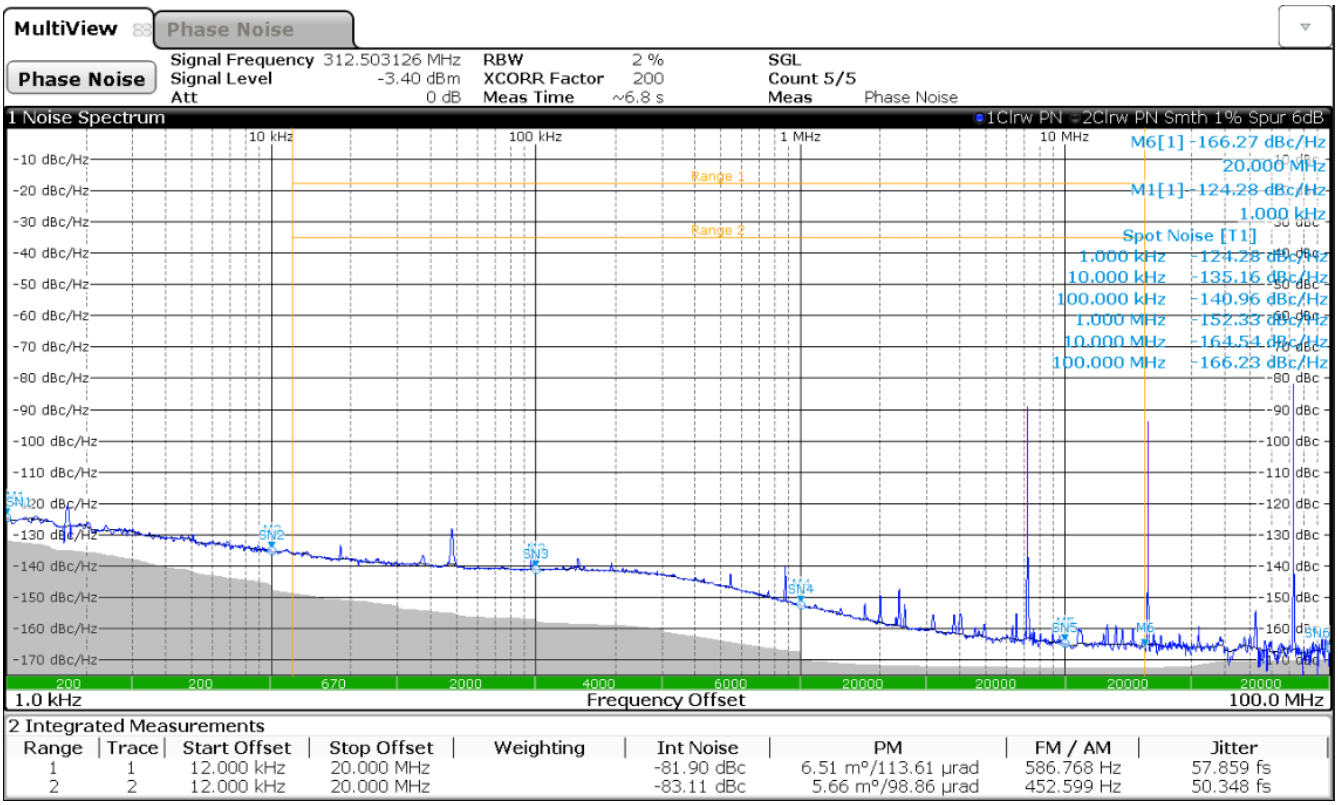


Figure 6. 312.5 MHz Phase Noise

3.2.1. Advantages

FemtoClock™3 is the only clock synthesizer solution to meet the 112G specification at all offsets with the most margin when generating ultra-low jitter (<60 fs rms) reference clocks. With up to 4 independent frequency domains, improved EMI, low power, and integrated LDOs with superior PSRR, FemtoClock™3 simplifies the PCB layout for 112G SERDES applications.

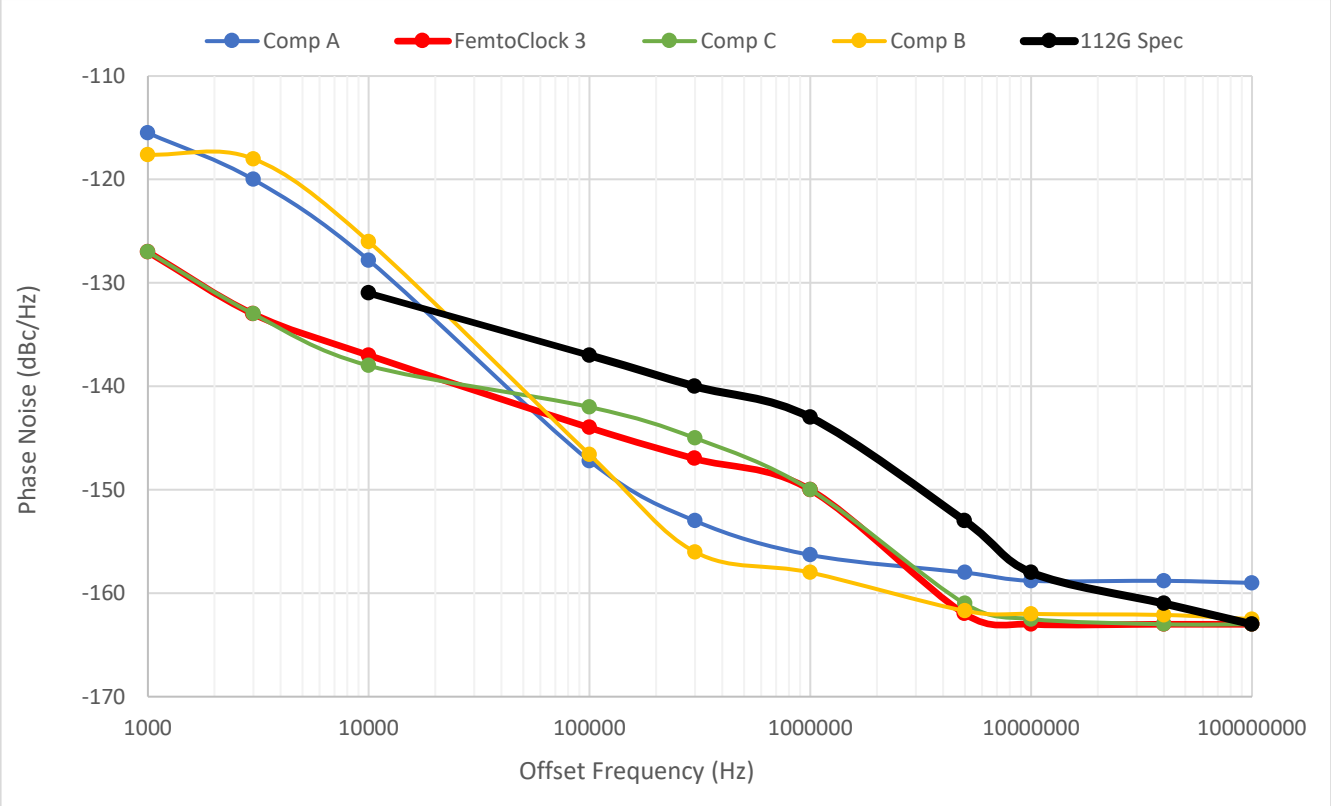


Figure 7. FemtoClock™3 vs Competition - 312.5 MHz Phase Noise

In addition, compliance to ITU-T G.8262 Synchronous Ethernet and G.8262.1 enhanced Synchronous Ethernet, with no jitter degradation when using a low frequency TCXO (< 20MHz), makes it ideal for the latest 5G infrastructure equipment using 112G SERDES technology.

4. Summary

112G PAM-4 SERDES represents a significant advance in the field of data communication, offering the potential for faster and more efficient transmission of data across networks. However, to ensure optimal performance, it is essential to address the issue of jitter needs, including low jitter tolerance, precise timing synchronization, advanced signal processing, high-speed testing, and compliance with industry standards. Ultra-high performance clock synchronizers from Renesas such as the FemtoClock™3 family of devices can outperform the overall performance of high-speed serial link systems as outlined in this white paper.

The ultra-low jitter of the RC32312, combined with features like support for synchronization and frequency margining, simplify the overall system development. By addressing these needs, designers and engineers can ensure that 112G PAM-4 SERDES operates at peak performance, providing reliable and efficient communication across a wide range of applications.

References

- https://www.chipestimate.com/Understanding-the-high-speed-SerDes-solution-space-10G-112G/Cadence/Technical-Article/2020/06/30
- https://www.renesas.com/products/clocks-timing/femtoclock-low-phase-noise-frequency-synthesizers

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
https://www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
https://www.renesas.com/contact-us

Trademarks

Doc Number: R31WP0004EU0200