Direct 800V-to-6V Conversion for AI Compute Infrastructure

A modular 20 kW, 128:1 LLC DCX architecture for next-generation power delivery boards

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Abstract

Artificial intelligence infrastructure is increasing compute density and pushing power delivery from centralized shelves toward distributed power delivery boards located inside each compute tray. High-voltage DC distribution reduces rack-level current, but the downstream conversion path remains a critical determinant of efficiency, volume, thermal load and copper utilization.

This paper presents a direct 800V-to-6V isolated DCX LLC DC/DC concept developed around a fixed 128:1 conversion ratio. The proposed 20 kW architecture combines two 10 kW input-parallel/output-parallel converter groups in an input-series/output-parallel arrangement. Each 10 kW group is formed from two 5 kW full-bridge LLC building blocks. The modular structure supports an 800V input while delivering a high-current 6V output close to the point of load.

Each 5 kW building block uses four TP65H020G4PLSGBD 650V GaN primary switches, a matrix-transformer structure, low-voltage synchronous rectification and interleaved operation. The demonstrated power area for the complete 20 kW converter is approximately 400mm x 60mm x 6.5mm, excluding the horizontal output bus bar. The current design target is greater than 96% efficiency at 20 kW.

By removing intermediate 48V and 12V conversion stages from the rack-bus-to-processor path, the architecture offers a route toward fewer conversion stages, lower distribution current at the rack level and a compact low-voltage source for downstream voltage-regulator modules. The result is a practical platform for evaluating direct high-ratio conversion in future AI compute systems.

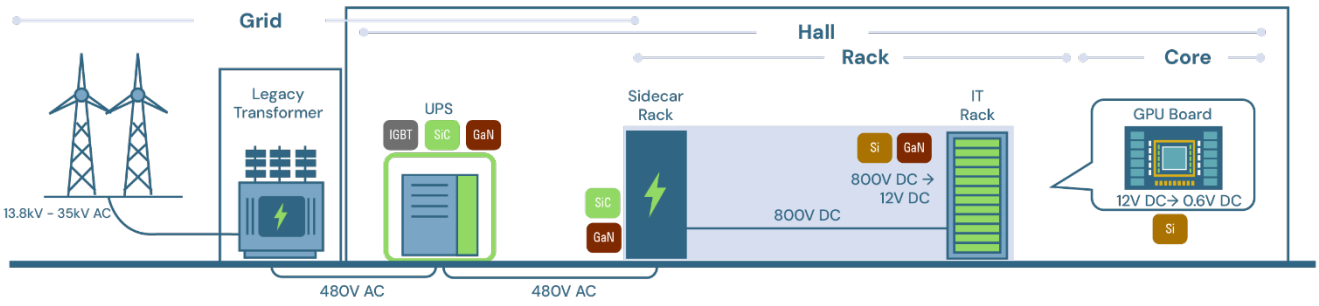
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Introduction

The rapid expansion of artificial intelligence is transforming the electrical architecture of data centers. AI accelerators, high-performance CPUs, networking devices and memory systems are driving rack power well beyond the levels addressed by conventional server infrastructures. Installed systems are already exceeding 200 kW per rack, while future deployments must accommodate increasingly dense computing configurations within strict thermal, mechanical and electrical limits. At the same time, individual xPUs can demand currents above 3kA, placing unprecedented stress on the complete power delivery network.

These trends are forcing industry to reconsider the traditional 48V rack architecture. As rack power approaches approximately 350 kW, distributing the required energy at 48V leads to extremely high currents, increased conduction losses and considerably greater copper requirements for bus bars, connectors and distribution structures. Higher voltage DC distribution therefore becomes an essential architectural step rather than a simple incremental improvement. The emerging 800V, or ±400V, low-voltage Direct Current (LVDC as per OCP standardized nomenclature in the released specification 1.1.0) architecture enables power to be distributed efficiently from a centralized sidecar power rack to multiple compute racks, reducing current throughout the high-power distribution path and improving the scalability of the overall infrastructure.

Within this architecture, the sidecar rack converts the facility's three-phase AC input into 800V DC bus (LVDC) and may also provide the connection point for energy-storage resources. The 800V bus is then delivered to the IT rack, where high-power DC/DC converters generate the lower intermediate bus voltages required by the compute trays. Both two-wire 800V and three-wire ±400V configurations (used seamlessly across this paper) are being considered and can be accomplished by the proposed converter. The two-wire implementation can provide better copper utilization, while the split-bus approach reduces the voltage stress imposed on individual converter stages, although it introduces additional balancing and control requirements in the front-end AC to 800V power supply.



The move to 800V does not, however, define a single downstream conversion chain in the Compute Rack. Several architectural permutations are possible between the high-voltage bus and the processor supply. An 800V-to-48V isolated conversion stage can preserve compatibility with the existing 48V power ecosystem, allowing established intermediate-bus converters, power-distribution boards and point-of-load solutions to continue to be used. Alternative approaches can convert directly from 800V to 12V or 6V to be used by the multi-phase core supply, potentially eliminating a conversion stage and improving system-level efficiency and power density. The optimum solution, defined by Figure of Merit (FOM) like efficiency, power density, current density, depends on the power level of the specific xPU, the number of accelerators per compute tray, the mechanical construction of the tray, isolation requirements, redundancy strategy and the architecture of ancillary power rails.

High-frequency resonant conversion, advanced magnetic integration and wide-bandgap semiconductor technologies are important enablers for these new high-voltage conversion stages. LLC Direct Current

Transformer (DCX) topologies can provide an efficient, fixed-ratio conversion between the 800V bus and an intermediate output, while matrix planar transformers support compact, scalable implementations with controlled current sharing and reduced magnetic losses. GaN devices further enable higher switching frequencies and smaller passive components selection, helping converters achieve the efficiency and power density required inside increasingly constrained rack and tray form factors. In summary, as of today, Silicon and GaN semiconductor technology dominate the Compute Rack content.

Below the intermediate bus, the power architecture must ultimately support low-voltage, high-current loads with very fast transient behavior. Reducing the intermediate voltage from 12V toward 6V can improve the efficiency of the final multiphase stage, while emerging vertical power delivery and integrated voltage regulator concepts are essential to shorten the electrical path between the converter and the processor, as well as reduce power distribution network (PDN) losses. Nevertheless, these core-supply stages form only one part of a broader grid-to-core optimization problem. The principal architectural challenge is to select the proper combination of bus voltages, conversion ratios, topologies, semiconductor technologies, control methods and packaging approaches that delivers the best overall balance of efficiency, power density, reliability, scalability and cost.

This paper examines direct conversion from an 800V DC distribution bus to a 6V intermediate rail for AI compute trays. It presents a modular 20 kW, 128:1 LLC DCX architecture built from 5 kW full-bridge converter cells and describes the use of Renesas TP65H020G4PLSGBD 650V GaN switches in PQFN 8x8 DSC, matrix transformers, low-voltage synchronous rectification, interleaving, integrated bus bars and digital control. The discussion covers the electrical and mechanical implementation, the analytical efficiency and loss model and the prototype validation required to establish a scalable, high-density power-delivery platform for next-generation AI infrastructure.

From High-Voltage (LVDC) Distribution to Low-Voltage Compute

The adoption of an 800V DC (LVDC) distribution bus changes where power conversion can be placed. Instead of converting the rack bus in a centralized power shelf and distributing 48V IBC at very high current, conversion can be distributed across power delivery boards (PDB) located within the compute trays. The high-voltage bus is then routed to each tray, where local DC/DC stages generate 48V, 12V or 6V rails for downstream regulation. The block diagram depicted in figure 1 shows the tray-level power conversion described above.

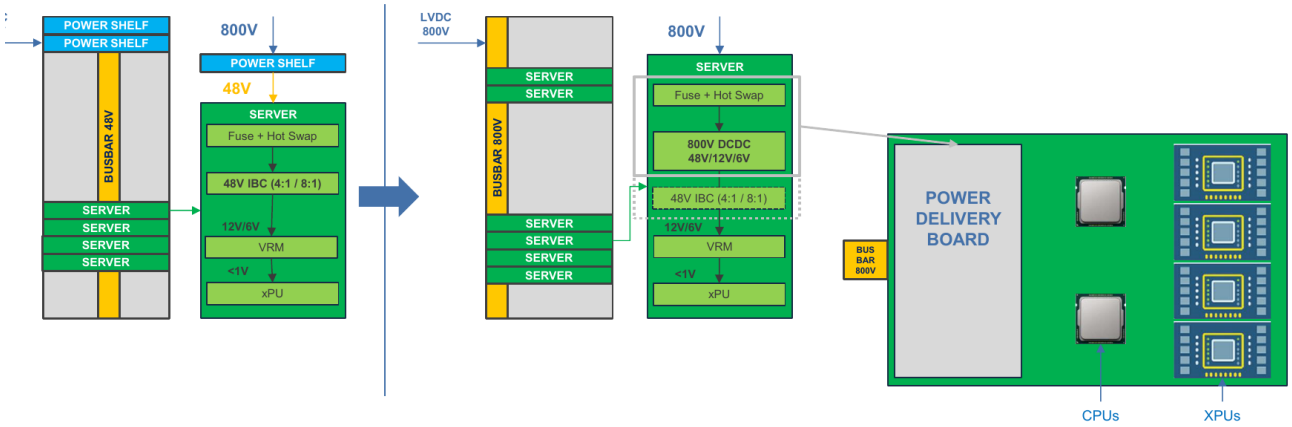


Figure 1. Transition from centralized 48V distribution to tray-level conversion from an 800 VDC bus

The architecture examined here takes the distributed approach one step further by converting the 800V bus directly to 6V. A local Vertical Power Distribution (VPD) digital multi-phase DC/DC converter then completes the conversion to the sub-1V rails required by xPUs. This structure is intended to reduce the number of intermediate buses between the rack distribution system and the compute load.

Why Direct 800V-to-6V Conversion?

While first-generation LVDC architectures typically employ an isolated 16:1 conversion stage to generate a conventional 48V intermediate bus, future AI systems may benefit from a more aggressive reduction in the number of conversion stages. Instead of implementing the traditional conversion chain of 800V → 48V → 12V → Core Voltage, future architectures may increasingly adopt a direct 800V → 6V intermediate bus dedicated to AI processor power delivery. This approach offers advantages not only in efficiency but also in power density, thermal management, current density and compatibility with emerging processor packaging technologies.

Eliminating conversion stages improves Grid-to-Core efficiency. As rack power approaches several hundred kilowatts, efficiency must be evaluated at a system level rather than at the individual converter level. Even highly optimized architectures accumulate losses across multiple conversion stages. A conventional architecture implementing 800V-to-48V conversion followed by a 48V-to-12V intermediate bus converter and finally multiphase core regulation may achieve excellent efficiency in each individual block, yet the cumulative impact becomes substantial when supplying hundreds of kilowatts.

A direct 800V-to-6V architecture removes one complete conversion stage, reducing conduction losses, switching losses, magnetic losses and associated thermal dissipation. The resulting efficiency gain may appear modest on a percentage basis but translates into several kilowatts of reduced heat generation at rack level. These reductions benefit not only the power electronics but also the cooling infrastructure that must continuously remove the generated heat. Consequently, direct conversion becomes increasingly attractive as rack power scales toward 350 kW and beyond. Additionally, supplying the final digital multi-phase stage with 6V enables an extra boost of efficiency in that stage, through usage of lower voltage node technologies.

In addition to the well-known efficiency and thermal management related considerations, the 800V to 6V direct conversion offers an output voltage which is better aligned with future processor requirements.
The emergence of Vertical Power Delivery (VPD) is reshaping the way power reaches AI accelerators.
Instead of delivering current through long horizontal power-distribution paths on the package substrate, new power architectures increasingly inject power vertically through the underside of the processor package, minimizing impedance and reducing transient voltage excursions.
The objective is to shorten the Power Distribution Network (PDN), reduce resistive losses and improve transient response as processor currents exceed multiple kiloamps.
Current density is rapidly becoming the primary constraint for future AI power delivery systems. The industry currently supports about 2A/mm² current density, while future platforms are expected to require substantially higher values. Achieving these targets requires minimizing electrical path length, reducing parasitic inductance and lowering distribution impedance throughout the power-delivery network.

Direct generation of a 6V rail closer to the compute device enables significant improvements in these areas. By reducing the physical distance between the final conversion stage and the load, designers can lower IR drops, reduce transient-induced voltage deviations and decrease the amount of bulk capacitance required to maintain voltage stability. This contributes directly to higher system efficiency and improved electrical performance under the extremely dynamic load conditions characteristic of modern AI accelerators.

A 6V intermediate bus aligns naturally with these requirements. The final voltage conversion ratio from 6V to the processor operating voltage is substantially lower than from a traditional 12V rail, reducing voltage stress on the switching devices while enabling higher switching frequencies and improved dynamic performance. The lower conversion ratio also facilitates implementation of highly integrated voltage-regulation structures placed physically closer to the silicon die.

The evolution toward a 6V intermediate bus also opens the door to innovative conversion schemes beyond traditional isolated bus converters. As mentioned, different permutations in conversion are possible, in aim to optimize performance. The use of Hybrid Switched Capacitor (HSC) converters, advanced LLC DCX implementations and matrix-transformer-based architectures creates additional opportunities to improve power density and efficiency while maintaining scalability across multiple rack power levels. For example, the possibility of replacing today's 4:1 intermediate bus conversion stage with more aggressive conversion ratios (8:1 or higher), enables direct generation of lower intermediate voltages optimized for AI core supply.

The architectural flexibility offered by these approaches allows different optimization paths depending on processor power level, rack configuration and cooling strategy. Rather than enforcing a single universal architecture, direct 800V-to-6V conversion provides another important building block for future AI system architects seeking the best balance between efficiency, density, cost and reliability, to be benchmarked against other possible cascaded architectural approaches.

800V to 6V Converter: A Dedicated Power Path for AI Compute

A particularly attractive aspect of the 800V-to-6V approach is the possibility of creating two independent optimization domains inside future AI infrastructure. Conventional 48V distribution can continue supporting networking, storage, cooling subsystems and auxiliary functions, preserving compatibility with the existing ecosystem. At the same time, a dedicated 6V path can be optimized specifically for AI core power delivery, enabling future VPD, IVR and advanced packaging technologies without requiring a complete redesign of the remaining rack infrastructure.

In this vision, the transition to 800V distribution represents only the first step. The subsequent migration toward lower intermediate voltages may ultimately prove equally important by enabling the next generation of AI accelerators to operate at higher efficiency, greater power density and improved scalability while maintaining manageable thermal and electrical constraints throughout the entire power-delivery chain.

Table 1 below summarizes key design considerations for both multi-stage approach versus the direct 800V to 6V DCX LLC conversion path.

Design consideration	Multi-stage path	Direct 800V-to-6V DCX path
Conversion chain	800V => 48V => 12/6V => core	800V => 6V => core
Isolated intermediate stages	More than one may be required	One isolated high-ratio DCX
Rack/tray distribution	High current after early step-down	High voltage retained to the compute tray
Primary design challenge	Accumulated loss and hardware across stages	Extreme ratio, magnetics, high output current
Validation priority	Stage-by-stage optimization	System efficiency, sharing, isolation, transient response

Table 1. Architectural comparison. Statements describe the proposed concepts and are not product guarantees.

A Modular 20 kW, 128:1 LLC DCX Architecture

The evolution of AI compute platforms is driving power delivery toward a fundamentally different architecture than the one used in conventional servers. As hyperscalers adopt 800V rack-level distribution and progressively move power conversion closer to the processor, a direct 800V-to-6V intermediate bus emerges as an attractive alternative to the traditional 48V and 12V conversion hierarchy. To evaluate this concept, Renesas has developed a Proof-of-Concept reference design based on a modular 20 kW, 128:1 LLC Direct Current Transformer (DCX) architecture specifically targeting next-generation AI compute trays.

The proposed solution is designed around a highly scalable building-block philosophy. Rather than implementing a monolithic 20 kW converter, the architecture is constructed from a set of identical 5 kW Full-Bridge LLC DCX converter modules. Each 5 kW module operates from a 400V input rail and directly generates a regulated 6V output through a fixed-ratio resonant conversion stage. Four of these 5 kW building blocks are then interconnected using Input-Series Output-Parallel (ISOP) and Input-Parallel Output-Parallel (IPOP) techniques to realize a complete 20 kW, 800V-to-6V conversion system. This modular approach simplifies development, improves manufacturability and provides a natural path toward higher power implementations through replication of standardized converter cells.

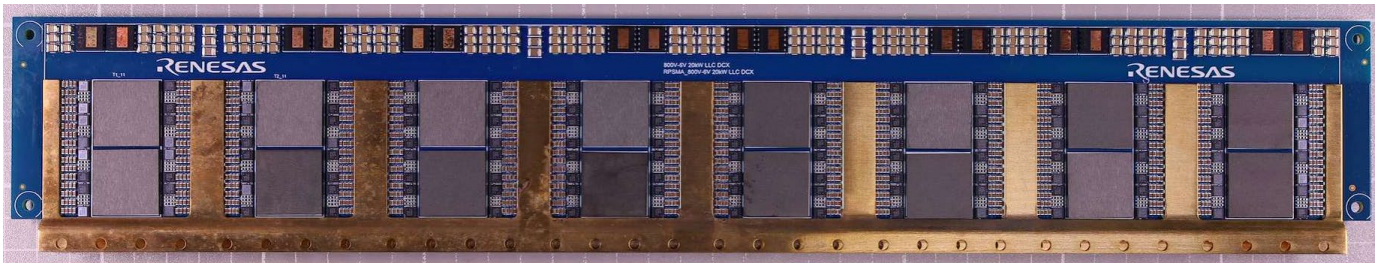


Figure 2. Proposed 20 kW LLC DCX DC/DC converter

At the converter-cell level, each 5 kW module utilizes a full-bridge LLC topology built around four Renesas TP65H020G4PLSGBD 650V GaN switches on the primary side and an array of ultra-low-voltage synchronous rectification stages on the secondary side in center-tap configuration – block diagram depicted in Figure 3. The new D-mode device delivers 20 mΩ on-resistance—among the lowest in the 650V class—in a compact 8×8 mm PQFN package. By combining low conduction loss with a small footprint, it provides the power density and space efficiency demanded by compact 800V infrastructure. The power stage employs four series-connected transformers, each processing approximately 1.25 kW, providing a total module power capability of 5 kW. The secondary side implements a multi-winding center-tapped architecture optimized for extremely high output current operation at 6V. The complete power BOM of a single 5 kW module comprises only four 650V GaN devices, thirty-two 25V QFN3x3 MOSFETs and sixteen dual-channel MOSFET drivers (ISL89163 or same size QFN3x3 next generation driver coming soon to support also GaN variant not just Silicon), highlighting the remarkable simplicity of the solution considering the achieved power density and conversion ratio.

A key enabler of the architecture is the LLC DCX operating mode. In contrast to conventional LLC converters, which regulate output voltage by continuously adjusting switching frequency, the DCX operates at or near resonance with a fixed conversion ratio determined by the transformer turns ratio. Under these conditions, the converter behaves as a high-efficiency DC transformer, transferring energy with minimal control overhead. Zero Voltage Switching (ZVS) is achieved on the primary-side GaN devices, while Zero Current Switching (ZCS) is

realized on the secondary side, significantly reducing switching losses and electromagnetic emissions. Because downstream voltage regulators perform the final load regulation, the intermediate 6V output does not require tight regulation, allowing the converter to operate in its highest efficiency region across a broad operating range.

To realize the extreme 128:1 conversion ratio while maintaining practical dimensions, the converter leverages an array of compact matrix-transformer structures. A total of sixteen transformers are distributed throughout the complete 20 kW system, each transformer measuring only 21mm × 21mm and incorporating four secondary windings. Unlike conventional magnetic implementations where each transformer operates independently, the matrix-transformer concept integrates multiple windings and magnetic paths into a tightly coupled structure. This approach improves current sharing, reduces leakage variation, minimizes core losses and enables significantly higher power density. Flux cancellation between phases further contributes to magnetic optimization while reducing transformer volume and thermal stress.

The modular arrangement consists of two 10 kW converter groups connected in parallel at 400V input. These two 10 kW sections are then connected in series on the input side to support the full 800V rack distribution bus while maintaining a low-voltage, high-current 6V output. This arrangement keeps each full bridge within the 650V device class and enables the TP65H020G4PLSGBD to combine its 20mΩ on-resistance and compact 8×8mm PQFN footprint with practical voltage margin. The resulting architecture couples the benefits of high-voltage distribution and direct low-voltage conversion with the power density of Renesas GaN technology.

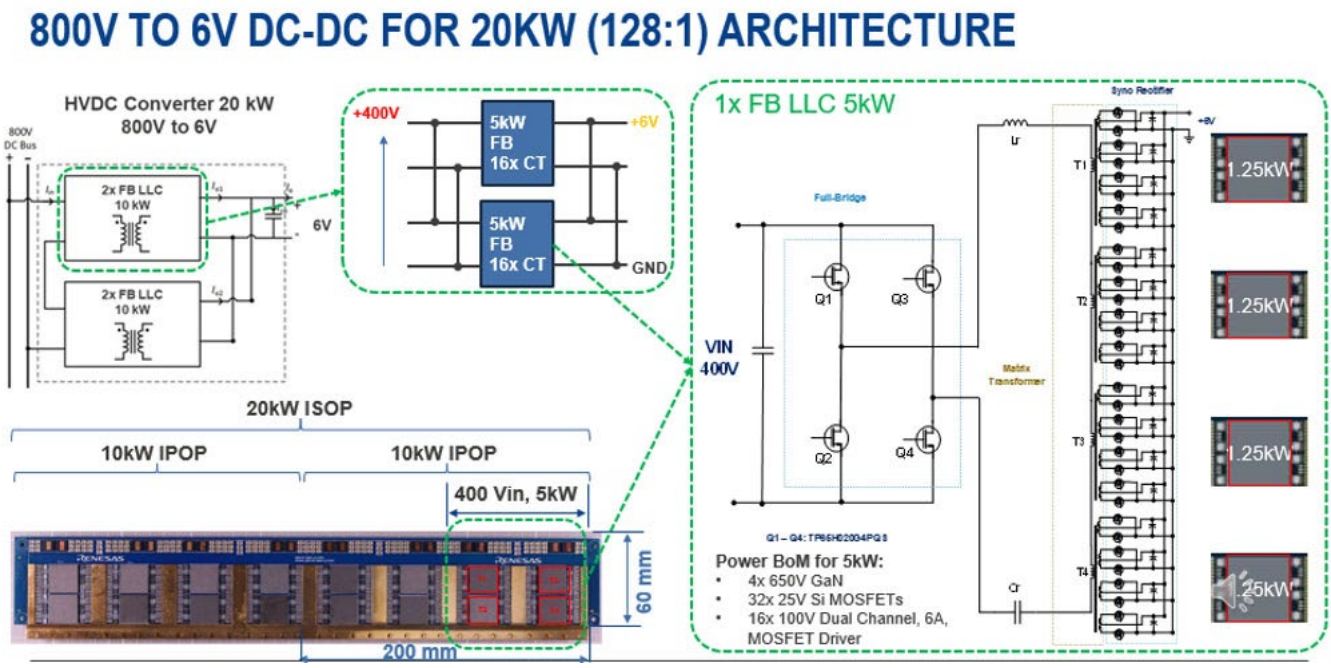


Figure 3. Hierarchical construction of the proposed 20 kW architecture from 5 kW full-bridge LLC modules

800V to 6V, 20 kW DC/DC – Mechanical Requirements

Mechanically, the converter is optimized for deployment inside next-generation compute trays. The complete power stage occupies a maximum area of 400mm × 60mm with a profile of 6.5mm, excluding the horizontal bus-bar structure. Such a compact form factor enables installation directly within Power Delivery Boards (PDBs),

significantly reducing the distance between the power converter and the load. The resulting reduction of Power Distribution Network (PDN) impedance supports Vertical Power Delivery architectures and helps address the rapidly increasing current-density requirements of future xPU AI processors.

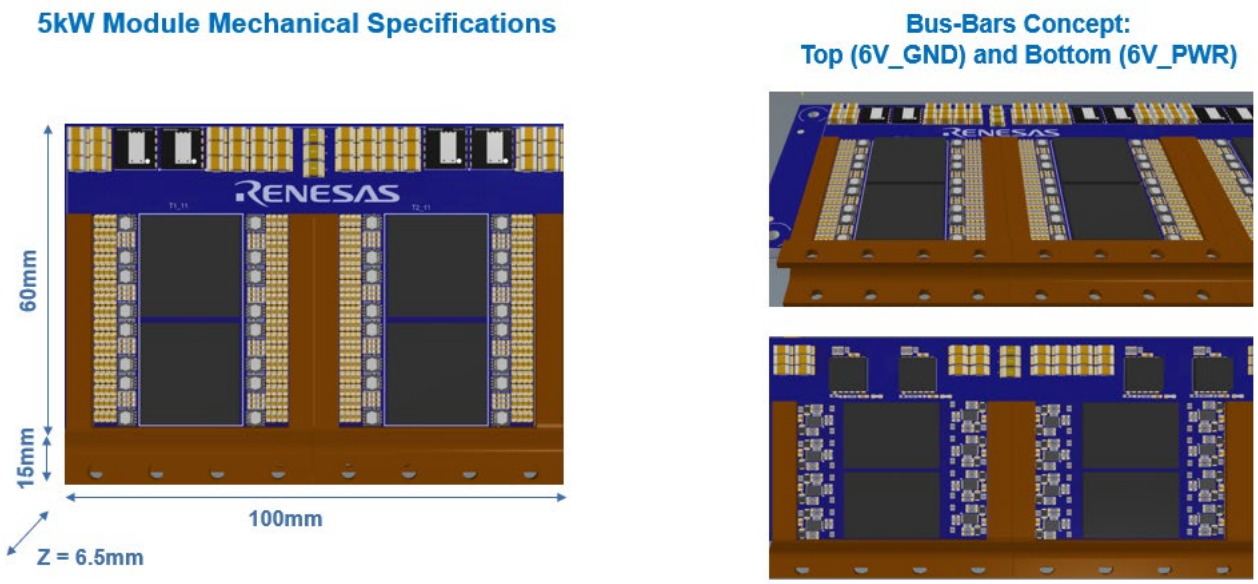


Figure 4. 800V to 6V – 5 kW brick Mechanical Specifications

800V to 6V, 20 kW DC/DC – Matrix Transformer Design Aspects

For ultra-high-power-density LLC DCX converters, planar matrix transformers offer significant advantages over conventional magnetic structures. They enable a more compact design, improved integration and better control of magnetic parameters. In this work, an integrated four-limb matrix transformer was developed in collaboration with magnetic partner Payton Planar Group. The transformer structure was optimized using 3D magnetic simulations in Ansys to minimize both core and conduction losses. Uniform flux distribution and optimized air-gap placement ensure efficient core utilization, resulting in lower losses and improved overall performance.

The 800V-to-6V converter is realized using a full-bridge LLC converter with a center-tapped secondary. The center-tapped structure is selected to meet the voltage rating requirements of the secondary-side devices while optimizing the converter footprint.

The converter uses four matrix transformers connected in series, with each matrix transformer rated for 1.25 kW. Each matrix transformer consists of four limbs and each limb acts as an individual transformer. The windings are arranged such that all four transformers within a matrix transformer are connected in series, resulting in a total of sixteen transformers connected to the full-bridge LLC converter.

This architecture allows the 400V primary voltage of the full-bridge LLC converter to be evenly distributed across all sixteen transformer sections. As a result, each transformer limb sees only 25V, significantly simplifying the planar magnetic design. The reduced voltage per transformer enables the use of a practical 4:1 turns ratio while maintaining high power density and uniform flux distribution throughout the magnetic structure.

Simulation Results – 2.5 kW Transformer

The 400V-to-6V transformer design was evaluated across different switching frequencies while maintaining an overall converter profile height of 6.5 mm.

The layerstack-up and PCB material is chosen carefully to meet the reinforced isolation requirement.

For the selected layer stack, switching frequency has been optimized after considering both skin-effect and proximity-effect losses. To accurately estimate conduction and high-frequency losses, electromagnetic simulations were performed using the actual PCB layout, including routing details, via dimensions and copper plating thickness.

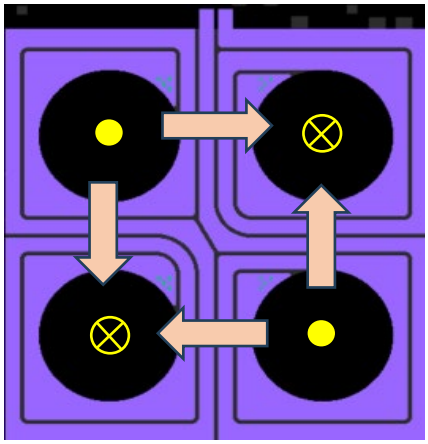


Figure 5. 1.25 kW matrix transformer structure

The simulation model consisted of two matrix transformers connected in series, from which the transformer parameters were extracted. The simulation results for the two series-connected matrix transformers are shown in figures 5 and 6.

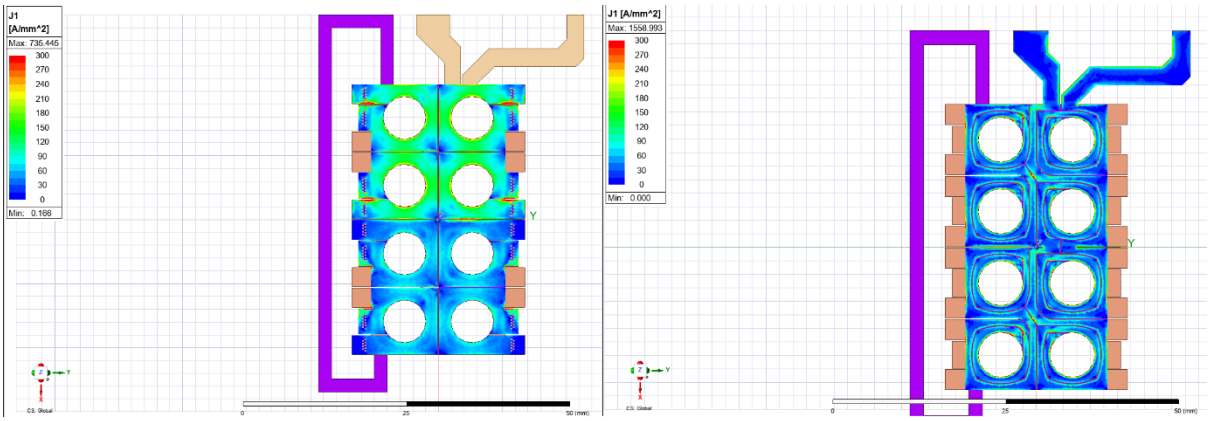


Figure 6. On the primary and secondary of transformer at 5 kW power

Current Sharing

The 400V-to-6V full-bridge LLC converter utilizes four matrix transformers connected in series on the primary side, while all secondary windings are connected in parallel. The series connection of the primary windings inherently forces the same current through all transformer sections, resulting in natural current sharing among the secondary outputs of each full-bridge converter.

The 20 kW 800V-to-6V converter is realized using four 5 kW full-bridge LLC converter modules. Two full-bridge converters are connected in parallel across the upper 400V bus, while the remaining two full-bridge converters are connected in parallel across the lower 400V bus. By connecting the converter modules in series across the 800V input, each full bridge is exposed to only 400V, enabling the use of 650V power devices.

All four converter modules are implemented on a single PCB using identical layouts, routing structures and via arrangements. Maintaining equal impedance paths across all power stages helps achieve balanced current distribution between the full-bridge converters. Because all converter modules share the same PCB environment and operate at the resonant frequency, uniform current sharing is achieved without the need for an active current-balancing control loop. During testing, the switching frequency of each converter module was fine-tuned to ensure operation exactly at the resonant frequency.

In addition to this open-loop current-sharing approach, the design includes provisions for implementing active current balancing. Secondary current can be estimated using the resistance of the output bus bar, enabling current-sharing control between converter modules. The design also provides support for SR MOSFET DCR current sensing on the secondary side, along with temperature measurement for compensation and improved current measurement accuracy.

800V to 6V, 20 kW DC/DC – Digital Power Control

The digital control functionality is implemented on a dedicated controller card based on the Renesas RA6T2 microcontroller. The RA6T2 integrates a 240MHz Arm Cortex-M33 core together with high-resolution PWM peripherals specifically intended for digital power applications. The controller board provides all converter-management functions, including resonant converter control, monitoring, fault supervision, startup sequencing, system telemetry and communication. Standard interfaces including isolated UART, SPI and CAN are supported, enabling straightforward integration into future rack-level management architectures and allowing communication with external supervisory controllers.

External interface diagram of 800V to 6V Digital power controller is illustrated in the Figure 8. RA6T2 Digital power controller mainly interacts with power stage and external GUI. The controller's Pulse Width Modulation (PWM) module generates the gate-drive signals required for the primary and secondary power switches (GaN FETs). These gate pulses are produced according to the configured switching frequency and control algorithm requirements to regulate power transfer through the LLC resonant converter. To ensure safe operation of the power stage, the PWM peripheral incorporates dedicated hardware dead-time insertion circuitry, which prevents simultaneous turn-on of complementary switches and protects the converter against shoot-through conditions. ADC module of the digital controller acquires analog signal data to convert it to digital format. This digital data is used for control, protection and telemetry purposes. It also has dedicated GPIOs to transmit/receive the commands. Communication modules of the digital power controller are used to interact with external world for firmware update, telemetry and parameter configuration. In the present 800-6V converter, the RA6T2 controller UART module has been used for telemetry and configuration of parameters.

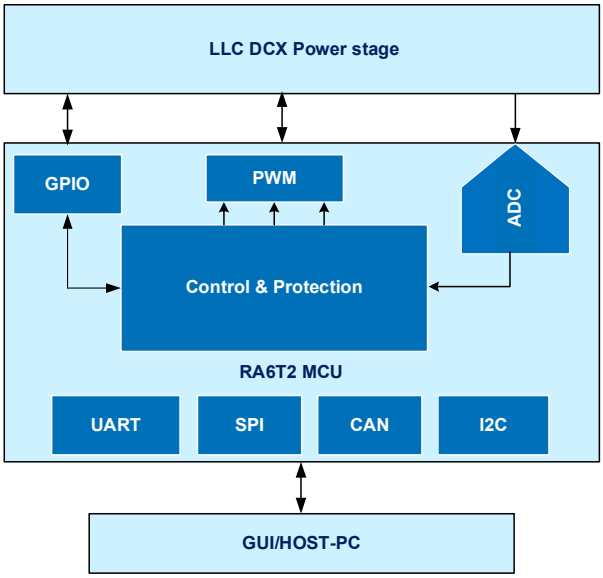


Figure 7. External interface diagram of digital power controller

Overall, the RA6T2 digital power controller acts as the intelligence hub of the converter, coordinating power-stage control, data acquisition, protection mechanisms and user interaction through its integrated peripheral set. Controller board developed for 800V to 6V LLC DCX converter is shown in 9

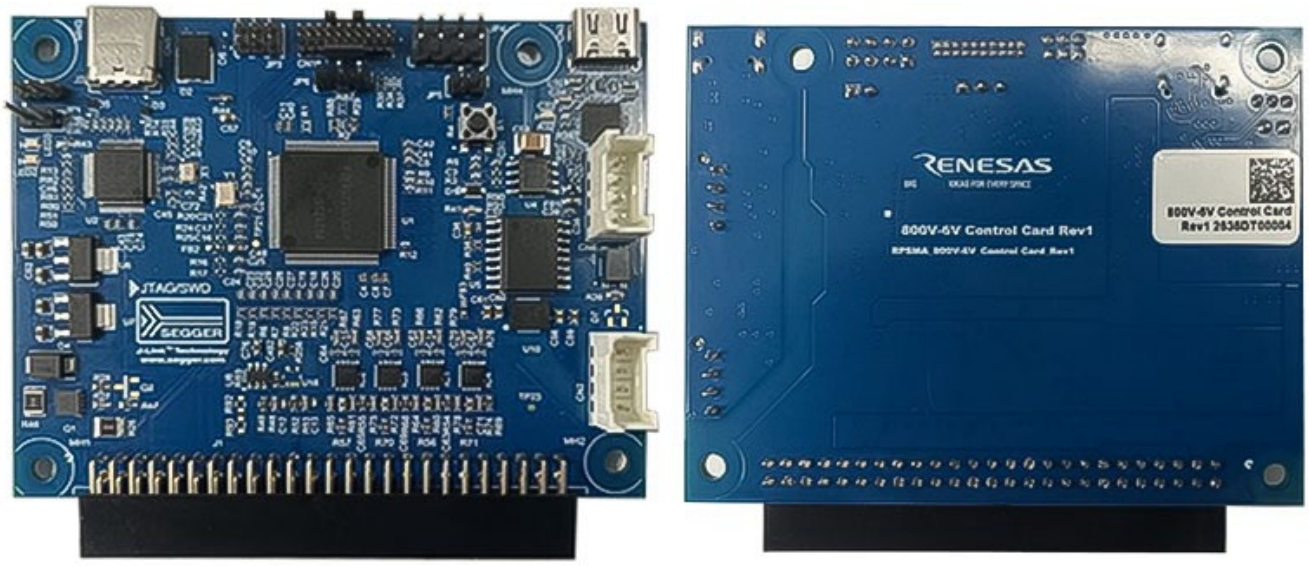


Figure 8. RA6T2 digital controller card

The firmware developed for the platform leverages the digital nature of the LLC DCX topology. Since the converter operates as a fixed-ratio Direct Current Transformer (DCX) near its resonant frequency, complex high-bandwidth voltage-regulation loops are not required. Instead, the embedded software focuses on system supervision, protection management, telemetry acquisition, parameter configuration and power-stage management. This significantly reduces control complexity while preserving the flexibility to implement future

enhancements such as module synchronization, interleaving optimization, active current sharing, diagnostics and predictive maintenance functions.

The 800V to 6V LLC DCX firmware is structured using a layered architecture consisting of a Hardware Support Layer (HSL) and an Application Layer. This modular approach enables the application layer to be developed independently of the underlying microcontroller (MCU) platform, significantly simplifying firmware portability across different digital controllers and reducing development effort and migration time.

The Hardware Support Layer interfaces directly with the digital power controller peripherals and hardware resources, providing a standardized abstraction layer to the application software. This abstraction isolates application functionality from device-specific implementation details, thereby improving code reusability, maintainability and scalability.

The Hardware Support Layer has been developed using the Renesas Flexible Software Package (FSP), which offers a comprehensive and user-friendly framework for peripheral configuration, driver development and system integration. Leveraging FSP accelerates firmware development while ensuring a consistent and robust interface between the hardware and application layers.

The application layer is further organized into multiple functional modules, each responsible for a specific aspect of the LLC DCX converter operation. This modular software architecture improves maintainability, scalability and code reusability while enabling independent development and testing of individual functionalities.

The **Control Module** forms the core of the LLC DCX firmware and is responsible for managing all converter operating states and power-stage control functions. It executes the startup and shutdown sequences, ensuring safe converter operation during power-up, power-down and fault recovery conditions. During startup, the module performs frequency ramping and soft-start functions to limit inrush currents and prevent excessive stress on the resonant components and power semiconductor devices.

In addition, the Control Module offers a configurable framework that may support further refinement of converter operation in areas such as those outlined below.

- **Switching-transition management**
- **Operating-point management**
- **Secondary-side switching coordination**

By continuously monitoring system operating parameters and coordinating control actions, this module ensures stable, efficient and reliable power conversion.

The **Protection Module** is dedicated to system protection and fault management. Its primary responsibility is to safeguard the LLC DCX converter against abnormal operating conditions that could compromise system reliability or damage power-stage components.

The module continuously supervises critical system parameters and provides comprehensive protection mechanisms including:

- Output overvoltage protection (OVP)
- Output overcurrent protection (OCP)
- Input voltage fault detection
- Overtemperature protection (OTP)

Upon detection of a fault condition, the Trip Module initiates the appropriate protection response, such as controlled shutdown, fault latching, or automatic restart based on system requirements. The module also records fault status information, enabling diagnostics and troubleshooting during system validation and field operation.

The **Communication and User Interface Module** provides the interface between the converter firmware and external configuration, monitoring and diagnostic tools. This module utilizes the UART services provided by the Hardware Support Layer to establish reliable communication with a graphical user interface (GUI) or host controller.

Key functions of this module include:

- Real-time monitoring of converter operating parameters
- Configuration of control and protection settings
- Parameter tuning and calibration
- Fault reporting and event logging

This module enables users to configure system parameters, monitor converter performance and perform firmware maintenance without requiring modifications to the core control software. As a result, it enhances usability, simplifies product commissioning and supports efficient field updates and diagnostics.

Together, these software modules provide a robust, scalable and platform-independent application framework that enables high-performance control, comprehensive protection and flexible system management for the 800V to 6V LLC DCX converter.

800V to 6V, 20 kW DC/DC – Efficiency and Loss Model

Beyond power density, efficiency remains a primary design objective. Simulation and design analysis indicate an efficiency target exceeding 96% at the full 20 kW operating point. Detailed loss analysis shows that the dominant losses originate from transformer copper resistance and secondary-side conduction, while the primary-side GaN switching stage contributes only a small percentage of total converter losses due to the effectiveness of resonant operation and soft-switching techniques.

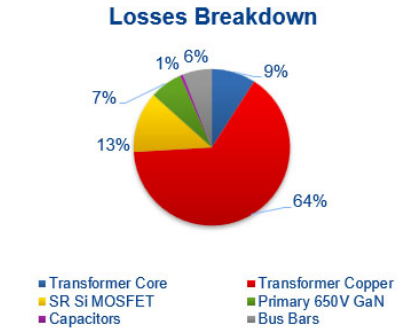
Total converter losses are estimated at approximately 764 W at full power, corresponding to a projected efficiency of approximately 96.3%.

Excluding gate-drive losses, the model reports 744.43 W and 96.41%.

Loss group	Loss (W)	Share of modeled loss	Observation
Transformer core	69.6	9.1%	Magnetic material and frequency
Transformer copper + shield	496.0	64.9%	Dominant optimization opportunity
Secondary MOSFETs	96.4	12.6%	Conduction and drive losses
Primary TP65H020G4PLSGBD 650V GaN	51.26	6.7%	Primarily conduction loss
Capacitors	4.83	0.6%	Resonant, input and output capacitors
Bus bars	45.76	6.0%	Critical at kiloampere output current

Table 2. Analytical loss breakdown for the proposed 20 kW converter, percentages are rounded

Efficiency Estimation Summary	
Loss Total [W]	763.8
Efficiency [%]	96.3
Loss Total (W/O driving) [W]	744.4
Efficiency (W/O driving) [%]	**96.4**



Loss break down of Renesas 800V-6V 20kW LLC DCX module		
Block/Component	**Loss [W]**	**Note**
Transformer		
Core	69.6	Ansys Simulation
Primary + Shield	496	Ansys Simulation
Secondary		Ansys Simulation
Total Transformer	**565.6**	
Sec MOSFET		
SR cond	68.94	0.42mOhm Max
SR Driving	18.78	Vgs 10 V (6.5V to 7V)
Body Diode Losses	8.68	
Total SR (25V Si)	**96.4**	
Primary 650V GaN		PN: TP65H020G4PLSGBD, 22 mΩ - PQFN8X8
GaN cond	50.08	650V Renesas GaN, 20mΩ (TYP)
GaN Eoff	0.57	
GaN Driving	0.61	Vgs pri=8.5V
Total Primary (650V GaN)	**51.26**	
Caps		
Cr Cap	0.55	10mOhm ESR
Input cap	4.15	10moHm ESR
Output cap	0.14	
Total caps	**4.83**	
Bus Bar losses	**45.76**	

Figure 9. Original engineering loss model and efficiency-estimation summary

Complete 800V-to-6V LLC DCX Demonstration Platform

To accelerate development and validation of the 800V-to-6V 128:1 LLC DCX architecture, Renesas implemented the Proof-of-Concept as a complete hardware and software evaluation platform rather than as a standalone power stage. The system consists of three tightly integrated elements: an input interface board, a dedicated digital control card and the 20 kW power module, all supported by embedded firmware and a graphical user interface (GUI). This approach enables rapid evaluation, telemetry collection, parameter optimization and system-level characterization while providing a reusable framework for future high-voltage AI power architectures.

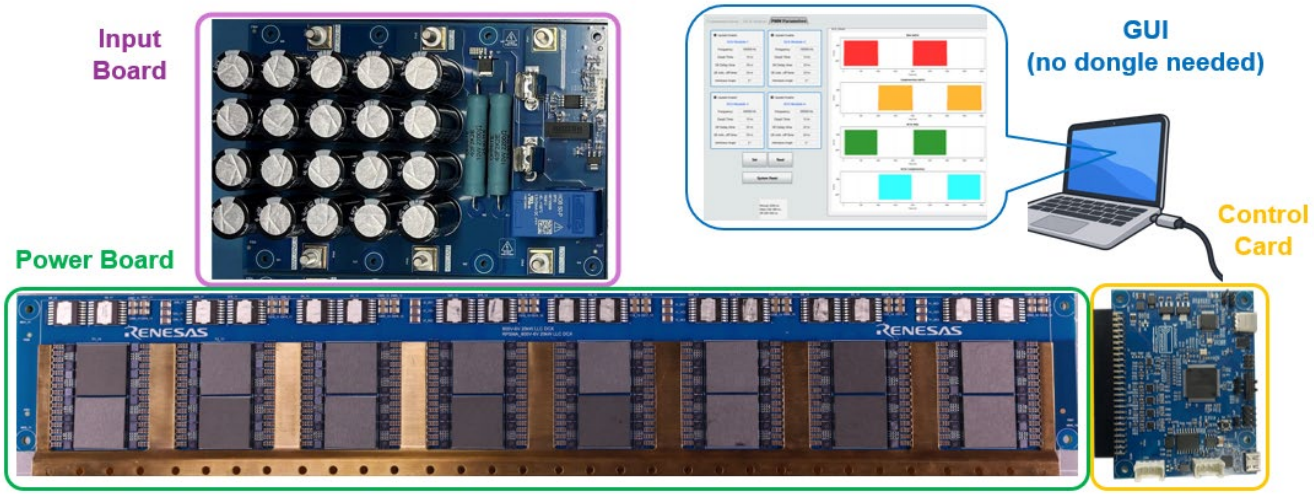


Figure 10. 800v to 6V DCX POC platform

The input board interfaces directly with the 800V LVDC distribution bus and provides the energy-storage, sensing and protection functions required for safe operation of the converter. The board incorporates twenty 100 µF electrolytic capacitors to form the high-voltage bulk capacitor bank, together with passive discharge circuitry and fuse protection to ensure safe startup and shutdown of the platform. Hall-effect current sensors are used to monitor input current, enabling accurate power measurement, converter characterization and over-current

protection. This dedicated front-end stage allows the power converter to be evaluated under realistic AI infrastructure operating conditions while maintaining the safety requirements associated with an 800V environment.

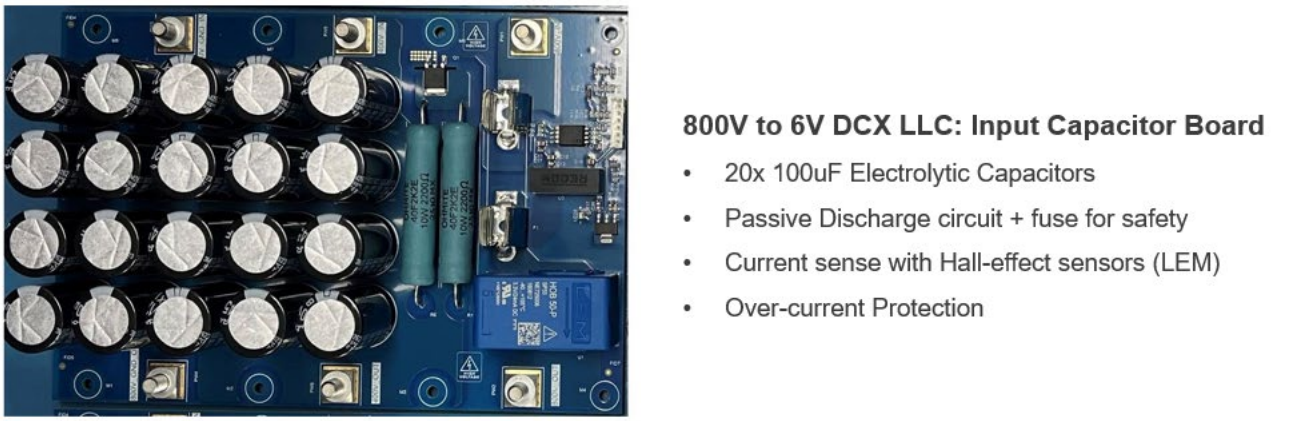


Figure 11. 800V to 6V DCX LLC input capacitor board details

As described in greater detail above, a dedicated control card based on the Renesas RA6T2 manages converter operation, startup, protection, telemetry and communications. Its embedded firmware supports system supervision and parameter configuration, with isolated UART, SPI and CAN interfaces for laboratory and rack-level integration. To complement the hardware platform, a dedicated PC-based graphical user interface was developed. The GUI provides direct access to converter settings, operating parameters and real-time telemetry without requiring external communication dongles. Through the interface, developers can monitor operating conditions, evaluate converter behavior, configure system parameters and capture performance data during laboratory testing. The GUI transforms the power stage into a complete development environment, significantly reducing debug and optimization effort during evaluation of new converter configurations and magnetic designs.

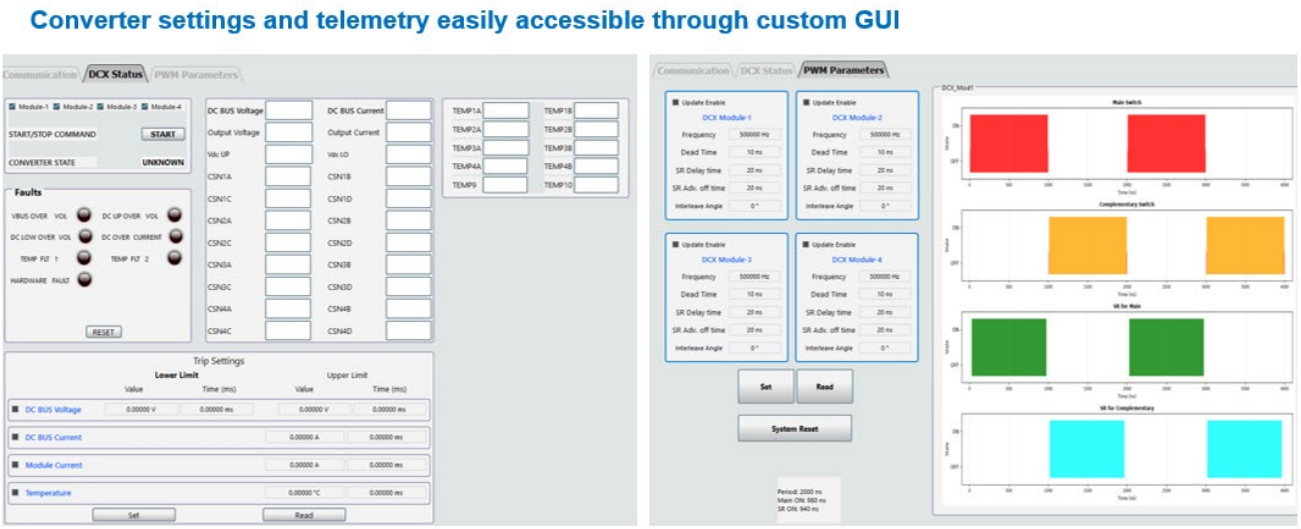


Figure 12. 800v to 6V DCX POC GUI menu

Together, the input board, digital control card, embedded firmware and graphical user interface create a complete evaluation ecosystem for the 800V-to-6V LLC DCX architecture. Beyond demonstrating the feasibility of direct 128:1 conversion, the platform provides the instrumentation and software infrastructure necessary to

characterize efficiency, thermal behavior, transient performance and scalability, creating a foundation for future deployment of high-density 800V power delivery solutions in next-generation AI compute racks.

Conclusion

As AI rack power and processor current continue to rise, efficient high-voltage distribution must be matched by an equally efficient conversion architecture inside the compute tray. Direct 800V to 6V conversion offers a path to potentially eliminate intermediate 48V and 12V stages from the xPU power chain, retain the benefits of high-voltage rack distribution and generate a low-voltage rail close to the load for emerging vertical power-delivery and integrated-regulator architectures.

The Renesas proof of concept translates this system concept into a modular 20 kW, 128:1 LLC DCX built from four 5 kW full-bridge cells. The combination of TP65H020G4PLSGBD 650V GaN primary switches—delivering 20 mΩ on-resistance in a compact 8×8 mm PQFN package—series-connected planar matrix transformers, low-voltage synchronous rectification, resonant soft switching, integrated current paths and RA6T2-based digital control supports a compact implementation targeted at greater than 96% efficiency. An integrated input card, protection and sensing functions, embedded firmware and a PC-based GUI extend the converter into a complete development platform for configuration, telemetry and system characterization.

The work demonstrates a practical and scalable route for bringing an isolated 6V source directly into future AI compute trays. The analytical results establish the feasibility of the approach and identify transformer copper, shielding and high-current secondary conduction as the principal optimization areas; prototype testing will now be essential to confirm efficiency, thermal performance, current sharing, protection behavior and transient response under representative operating conditions.

References and Source Material

[1] Renesas Electronics, “Power Architecture Evolution in Data Centers,” 2025 white paper.

[2] Renesas Electronics, “Why AI's Next Growth Phase Is Redefining Data Center Infrastructure”, June 2026.

[3] Open Compute Project, “Data Center Facility – Low Voltage Direct Current Power Distribution.”

[4] Renesas Electronics, RA6T2 Group product documentation.

[5] Renesas Electronics, “Renesas Unveils Industry's First 650V GaN in Dual-Side Cooled 8x8mm Package for Megawatt-Scale AI Data Centers”;

[6] Payton Planar, “High-Density Power for AI & Cloud: Planar Magnetics in Data Centers”,

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