White Paper

ASi-5 Empowers Industry 4.0 Applications with Tons of Features and Easy Integration Options

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Abstract

Industrial automation devices nowadays are required to handle more data than ever before. Whereas legacy implementations just focus on data that is required for the actual processing tasks, today's devices process auxiliary information for configuration, diagnostic, alarm reporting, parameterization, and more. Modern communication systems are needed to handle different levels of information needs. The Actuator-Sensor-Interface version 5 (ASi-5) facilitates mechanisms to support this information processing, while meeting the reliability of legacy systems and increasing cycle time performance. As ASi-5 is a real bus system, it offers tremendous flexibility in the cabling installation which leads to overall low system cost. The ASI4U-V5 silicon solution offers an all-in-one system solution for ASi-5 that ensures the easiest integration option to enable ASi-5 in all modes defined by the ASi-5 specification

This white paper explores some of the technical details of the ASi-5 technology and outlines how those are implemented in the ASI4U-V5 silicon solution.

About ASI4U-V5

Renesas has contributed its know-how in transmission methods and semiconductor technology to the definition of the ASi-5 standard and the technical implementation in a silicon solution. In analog technology in particular, a highly robust state-of-the-art technology has been implemented with a great deal of innovation.

In addition to the ASI4U-V5 semiconductor, the development alliance also provides verified firmware for the IC. This simplifies the ASi-5 implementation enormously, as developers do not have to deal with the internals of the ASI4U-V5 chip. All the chip functions are encapsulated by the firmware. The firmware covers the two device implementations defined in the ASi-5 standard (see figure 1). With the simple device, process data is only transferred to the chip via digital I/Os and successively via the ASi-5 protocol.

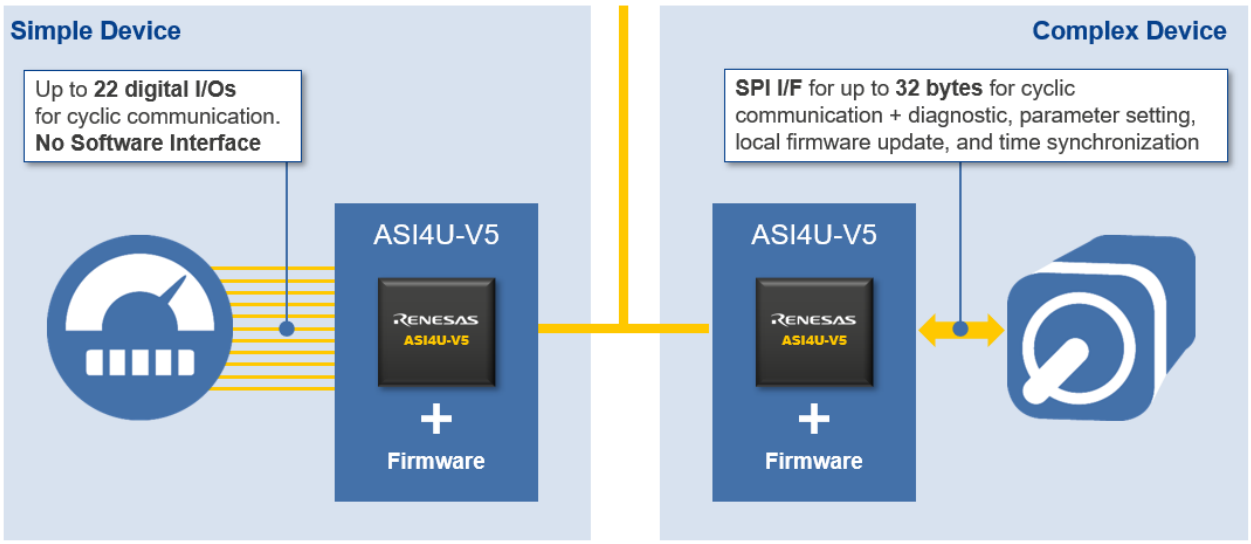

Figure 1: ASi-5 Device Options

In contrast, the IC is served via the SPI interface in the complex device mode. Here, up to 32 bytes per cycle are exchanged, which enables complex application scenarios and makes the extended functionality of ASi-5 accessible.

ASi-5 Transmission Features

Transmission technology

Compatibility to legacy ASi implementation has been a key requirement for the specification of ASi-5. To ensure compatibility with ASi-3 on the same cable, the development team decided to transmit the ASI-5 data in a frequency spectrum above the ASi-3 channel. ASi-3 uses a time-division multiplex method to exchange data sequentially within a cycle time of 5ms with a maximum of 31 slaves (62 slaves with A/B addressing). ASi-3 occupies a frequency band from 50 kHz to 500 kHz. ASi-5 data is modulated between 2 and 8 MHz in the actual implementation. Here, an orthogonal frequency division multiplex method is used. This means that the frequency band is divided into many sub bands, each of which is used to transmit a separate data stream.

With ASi-5 these frequency bands have a spacing of 58.59 kHz. In regular operation, at least 136 of these channels are available for ASi-5 communication. In each of these channels, a time division multiplex method is used to transport data from the master to the slaves within 1.2ms first, and then data from the slaves to the master. The modulation method used is the Differential Quadrature Phase Shift Keying (DQPSK). With DQPSK, two data bits are transmitted per transmitted symbol.

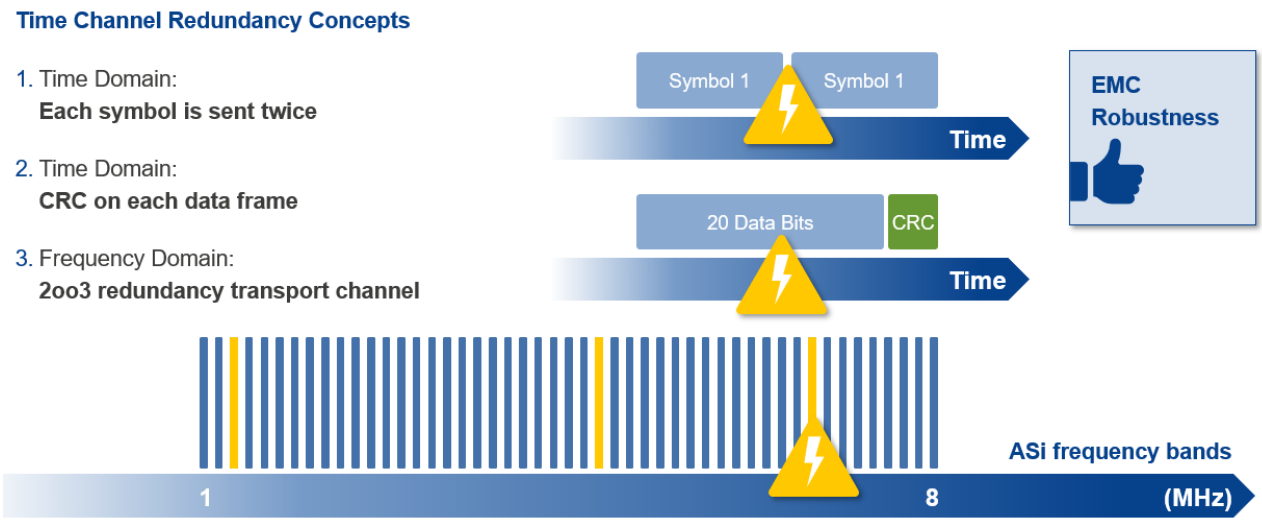

Figure 2: Unmatched EMC Robustness

Unmatched EMC robustness

Every 20 bits that are transmitted bi-directionally per cycle and per data channel are secured by a cyclic redundancy check (CRC), so that errors can be effectively identified. Each process data transmission takes place on three channels simultaneously. The receiver must receive the same data on at least two channels to recognize the process data as valid (2oo3 protection). An additional safeguard is that each symbol is transmitted twice in succession, which additionally protects against short-term electromagnetic interference. Three different methods are therefore used to protect data transmission against external interference. All in all, this leads to stable data transmission, even under unfavorable transmission conditions.

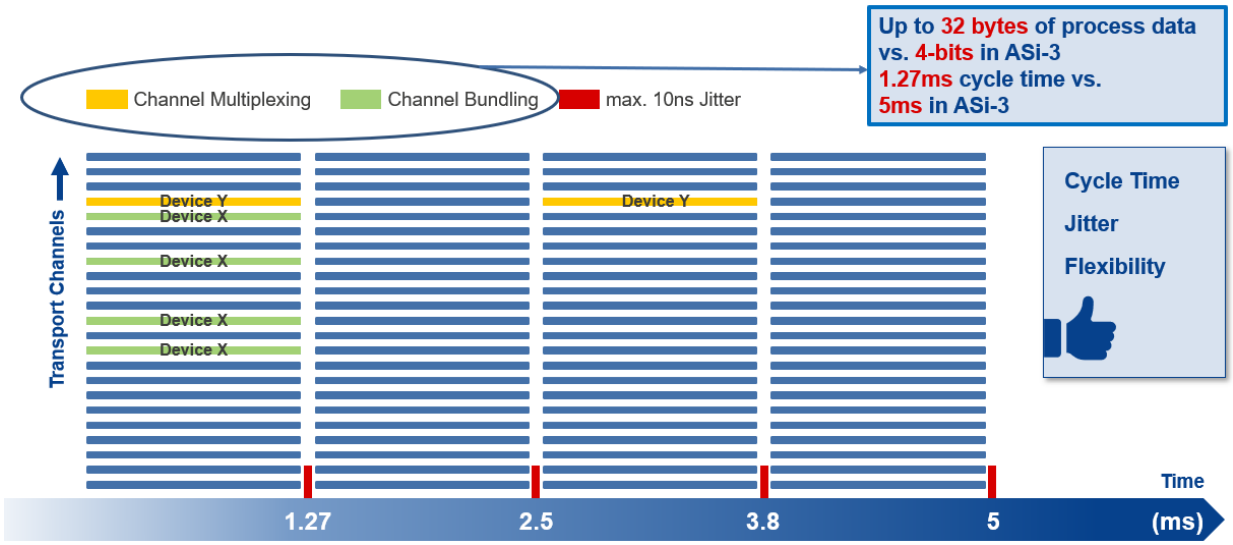

Figure 3: Sub-cycles / Channel Bundling & Multiplexing / Jitter

Application-dependent bus configuration

Figure 3 depicts that up to 24 logical transmission channels can be handled in a 1.2ms cycle. This means that up to 24 slaves can be addressed. If more slaves are to be connected, they can share the same transmission frequencies by means of a time division multiplex procedure. This allows cycle times of 2.5ms, 3.8ms, or 5ms to be achieved, resulting in a maximum connection of 48, 72 or 96 slaves.

Flexibly configurable data rates per network node

If more than 16-bit I/O data is to be transmitted per cycle, this can be achieved via channel bundling and multiplexing. Channel bundling connects several channels in a sub-cycle. With multiplexing, several channels are connected over several sub-cycles. In this way, up to 32 bytes can be exchanged in one cycle.

In addition to cyclic data, there is an asynchronous channel called the asynchronous management channel (AMC). This channel couples four carrier frequencies for communication and is designed with 5-fold redundancy. The AMC thus occupies 20 carrier frequencies. The initial activation of the slaves is negotiated via the AMC. In addition, the AMC enables many new mechanisms such as diagnostics and parameterization.

ASI4U-V5: The ASi-5 Silicon Solution Transmission Features

Functionality and Interfaces

All ASi-5 requirements are mapped into the ASI4U-V5 silicon solution. Customers can concentrate on the correct connection of the respective application, allowing easy integration of the ASi-5 transceiver. Figure 4 shows connections to the chip in typical applications.

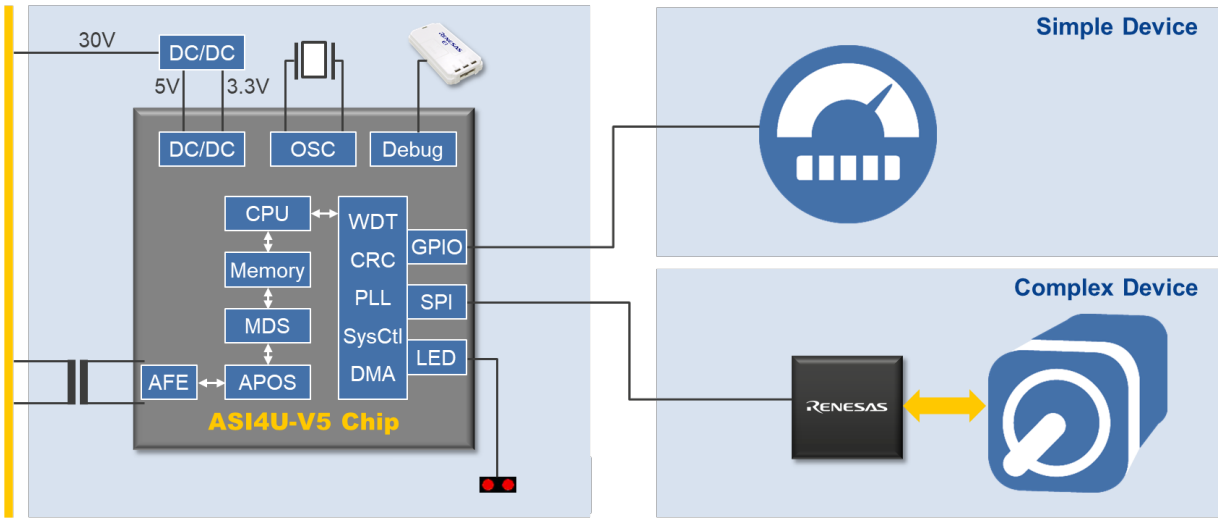

Figure 4: Main Interfaces and Application Examples

The firmware is stored chip-internally in non-volatile memory. Application-dependent ASi-5 configurations are stored by the sensor/device manufacturer via a debug interface in designated programmable flash memory locations and are interpreted accordingly by the firmware.

The ASi-5 signals on the line are coupled to the chip's internal analog, power and oscillator block (APOS) via a transformer. In the APOS block, the signal for the high-precision analog-to-digital converter is provided in the receiver unit via various amplifier stages and signal filters. After the analog-to-digital converter, a digital block demodulates the signal and stores the demodulated data in the internal memory. A burst detector detects when the receive path is overdriven by external interference and marks the resulting erroneous data. This can then normally be recovered using the mechanisms described above.

The internal CPU takes over all further processing steps. In the opposite direction, the sending is then implemented analogously. The CPU stores the data to be sent in the internal memory. The modulator unit digitally modulates the signal and transfers the data values to an analog-to-digital converter in the APOS. The further signal path runs via the impedance converter and filter to the line driver, which transmits the signals on the ASI line.

The supply voltage is derived from the 24 V to 30 V of the ASi line. In addition, four other voltages are generated via internal LDOs in the chip.

In simple device applications, up to 22 I/O data are directly connected to the corresponding application via GPIOs. The GPIOs are directly coupled to the corresponding ASi-5 transport channels. For the overall system to function, only the corresponding configuration needs to be stored in the flash of the ASI4U-V5 device. All simple device specific properties can be configured via the on-chip configuration sectors. During operation, the application does not require any software components to address the ASI4U-V5 device. This makes the simple device mode extremely easy to implement.

In contrast, the application interface in complex device mode is the SPI interface of the chip. Also in complex device mode, is the complexity of the device encapsulated by the firmware. In this mode, up to 32 bytes of process data can be transferred per cycle. In contrast to the simple device, it is possible to serve diagnostics and event handling via the SPI interface. An LED interface independently controls the status LEDs in accordance with the standard.

Conclusion

ASi-5 supports industry 4.0 applications with an extensive feature set. It supports real-time communication, as well as auxiliary functionality like parameterization, diagnostics, and alarm reporting. The transmission technology is state-of-the-art and extremely robust. With the ASI4U-V5, Renesas provides a component that reduces the integration effort of an ASi-5 interface to a minimum. The implementation of the complex transmission method is optimally distributed between hardware and firmware components. In simple device application, the chip is only supplied with process data. The compact, power-saving design enables the development of even the smallest sizes. Uniform firmware guarantees the interoperability of ASi-5 components, while compatibility with ASi-3 allows easy expansion of existing installations. Next to the chip, the firmware and the development board, Renesas provides extensive documentation of the silicon solution and its applications.

Renesas provides the silicon in a 64-pin QFN package (9 x 9 mm, 0.5 mm pitch), which consumes less than half a watt in a typical application. It supports a temperature range of -40°C to 85°C. Renesas also provides reference circuits. IC samples and starter kits are available.

Learn More

- ASI4U-V5 Fully Compliant ASi-5 Transceiver ASSP