Principles of the Driver and Receiver in RS-485 Networks

RS-485 is a well-known communication standard that is effective for long-distance data transmission and environments with substantial electrical noise. This tutorial provides a clear and detailed explanation of the driver and the receiver—key components of RS-485 networks that ensure the integrity and efficiency of data communication.

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1. Driver

The output structure of the RS-485 driver is a complex system designed to handle data transmission efficiently and safely. This structure features an H-bridge driver configuration that consists of high-side and low-side transistors for each Y and Z output. These transistors are complemented by electrostatic discharge (ESD) cells on each terminal to protect against voltage spikes. An essential part of this structure is the inclusion of diodes in series with each transistor. These diodes prevent reverse current flow by (1) stopping current from flowing back from the bus terminals to the power supply when the voltage on Y or Z exceeds VCC and (2) stopping current from ground to the bus terminals when the voltage is below ground potential.

Essentially, the driver output is a waveform that combines both positive and negative differential voltages on top of a common-mode offset voltage, which usually amounts to half of the supply voltage (VCC/2). According to the RS-485 standard, the driver must be able to produce a differential output voltage of more than 1.5V across a 54Ω load. To achieve this, the on-resistance of both high-side and low-side transistors is kept low, typically between 20Ω and 30Ω, to supply enough current for this voltage level. The standard also requires the driver to maintain this output voltage with a 60Ω differential load and a common-mode load of 375Ω, accommodating a range of voltages from -7V to +12V.

Another critical feature of the RS-485 driver is the control of the output rise and fall times. This control is managed by a separate circuit that switches the transistors Q1, Q2, Q3, and Q4. The speed of these transitions determines the maximum data rate of the transceiver. Ideally, the rise and fall time should not exceed one-third of the total bit time for a given data rate. In practice, transceivers with slower rise and fall times are preferred over those with faster times, because slower rise and fall times generate less electromagnetic interference (EMI) reducing the impact on adjacent circuitry.

This combination of a large differential output voltage and a broad common-mode range differentiates the RS-485 from other signaling standards. With a robustness and versatility, the RS-485 is suitable for challenging electrical environments such as those found in industrial automation, e-metering, and motor control applications.

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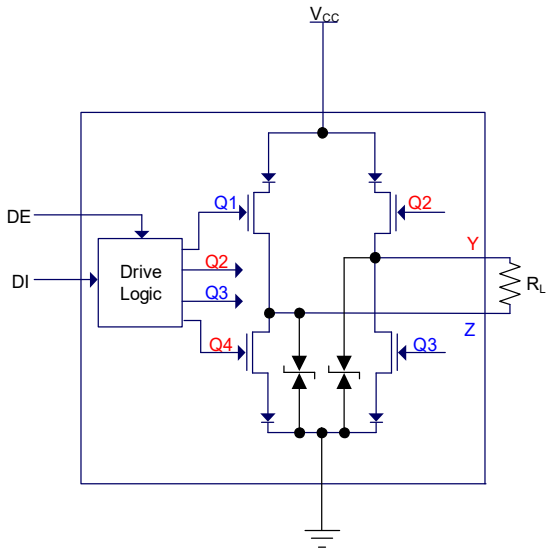

Figure 1. Circuitry of a Driver

2. Receiver

The input circuitry of the RS-485 receiver, crucial for proper functioning, includes an electro-static discharge (ESD) protection, a resistor-divider network, and a biasing current. These components combine to manage the magnitude and common-mode voltage as they reach the differential comparator for signal processing.

For ESD protection, the design differs based on the type of transceiver. In half-duplex transceivers, the driver and receiver share the same ESD protection, optimizing space usage. In contrast, full-duplex transceivers require independent ESD protection for both the driver (Y and Z pins) and the receiver (A and B pins), which doubles the space required for this protection.

The resistor-divider network on the A and B inputs, consisting of components such as R_B and R_{IN}, serves two primary functions. The first primary function is that the network attenuates signals that are beyond the supply voltage range of the receiver. This attenuation is necessary because the RS-485 standard allows for bus terminal voltages from -7V to +12V, which occur as a result of differences in ground potential between devices on the same network. Typically, the network reduces these voltages to a level manageable by 3.3V or 5V transceivers and by a factor of approximately 10-to-1. The series combination of R_{IN} and R_B || R_B (where resistors R_B are parallel) is critical because it determines the input impedance of the receiver.

The second primary function of the resistor-divider network is to bias the bus voltages toward VCC/2. The biasing is important because simply attenuating a negative signal is insufficient to align it within the operating range of the local ground of the receiver and VCC. By attenuating the signal and biasing it, the network prevents the comparator inputs from becoming saturated, ensuring accurate differential voltage evaluation between terminals A and B. Also, this design allows for operation without a common-ground connection between the remote ground of the RS-485 driver and the local ground of the receiver.

A critical design aspect of the resistor-divider network is balancing the reduction of input leakage current with the management of resistor values. High resistor values are required to lower leakage current, but this increases the size of the components in the attenuator, leading to higher costs and more parasitic capacitance. This capacitance, combined with the input capacitance of the comparator, forms a low-pass filter that limits the maximum bandwidth of the receiver. Therefore, designers must balance reducing input leakage current with managing resistor values, while considering bandwidth and the size of the attenuator. Especially with voltages between -7V and +12V, this careful balancing act is vital for the RS-485 receiver to function effectively in challenging electrical environments.

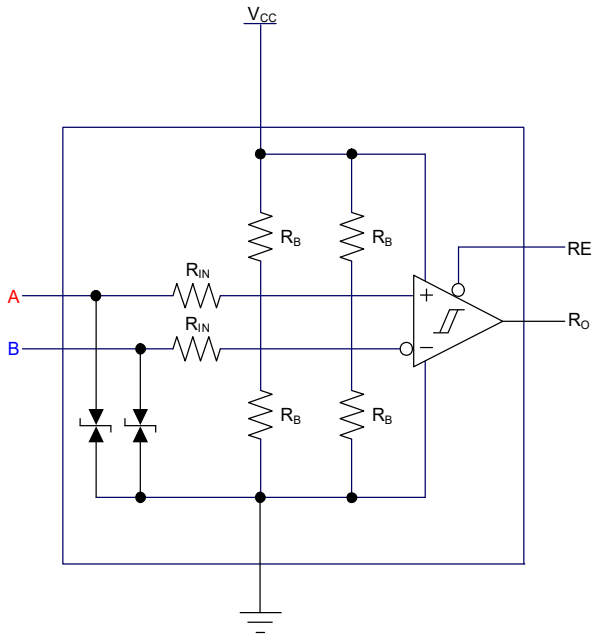

Figure 2. Circuitry of a Receiver

3. Revision History

Revision	Date	Description
1.00	Dec 18, 2023	Initial release.

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