

MAEC TOOL NEWS: MAECT-M3062PT-EPB_2-030216D

Free-of-Charge Upgrade of the M3062PT-EPB Emulation Probe Fabricated as ES and Specific Products

We inform you of the free-of-charge upgrade of the M3062PT-EPB emulation probe fabricated as ES and specific products. (It is the PC7501-dedicated emulation probe for the M16C/62P MCU in the M16C/62 group of the M16C/60 series.)

1. Products Concerned

Product Type	Serial numbers
M3062PT-EPB (ES product)	Labeled "ES TOOL" Total 51
M3062PT-EPB (specific product)	2JS0001--2JS0025 Total 25
	2KS0026--2KS0050 Total 25
	2LS0051--2LS0150 Total 100
	Grand Total 201

2. Descriptions of Upgrade

Your M3062PT-EPBM board can be replaced with the type of new board on which a production-run MCU is mounted from March 10, 2003.

The upgraded product resolves the following problems concerning the MCU's operation:

(1) RAM data at DMA transfer

PROBLEM : If the following conditions are met, RAM data may be rewritten unintentionally.

Condition 1 : The wait bit (bit 7 of 000516) of Processor Mode Register is set to "0", and then the internal memory is used without wait.

Condition 2 : DMAC is used to transfer write-data to the internal RAM

(2) I2C function

PROBLEM 1 : If the STSPSEL bit (SCL, SDA output select bit) of UARTi (i=0 to 2) Special Mode Register is set to 1, start/stop condition generation/completion interrupts may not be generated.

PROBLEM 2 : If the transmit interrupt cause select bit (UiIRS; i = 0,1,2) is set to 1 (transmit is completed) with clock delay (CKPH = 1) in I²C mode, interrupt requests occur even before the transmit starts.

(3) CTS/RTS separate function in UART0

PROBLEM : When the CTS/RTS separate function is set, CTS1 input affects UART1 transmit operation.

(4) Low-voltage detection circuit

PROBLEM : When the VC26 and VC25 bits are both set to 1, if a low-voltage reset occurs in other than STOP mode, the VC25 bit is cleared immediately and the RAM retention limit monitor during low-voltage reset is not performed.

(5) DMA0 request cause select

PROBLEM : If DMA transfers are performed triggered by INT0 input when both edges of INT0 pin were selected with the DMA0 Request Cause Select Register, the DMA transfers are affected by the INT0 interrupt polarity select bit.

3. How to Upgrade the Current Product

- (1) Please copy and fill in the application form and send it to us by e-mail or fax.
- (2) We will ship the new M3062PT-EPBM board by return.
- (3) Replace your current board with the new one following the replacement manual included with the new board.
- (4) Confirm the operation of the upgraded product; then send the previous board(s) listed below back to us.

ES product : an M3062PT-EPBM board or an M30620T-EPBM board

Specific product : two boards of M3062PT-EPBM and M3062PT-EPBD

SEND TO:

Your local Renesas Technology sales office or distributor

4. Effective Date of Application

From February 16, 2003, to September 30, 2003, inclusive

Note:

If there are many applications, the shipment will possibly be delayed.

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