[Revisions to documents]
E1/E20 Emulator Additional Document for User's Manual (Notes on Connection of RH850/D1L and RH850/D1M) Rev2.00

R20TS0013EJ0100
Rev.1.00
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Outline

Errata of E1/E20 Emulator Additional Document for User's Manual (Notes on Connection of RH850/D1L and RH850/D1M) Rev2.00

1. Relevant Document

Title: E1/E20 Emulator Additional Document for User's Manual
(Notes on Connection of RH850/D1L and RH850/D1M)

Doc Number: R20UT3120EJ0200

Revision: Rev2.00

2. Errata

The items below are to be added to section 4.2, Cautionary notes on debugging.

(1/3)

No.		
1	Item	Hardware break [Read/write access cannot be detected]
	Content	Even if the following instructions satisfy read or write access conditions, a break will not occur. • CAXI, SET1, CLR1, NOT1, and TST1 A break will normally occur only for the read-access address conditions by the following instructions. • PREPARE, DISPOSE, PUSHSP, POPSP, SWITCH, CALLT, and SYSCALL
2	Item	Hardware break [EIINT Table]
	Content	Do not set an address within the table for EIINT interrupts as a break condition. If a break occurs, it will not be possible, in some cases, to return from the interrupt processing even if EIRET is executed.
3	Item	Restriction on rewriting of on-chip flash memory (clock monitor)
	Content	The debugger changes the PLL settings when the flash memory is rewritten*. Thus, rewriting the flash memory raises a possibility of the frequency becoming higher than that currently in use. If the frequency surpasses the upper limit which was set by the clock monitor (CLMA), this prevents rewriting of the flash memory. Note: Rewriting of flash memory proceeds in response to any of the operations below. • Downloading to on-chip flash memory • Changes in on-chip flash memory due to operations in the memory panel • Setting or cancellation of software breaks • Re-execution after a software break is encountered (including stepped execution)

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4	Item	Breaks while clock settings are being made
	Content	The flash memory cannot be programmed if a break occurs while clock settings are being made. When performing operations below in a break state while the clock was being set, set [Change the clock to flash writing] in the property panel to [No]. • Any operation that involves programming of the flash memory (e.g. re-downloading) • Setting or deleting software breakpoints Also, do not set software breakpoints within the clock-setting routine.
5	Item	Contention in satisfaction of break conditions
	Content	If other read-access events are detected immediately before a transition to the break state due to a forced break, event break, etc., a break request due to a read-access event will be accepted during re-execution of the user program and a further break will then be generated.
6	Item	Event function (regarding the order of event detection)
	Content	In the following cases, since the orders of instructions and event detection may vary, time measurement and performance measurement between sequential events and over desired intervals will not be possible. • Events that are specified for consecutive instructions (because two instructions will be executed at the same time in some cases) • Access events by proximate read and write instructions are to be detected Since the timing of the detection of the events for write and read access will be different, even if instructions are executed in the order writing then reading, they may be detected in the order reading then writing.
7	Item	Event function (bit-manipulation instructions)
	Content	When a read or write access condition is set for an event, the writing cycle of read-modify-write generated by a bit-manipulation instruction is not detected as an event. This condition cannot be used as a trigger for a break, trace acquisition, or performance measurement in the case of such instructions.
8	Item	Event function (64-bit access)
	Content	Do not set an event for which a condition is 64-bit access. Doing so raises a possibility that an access not in a 64-bit unit will be detected, or that other events will not operate normally.
9	Item	Using power-saving modes
	Content	• For debugging of a program, ensure that the program sets WUFMSK0[0] to 0. • Release from the DEEPSTOP mode follows any of the following operations or conditions while the user program is being executed. Break Memory access Setting an event • The power supply to the ISO area (CPU, RAM, peripheral module, etc.) is not stopped in the DEEPSTOP mode during debugging. For this reason, RAM or registers which should have undefined initial values retain their values. Since these values become undefined after returning to the RUN mode in an actual device, be sure to initialize them.

No.		
10	Item	Reset
	Content	If a CPU reset occurs during execution of a user program, debugging functions (breaks, events, timers, etc.) and operation of the microcontrollers will become unstable.
11	Item	Restriction on rewriting of on-chip flash memory (register value)
	Content	The debugger changes the PLL0 settings when the flash memory is rewritten*. Thus, the value of PLL0SACT in CKSC_IPLL0S_ACT will be changed from 0 to 1. If the change in the register value creates a problem, set [Change the clock to flash writing] in the property panel to [No]. Note: Rewriting of flash memory proceeds in response to any of the operations below. • Downloading to on-chip flash memory • Changes in on-chip flash memory due to operations in the memory panel • Setting or cancellation of software breaks • Re-execution after a software break is encountered (including stepped execution)
12	Item	Registers in serial flash memory interface A (SFMA), CAN interface (RS-CAN), and CANFD interface (RS-CANFD)
	Content	If no clock signal or an abnormal clock signal is being supplied to SFMA or RS-CANFD and the debugger accesses the SFMA register via the I/O register window, a timeout error will occur. The SFMA, RS-CAN, and RS-CANFD registers must be accessed from the debugger after a normal clock signal has been supplied.
13	Item	PBG
	Content	When you are using an emulator, leave the PROTDEB bit of the FSGDxxPROTn register with the setting 1 (which allows access by a debug master). Changing the bit to a value other than its initial value may lead to normal access to memory becoming impossible.

3. Timing of Inclusion in Document

The next revision of the document will reflect the additions.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 16, 2016	-	First edition issued

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