[Notes]
RX Family
Clock Synchronous Control Module for EEPROM Access Firmware Integration Technology,
RX Driver Package

R20TS0608EJ0100
Rev.1.00
Sep. 01, 2020

Outline

When using the products in the title, note the following point.

1. Notes on build when GPIO module Firmware Integration Technology and MPC module Firmware Integration Technology are used

1. Notes on build when GPIO module Firmware Integration Technology and MPC module Firmware Integration Technology are used

1.1 Applicable Products

(1) Clock Synchronous Control Module for EEPROM Access Firmware Integration Technology (EEPROM FIT module)

The applicable revision numbers and document numbers are as follows.

Table 1.1 EEPROM FIT module applicable products

Revision number of the EEPROM FIT module	Document number
Rev.3.01	R01AN2325EJ0301
Rev.3.00	R01AN2325EJ0300

(2) RX Driver Package

The EEPROM FIT module in (1) is also included in the RX Driver Package.
The product names and revision numbers of the applicable RX Driver Package and the revision numbers and documents of the included EEPROM FIT module are as follows.

Table 1.2 Products which include the EEPROM FIT module

RX Driver Package product name	RX Driver Package revision number	Document number	Revision number of the included EEPROM FIT module
RX Family RX Driver Package Ver.1.26	Rev.1.26	R01AN5401EJ0126	Rev.3.01
RX Family RX Driver Package Ver.1.25	Rev.1.25	R01AN5371EJ0125	Rev.3.01
RX Family RX Driver Package Ver.1.24	Rev.1.24	R01AN5267EJ0124	Rev.3.01
RX Family RX Driver Package Ver.1.23	Rev.1.23	R01AN4976EJ0123	Rev.3.01
RX Family RX Driver Package Ver.1.22	Rev.1.22	R01AN4873EJ0122	Rev.3.01
RX Family RX Driver Package Ver.1.20	Rev.1.20	R01AN4794EJ0120	Rev.3.01
RX Family RX Driver Package Ver.1.19	Rev.1.19	R01AN4677EJ0119	Rev.3.00

1.2 Applicable Devices

RX Family

1.3 Description and Conditions

A warning and linkage errors arise during building when the following conditions are met.

(a) CS+ Integrated Development Environment is used.

(b) General I/O ports of the EEPROM FIT module are controlled via both of the following FIT modules(Note 1).

- GPIO module using Firmware Integration Technology (GPIO FIT module)
- MPC module using Firmware Integration Technology (MPC FIT module)

The following warning and linkage errors arise:

- W0561010:Duplicate
  file specified in option “input” : “DefaultBuild¥r_eeprom_spi_dev_port.obj”
- E0562310:
  Undefined external symbol "_r_eeprom_spi_wait_lp" referenced in "DefaultBuild¥r_eeprom_spi_sub.obj"
- E0562310:
  Undefined external symbol "_r_eeprom_spi_cs_init" referenced in "DefaultBuild¥r_eeprom_spi_sub.obj"
- E0562310:
  Undefined external symbol "_r_eeprom_spi_set_cs" referenced in "DefaultBuild¥r_eeprom_spi_sub.obj"
- E0562310:
  Undefined external symbol "_r_eeprom_spi_cs_reset" referenced in "DefaultBuild¥r_eeprom_spi_sub.obj"

Note 1: Specified by either of the following:
- The definition ”EEPROM_SPI_CFG_USE_GPIO_MPC_FIT” is enabled in ”r_eeprom_spi_config.h”.
- The item ENABLE GPIO MODULE AND MPC MODULE is set to Enabled in the Smart Configurator.

1.4 Detailed Description

This phenomenon is caused by the combination of the following (1) to (3).

(1) Two source files for controlling general I/O ports of the EEPROM FIT module have the same name.

Control settings for general I/O ports of the Chip Select pin (Port(SS#)) of the Serial EEPROM are specified by using either of the following. Note that the source file used in (a) and (b) is saved with the **same file name** in **different folders**.

(a) “iodefine.h” is used(Note 1) (Default setting)

r_eeprom_spi¥src¥dev_port¥**using_iodefine**¥**r_eeprom_spi_dev_port.c**

(b) GPIO FIT module and MPC FIT module are used

r_eeprom_spi¥src¥dev_port¥**using_gpio_fit_module**¥**r_eeprom_spi_dev_port.c**

Note 1: The EEPROM FIT module directly controls the ports.

(2) In CS+, an object file with the same name will be overwritten.

CS+ saves the generated object file in the same folder. If an object file with the same name is generated, the existing file will be overwritten with the object file most-recently generated.

Therefore, if you control general I/O ports of the EEPROM FIT module using (1) (b), the file will be ultimately overwritten by the object file (r_eeprom_spi_dev_port.obj) generated from (1) (a).

(3) Functions in either the source file (1) (a) or (1) (b) are enabled.

For source files (1) (a) and (1) (b), the same names are used for functions that perform different tasks. For these functions with the same names, only the functions chosen by #ifdef condition (”EEPROM_SPI_CFG_USE_GPIO_MPC_FIT” definition) in both source files are enabled. All other unselected functions in the source files are disabled.

Therefore, if (1) (b) is selected, all the functions with the same names in (1) (a) ”r_eeprom_spi¥src¥dev_port¥**using_iodefine**¥r_eeprom_spi_dev_port.c” are disabled by #ifdef, and symbols of the functions no longer exist.

```
#if ((defined(EEPROM_SPI_CFG_USE_FIT) && !defined(EEPROM_SPI_CFG_USE_GPIO_MPC_FIT)) || ¥
      (!defined(EEPROM_SPI_CFG_USE_FIT)))
void r_eeprom_spi_cs_init(uint8_t devno) { <Omitted> }
void r_eeprom_spi_cs_reset(uint8_t devno) { <Omitted> }
void r_eeprom_spi_set_cs(uint8_t devno, uint8_t lv) { <Omitted> }
void r_eeprom_spi_delaywait (unsigned long loop_cnt) { <Omitted> }
bool r_eeprom_spi_softwaredelay(uint32_t delay, bsp_delay_units_t units) { <Omitted> }
eeprom_status_t r_eeprom_spi_wait_lp(uint8_t unit) { <Omitted> }
#endif   /* #if (defined(EEPROM_SPI_CFG_USE_FIT) && defined(BSP_MCU_RX64M) &&
                    !defined(EEPROM_SPI_CFG_USE_GPIO_MPC_FIT)) || ¥
                    (!defined(EEPROM_SPI_CFG_USE_FIT) && defined(EEPROM_SPI_CFG_RX64M))) */
```

1.5 Workarounds

Change the names of the source files with the same name, as described in 1.4 (1) (a) and (b), to names that are not used in the EEPROM FIT module.

The following shows an example of changing the names.

- Change From: r_eeprom_spi¥src¥dev_port¥using_iodefine¥r_eeprom_spi_dev_port.c
  Change To: r_eeprom_spi¥src¥dev_port¥using_iodefine¥r_eeprom_spi_dev_port_iodefine.c
- Change From: r_eeprom_spi¥src¥dev_port¥using_gpio_fit_module¥r_eeprom_spi_dev_port.c
  Change To: r_eeprom_spi¥src¥dev_port¥using_gpio_fit_module¥r_eeprom_spi_dev_port_gpio.c

1.6 Schedule for Fixing the Problem

This problem will be fixed in the next version.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.01.20	-	First edition issued

Corporate Headquarters

TOYOSU FORESIA, 3- 2- 24 Toyosu,
Koto-ku, Tokyo 135- 0061, Japan
www.renesas.com

Trademarks

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

TS Colophon 4.1