[Notes]

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CS+, Cubesuite+, e^2 studio Integrated Development Environment

Outline

When using the CS+, CubeSuite+, or e^2 studio integrated development environment, note the following point.

1. Using an on-chip debugging emulator while the middle-speed on-chip oscillator of RL78 Family products is being used

1. Using an On-chip Debugging Emulator While the Middle-speed On-chip Oscillator of RL78 Family Products Is Being Used

1.1 Applicable Products

- RL78 Family C Compiler Package (with IDE)

  The version of the CS+ for CC common program is from V3.00.00 to V5.00.00.

- RL78, 78K Family C Compiler Package (with IDE)

  The version of the CS+ for CA, CX common program is from V3.00.00 to V5.00.00, or the version of the CubeSuite+ common program is V2.02.00 and later.

- [Evaluation edition] CS+ Integrated Development Environment

  The version of the CS+ for CC common program is from V3.00.00 to V5.00.00, or the version of the CS+ for CA, CX common program is from V3.00.00 to V4.00.00.

- [Evaluation edition] CubeSuite+ Integrated Development Environment

  The version of the CubeSuite+ common program is V2.02.00 and later.

- e^2 studio V2.2.0 to V5.4.0

Applicable emulators: E1 emulator, E20 emulator, and E2 emulator Lite

Applicable MCUs: RL78/I1D group, RL78/I1C group, and RL78/G11 group

1.2 Details

If a program is stopped with all the following conditions satisfied while the CPU clock is operating as a high-speed system clock, low-speed on-chip oscillator clock, or subsystem clock, a communications error occurs between the emulator and MCU. Subsequently, the debugging tool no longer operates correctly.

- Condition 1: The middle-speed on-chip oscillator clock is selected as the main on-chip oscillator clock.
  (Bit 0 (MCM1) in the system clock control register (CKC) of the MCU is set to 1.)

- Condition 2: The middle-speed on-chip oscillator clock is stopped.
  (Bit 1 (MIOEN) in the clock operation status control register (CSC) of the MCU is set to 0.)

1.3 Workaround

In order to prevent conditions 1 and 2 in 1.2, use the following procedure to stop the middle-speed on-chip oscillator clock.

(1) Select the high-speed on-chip oscillator clock as the main on-chip oscillator clock.
(Set bit 0 (MCM1) in the system clock control register (CKC) of the MCU to 0.)

(2) Stop the middle-speed on-chip oscillator clock.
(Set bit 1 (MIOEN) in the clock operation status control register (CSC) of the MCU to 0.)

1.4 Schedule for Fixing the Problem

This problem will be fixed in the next version. (This information will be available from July 20.)

- CS+ for CC V6.00.00
- CS+ for CA, CX V4.00.01
- e^2 studio V6.0

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May 16, 2017	-	First edition issued

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061 Japan
Renesas Electronics Corporation

■Inquiry
https://www.renesas.com/contact/