
[Notes]**CS+ Code Generator for RX,
e² studio Code Generator Plug-in,
AP4 Coding Assistance Tool for RX**

Outline

When using the products in the title, note the following point.

1. Initialization of port direction register (PDR) of RX130

1. Initialization of Port Direction Register (PDR) of RX130**1.1 Applicable Products**

- V1.03.00 and later versions of CS+ Code Generator for RX
- V3.1.0.024 of e² studio (V1.1.2 of the Code Generator plug-in) and later versions
- V1.03.00 and later versions of the AP4 coding assistance tool for RX

1.2 Applicable MCUs

- RX Family: RX130 Group (64-pin, 48-pin)
64-pin package
R5F51303AxFK, R5F51303AxFM, R5F51305AxFK, R5F51305AxFM,
R5F51306AxFK, R5F51306AxFM, R5F51307AxFK, R5F51307AxFM,
R5F51308AxFK, R5F51308AxFM
48-pin package
R5F51303AxFL, R5F51303AxNE, R5F51305AxFL, R5F51305AxNE,
R5F51306AxFL, R5F51306AxNE, R5F51307AxFL, R5F51307AxNE,
R5F51308AxFL, R5F51308AxNE

1.3 Details

To initialize the port direction register (PDR), the reserved bit needs to be set^(Note) to "1" (output). However, even if it is set to "1", an initialization processing code is not generated.

For 64-pin package, PORTD initialization processing is not generated, and for 48-pin package, PORT0, PORT5, and PORTD initialization processing is not generated.

Note: The input-only P35 pin is set to "0" (input).

1.4 Workaround

Follow the steps below to edit the C source to initialize the port direction register (PDR) to add the code.

- (1) Execute code generation.
- (2) Depending on whether it is 64-pin package or 48-pin package, manually add the code to `r_cg_hardware_setup.c`.

Note that you have to perform (2) each time you execute code generation.

- For 64-pin package, PORTD initialization processing is not generated. Therefore, you must add the following red text.

Before modification:

```
void R_Systeminit(void)
{
    /* Enable writing to registers related to operating modes, LPC, CGC and
software reset */
    SYSTEM.PRCR.WORD = 0xA50FU;

    Omitted

    /* Initialize non-existent pins */
    PORT0.PDR.BYTE = 0xD7U;
    PORT1.PDR.BYTE = 0x0FU;
    PORT2.PDR.BYTE = 0x3FU;
    PORT3.PDR.BYTE = 0x18U;
    PORT5.PDR.BYTE = 0xCFU;
    PORTA.PDR.BYTE = 0xA4U;
    PORTB.PDR.BYTE = 0x14U;
    PORTC.PDR.BYTE = 0x03U;
    PORTE.PDR.BYTE = 0xC0U;
    PORTH.PDR.BYTE = 0xF0U;
    PORTJ.PDR.BYTE = 0x3FU;

    Omitted
}
```

After modification:

```
void R_Systeminit(void)
{
    /* Enable writing to registers related to operating modes, LPC, CGC and
software reset */
    SYSTEM.PRCR.WORD = 0xA50FU;

    Omitted

    /* Initialize non-existent pins */
    PORT0.PDR.BYTE = 0xD7U;
    PORT1.PDR.BYTE = 0x0FU;
    PORT2.PDR.BYTE = 0x3FU;
    PORT3.PDR.BYTE = 0x18U;
    PORT5.PDR.BYTE = 0xCFU;
    PORTA.PDR.BYTE = 0xA4U;
    PORTB.PDR.BYTE = 0x14U;
    PORTC.PDR.BYTE = 0x03U;
PORTD.PDR.BYTE = 0xFFU;
    PORTE.PDR.BYTE = 0xC0U;
    PORTH.PDR.BYTE = 0xF0U;
    PORTJ.PDR.BYTE = 0x3FU;

    Omitted
}
```

- For 48-pin package, PORT0, PORT5, and PORTD initialization processing is not generated. Therefore, you must add the following red text.

Before modification:

```
void R_Systeminit(void)
{
    /* Enable writing to registers related to operating modes, LPC, CGC and
    software reset */
    SYSTEM.PRCR.WORD = 0xA50FU;

    Omitted

    /* Initialize non-existent pins */
    PORT1.PDR.BYTE = 0x0FU;
    PORT2.PDR.BYTE = 0x3FU;
    PORT3.PDR.BYTE = 0x1CU;
    PORT4.PDR.BYTE = 0x18U;
    PORTA.PDR.BYTE = 0xA5U;
    PORTB.PDR.BYTE = 0xD4U;
    PORTC.PDR.BYTE = 0x0FU;
    PORTE.PDR.BYTE = 0xE1U;
    PORTH.PDR.BYTE = 0xF0U;
    PORTJ.PDR.BYTE = 0x3FU;

    Omitted
}
```

After modification:

```
void R_Systeminit(void)
{
    /* Enable writing to registers related to operating modes, LPC, CGC and
    software reset */
    SYSTEM.PRCR.WORD = 0xA50FU;

    Omitted

    /* Initialize non-existent pins */
    PORT0.PDR.BYTE = 0x0FFU;
    PORT1.PDR.BYTE = 0x0FU;
    PORT2.PDR.BYTE = 0x3FU;
    PORT3.PDR.BYTE = 0x1CU;
    PORT4.PDR.BYTE = 0x18U;
    PORT5.PDR.BYTE = 0x0FFU;
    PORTA.PDR.BYTE = 0xA5U;
    PORTB.PDR.BYTE = 0xD4U;
    PORTC.PDR.BYTE = 0x0FU;
    PORTD.PDR.BYTE = 0x0FFU;
    PORTE.PDR.BYTE = 0xE1U;
    PORTH.PDR.BYTE = 0xF0U;
    PORTJ.PDR.BYTE = 0x3FU;

    Omitted
}
```

For details about the reserved bit of the port direction register (PDR), see the user's manual at the link below:

<https://www.renesas.com/search/keyword-search.html#genre=document&q=r01uh0560>

RX130 Group User's Manual: Hardware (document number: R01UH0560EJ0200)

18.4 Initialization of the Port Direction Register (PDR)

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. The next version will be available in July 2018.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 16, 2018	-	First edition issued

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061 Japan
 Renesas Electronics Corporation

■Inquiry

<https://www.renesas.com/contact/>

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