RENESAS Tool News

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A Note on Using a C/C++ Compiler V.9.00 Release 00 for the SuperH RISC engine Family CPUs

Please take note of the following problem in using a C/C++ compiler package for the SuperH RISC engine family of CPUs (hereafter abbreviated to SH C):

- On creating projects for the SH7206 microprocessor.

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1. **Product Concerned**
   C/C++ compiler package V.9.00 Release 00
   (used for the SuperH RISC engine family)

2. **Description**
   During simulations of projects for the SH7206 microprocessor, simulations may be halted or memory access errors may arise because necessary memory resources for operand caches cannot be acquired.

   2.1 Conditions

   This problem occurs if the following conditions are all satisfied:

   (1) In the Target list of the High-performance Embedded Workshop's New Project-7/9-Debuggers dialog box, either the "SH2A-FPU Cycle Base Simulator" or the "SH2A-FPU Functional Simulator" check box is checked.

   (2) In the High-performance Embedded Workshop, debugger session "SimSessionSH2A-FPU_Cycle" or "SimSessionSH2A-FPU_Func" is selected either of the following ways:

   (a) A session is selected out of the drop-down list that is opened by clicking the down arrow next to Current Session on the High-performance Embedded Workshop's Toolbar.

   (b) A session is selected out of the Current Session drop-down list in the Debug Session dialog box. This dialog box appears by opening the High-

performance Embedded Workshop's Options menu and selecting Debug Session.

(3) After executing a build, a simulation is performed either of the following ways:

(a) A simulation is started:

- by opening the High-performance Embedded Workshop's Debug menu and selecting Execute after Reset, or
- by clicking the Execute after Reset button on the Toolbar
  (In this case, the simulation may not be executed after Reset.)

(b) A simulation is started after setting a 1 to the bit 0 of the cache controlling register 1 (CCR1) to use operand caches:

- by opening the High-performance Embedded Workshop's Debug menu and selecting Execute Each Simulation, or
- by clicking the Execute Each Simulation button on the Toolbar
  (In this case, a memory access error may arise with an error message of "MemoryAccess Error" displayed in the High-performance Embedded Workshop's Output window when an operand cache is accessed.)

3. Workaround

Secure memory resources for operand caches before executing simulations by going through the following steps:

(1) Open the High-performance Embedded Workshop's Options menu and select Simulator, Memory Resources to open the Simulator Systems dialog box.

(2) Click the Add Memory Resources button to open the Set Memory dialog box.

(3) Enter H'F0800000 in the Beginning Address, H'F08FFFFF in the Ending Address, and Read/Write in the Type of Access text box; then click the OK button.

(4) Click the Add Memory Resources button once more to open the Set Memory dialog box.

(5) Enter H'F1800000 in the Beginning Address, H'F18FFFFF in the Ending Address, and Read/Write in the Type of Access text box; then click the OK button.

(6) Click the OK button in the Simulator Systems dialog box and close it.

4. Schedule of Fixing the Problem

Download DeviceUpdater V.1.02 Release 00 from **HERE** and update Device data in the SH C V.9.00 Release 00.

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