RENESAS Tool News

RENESAS TOOL NEWS on September 1, 2006: 060901/tn3

Corrections to User's Manuals of the HI7000/4 Series of Real-Time OSes

We inform you of corrections to the user's manuals of the HI7000/4 real-time OS listed below. These manuals are used for the HI7700/4 and HI7750/4 real-time OSes as well as the HI7000/4.
Here, the real-time OSes and their support MCUs are as follows:

- HI7000/4: Supports the SH-1-CPU-, SH-2-CPU-, SH2-DSP-, SH-2E-CPU- (FPU excluded), SH-2A-CPU-, and SH2A-FPU-cored MCUs
- HI7700/4: Supports the SH-3-CPU-, SH3-DSP-, and SH4AL-DSP-cored MCUs
- HI7750/4: Supports the SH-4-CPU- and SH-4A-CPU-cored MCUs

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1. Manuals Concerned

(1) HI7000/4 Series User's Manual Rev.6.00 (Document Number: REJ10B0060-0600)

(2) HI7000/4 Series User's Manual Rev.5.00 (Document Number: REJ10B0060-0500)

(3) HI7000/4 Series User's Manual Rev.4.00 (Document Number: REJ10B0060-0400H)

(4) HI7000/4 Series User's Manual Rev.3.00 (Document Number: REJ10B0060-0300H)

(5) HI7000/4 Series User's Manual 2nd ed. (Document Number: ADE-702-248A)

(6) HI7000/4 Series User's Manual 1st ed. (Document Number: ADE-702-248)

2. Corrections

Correction 1

In each of the following pages (in Section 2.4.1), replace the 8 lines next to Table 2.1, which are shown as Incorrect Text below, with the ones shown as Correct text.

Pages:

(1) Page 8 in Rev.6.00 (REJ10B0060-0600)

(2) Page 8 in Rev.5.00 (REJ10B0060-0500)

(3) Page 7 in Rev.4.00 (REJ10B0060-0400H)

(4) Page 7 in Rev.3.00 (REJ10B0060-0300H)

(5) Page 5 in 2nd ed. (ADE-702-248A)

(6) Page 5 in 1st ed. (ADE-702-248)

Incorrect Text:

The following processing is executed in non-task context.

- Interrupt handler
- CPU exception handler
- Time event handler (cyclic handler, alarm handler, and overrun handler)
- A part where the interrupt mask is changed to a value other than 0 by the chg_ims service call

Note that extended service calls initiated in the above processing state are also executed in non-task context.

Correct Text:

The following items of processing are executed in non-task context.

- Interrupt handler
- Time event handlers (cyclic handler, alarm handler, and overrun handler)
- The processing executed by changing the interrupt mask to a value other than 0 using the chg_ims service call

Note that extended service calls initiated in the above processing states are also executed in non-task context, and that the CPU exception handler is executed in the same context as before any CPU exception occurs.

Correction 2

In page 307 (in Section 4.8), replace the upper right 4 lines in Figure 4.4, which are shown as Incorrect Text below, with the ones shown as Correct text. This correction is applied to Rev.6.00 (REJ10B0060-0600) only.

Incorrect Text:

<- When SH-2A or SH2A-FPU is used and
CFG_REGBANK is checked, this statement can be
used because the handler does not have to

guarantee general registers.

Correct Text:

<- Only when interrupts using register bank is serviced in SH-2A or SH2A-FPU, this statement can be used because interrupt handler does not have to guarantee general registers.

Correction 3

In page 308 (in Section 4.8), replace the description of Note 4 at the bottom of Table 4.9, which is shown as Incorrect Text below, with the ones shown as Correct text. This correction is applied to Rev.6.00 (REJ10B0060-0600) only.

Incorrect Text:

When the SH-2A or SH2A-FPU is used and CFG_REGBANK is selected, the end condition is not required.

Correct Text:

Only when the interrupts using the register bank is serviced in the SH-2A or SH2A-FPU, the end condition is not required.

Correction 4

In each of the following pages, follow the instructions of corrections shown later.

Pages:

(1) Pages 327--328 in Rev.6.00 (REJ10B0060-0600)

(2) Pages 333--334 in Rev.5.00 (REJ10B0060-0500)

(3) Pages 297--298 in Rev.4.00 (REJ10B0060-0400H)

For these three manuals, correct the illustrations of the stack pointer (R15) in (a), (b), and (c) of Article (3), Section 4.9 as described below (the corrections are made only to the illustrations).

(4) Page 279 in Rev.3.00 (REJ10B0060-0300H)

(5) Page 265 in 2nd ed. (ADE-702-248A)

(6) Page 309 in 1st ed. (ADE-702-248)

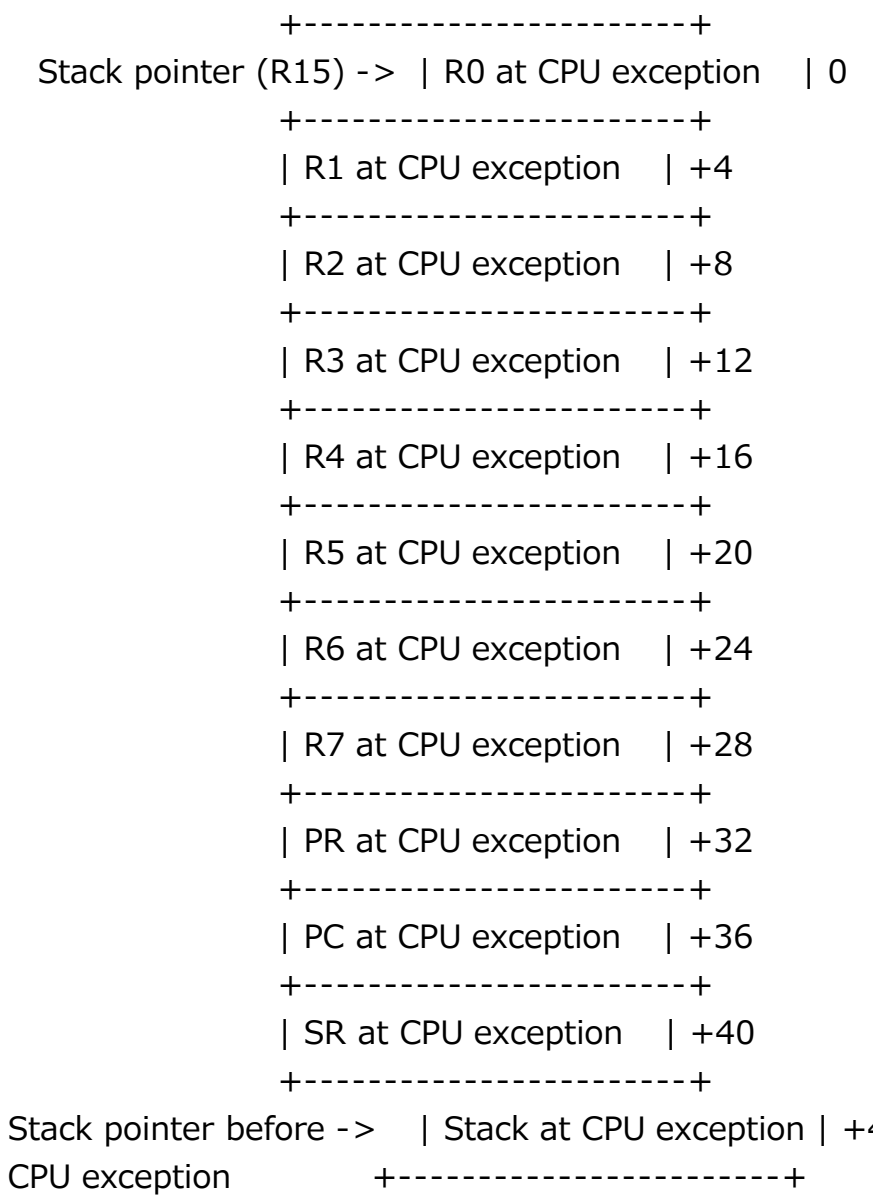
For these three manuals, add the contents of Article (3) corrected above to the end of the Section 4.8 "CPU Exception Handler".

Descriptions of additions and corrections:

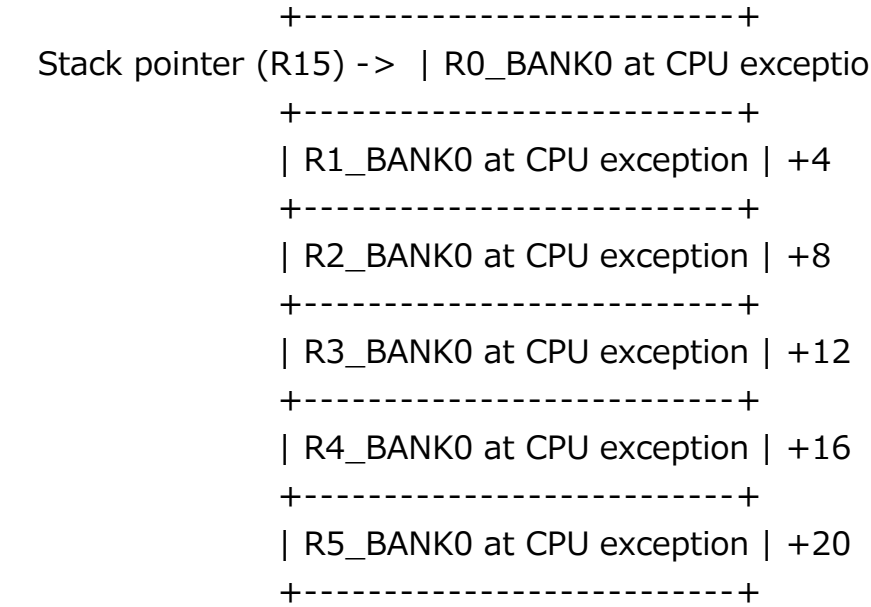
(3) Contents of Stack at Initiation
When a CPU exception occurs, the kernel saves the register contents in the stack. When execution is returned from a CPU exception handler, the

kernel restores these register contents from the stack.

In the illustration (a) HI7000/4



In the illustration (b) HI7700/4



```
                        | R6_BANK0 at CPU exception | +24
                        +--------------------------+
                        | R7_BANK0 at CPU exception | +28
                        +--------------------------+
                        | PR at CPU exception       | +32
                        +--------------------------+
                        | PC (SPC) at CPU exception | +36
                        +--------------------------+
                        | SR (SSR) at CPU exception | +40
                        +--------------------------+
    Stack pointer before ->    | Stack at CPU exception    | +44
    CPU exception              +--------------------------+
```

In the illustration (c) HI7750/4

```
                        +--------------------------+
      Stack pointer (R15) ->  | R0_BANK0 at CPU exception | 0
                        +--------------------------+
                        | R1_BANK0 at CPU exception | +4
                        +--------------------------+
                        | R2_BANK0 at CPU exception | +8
                        +--------------------------+
                        | R3_BANK0 at CPU exception | +12
                        +--------------------------+
                        | R4_BANK0 at CPU exception | +16
                        +--------------------------+
                        | R5_BANK0 at CPU exception | +20
                        +--------------------------+
                        | R6_BANK0 at CPU exception | +24
                        +--------------------------+
                        | R7_BANK0 at CPU exception | +28
                        +--------------------------+
                        | PR at CPU exception       | +32
                        +--------------------------+
                        | FPSCR at CPU exception    | +36
                        +--------------------------+
                        | PC (SPC) at CPU exception | +40
                        +--------------------------+
                        | SR (SSR) at CPU exception | +44
                        +--------------------------+
    Stack pointer before ->    | Stack at CPU exception    | +48
    CPU exception              +--------------------------+
```

The past news contents have been based on information at the time of publication. Now changed or invalid information may be included. The URLs in the Tool News also may be subject to change or become invalid without prior notice.