NEC Microcomputer Technical Information

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V853 32-Bit Microcontrollers Usage Restrictions	Document No.	ZBG-CC-05-0074	1/1
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	Issued by	Solution Development Group Multipurpose Microcomputer Systems Division 4th Systems Operations Unit NEC Electronics Corporation	
Related documents Hardware User's Manual: U10913EJ6V0UM00 (6th edition) Architecture User's Manual: U10243EJ7V0UM00 (7th edition) Data Sheet (mask ROM): U13188EJ6V1DS00 (6th edition) Data Sheet (flash memory): U13189EJ5V1DS00 (5th edition)	Notification classification	√	Usage restriction
			Upgrade
			Document modification
			Other notification

1. Affected products

V853, V853A

μPD703003, 703003A, 703004A, 703025A: Mask ROM versions

μPD70F3003, 70F3003A, 70F3025A: Flash memory versions

2. Details of restriction

The following restriction (No. 10) has been added (to μPD70F3025A rank M). For details, refer to the attachment.

- No. 10 Restriction related to internal verify error during flash memory programming

  An internal verify error may occur when programming to the internal flash memory (successive execution of erase, write, and verify) is performed.

3. Workaround

The following workaround is available for this restriction. For details, refer to the attachment.

- When using flash programmer PG-FP3:

  Execute the E.P.V. command after the Erase command is executed.

- When using flash programmer PG-FP4:

  Upgrade service will be available in conjunction with future firmware updates.

4. Correction

Device modification for restriction No. 10 is not planned. Regard this item as a usage restriction.

5. List of restrictions

The restriction history and detailed information is described in the attachment.

6. Document revision history

Document Number	Issued on	Description
SBG-DT-0081	April 24, 2002	1st edition
ZBG-CC-05-0067	December 15, 2005	Addition of restriction No. 10

List of Usage Restrictions in V853

1. Product Version

μPD703003:	Rank K
μPD70F3003:	Rank E
μPD703003A, 703004A, 703025A:	Rank K, E
μPD70F3003A:	Rank K, E, P
μPD70F3025A:	Rank K, E, P, X, M

* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

2. Product History

μPD703003, 70F3003

No.	Restrictions (Cautions)	Rank
		All Ranks
1	Restriction related to on-chip peripheral I/O access immediately after data read from external memory	Δ
2	Restriction related to conflict between execution of bit manipulation instruction for on-chip peripheral I/O register and external bus hold	Δ
3	Restriction related to timer capture operation	Δ
4	Caution on interrupt servicing after EI instruction	Δ
5	Caution on power save mode release	Δ
6	Caution on related to A/D converter status flag CS	Δ
7	Caution on flash memory programming	–
8	Cautions on A/D converter conversion operation time	Δ
9	Restriction on A/D converter operation	Δ
10	Restriction related to internal verify error during flash memory programming	–

√: Restriction does not apply, Δ: Restriction will also apply in future (caution), ×: Restriction applies, –: Not relevant

μPD703003A, 703004A, 703025A

No.	Restrictions (Cautions)	Rank
		All Ranks
1	Restriction related to on-chip peripheral I/O access immediately after data read from external memory	–
2	Restriction related to conflict between execution of bit manipulation instruction for on-chip peripheral I/O register and external bus hold	–
3	Restriction related to timer capture operation	–
4	Caution on interrupt servicing after EI instruction	Δ
5	Caution on power save mode release	Δ
6	Caution on related to A/D converter status flag CS	Δ
7	Caution on flash memory programming	–
8	Cautions on A/D converter conversion operation time	Δ
9	Restriction on A/D converter operation	Δ
10	Restriction related to internal verify error during flash memory programming	–

√: Restriction does not apply, Δ: Restriction will also apply in future (caution), ×: Restriction applies, –: Not relevant

μPD70F3003A

No.	Restrictions (Cautions)	Rank
		All Ranks
1	Restriction related to on-chip peripheral I/O access immediately after data read from external memory	–
2	Restriction related to conflict between execution of bit manipulation instruction for on-chip peripheral I/O register and external bus hold	–
3	Restriction related to timer capture operation	–
4	Caution on interrupt servicing after EI instruction	Δ
5	Caution on power save mode release	Δ
6	Caution related to A/D converter status flag CS	Δ
7	Caution on flash memory programming	√
8	Cautions on A/D converter conversion operation time	Δ
9	Restriction on A/D converter operation	Δ
10	Restriction related to internal verify error during flash memory programming	√

√: Restriction does not apply, Δ: Restriction will also apply in future (caution), ×: Restriction applies, –: Not relevant

μPD70F3025A

No.	Restrictions (Cautions)	Rank	
		K,E,P,X	M
1	Restriction related to on-chip peripheral I/O access immediately after data read from external memory	–	–
2	Restriction related to conflict between execution of bit manipulation instruction for on-chip peripheral I/O register and external bus hold	–	–
3	Restriction related to timer capture operation	–	–
4	Caution on interrupt servicing after EI instruction	Δ	Δ
5	Caution on power save mode release	Δ	Δ
6	Caution on related to A/D converter status flag CS	Δ	Δ
7	Caution on flash memory programming	×	√
8	Cautions on A/D converter conversion operation time	Δ	Δ
9	Restriction on A/D converter operation	Δ	Δ
10	Restriction related to internal verify error during flash memory programming	√	Δ

√: Restriction does not apply, Δ: Restriction will also apply in future (caution), ×: Restriction applies, –: Not relevant

3. Details of Restrictions

No. 1 Restriction related to on-chip peripheral I/O access immediately after data read from external memory

[Description]

The following phenomena may occur if any of the on-chip peripheral I/O registers are accessed immediately after a data read (except a program fetch) is executed on the external memory mapped to the memory block for which insertion of an idle state was enabled by the bus cycle control register (BCC).

- The read data is undefined if the on-chip peripheral I/O register is accessed by a read operation.
- Undefined data is written to the on-chip peripheral I/O register if the on-chip peripheral I/O register is accessed by a write operation, or data is written to an address incremented by 2.
- Undefined data is written to the on-chip peripheral I/O register if the on-chip peripheral I/O register is accessed by a bit manipulation instruction (set1, not1, clr1, tst1).

<Program example>

```
ld.w    0[r10], r20 ← Instruction for loading from external memory (with insertion of idle state)
ld.b    0xFFFFF … [r0], r21 ← Access to on-chip peripheral I/O register (bug occurs)
```

[Workaround]

Implement either of the following workarounds.

(1) Do not insert any idle states (set the BCn bit of the BCC register to 0).

(2) Insert a nop instruction between the load instruction for the external memory which is accompanied by an idle state and the instruction which is accompanied by access to the on-chip peripheral I/O register so that one instruction is not followed by the other.

No. 2 Restriction related to conflict between execution of bit manipulation instruction for on-chip peripheral I/O register and external bus hold

[Description]

If an external bus hold request is generated during the read cycle of a bit manipulation instruction (set1, clr1, not1 only; excluding tst1) for an on-chip peripheral I/O register, followed by an instruction fetch from the external memory, the bus cycle becomes abnormal and an undefined code is fetched, causing an inadvertent program loop.

[Workaround]

Implement either of the following workarounds.

(1) Do not use bus hold.

(2) Do not use a bit manipulation instruction (set1, clr1, not1) during execution of the program on the external memory.

No. 3 Restriction related to timer capture operation

[Description]

When CC132 of the timer (TM13) is specified as a capture register, if the timing at which data is captured and the timer is incremented conflict, data that should be captured to CC132 may be undefined.

[Workaround]

Do not specify CC132 of TM13 as a capture register.

No. 4 Caution on interrupt servicing after EI instruction

[Description]

An interrupt detection time of about 7 clock cycles is required from the generation of an interrupt request until the interrupt can be acknowledged. Instructions continue to be executed during this period, and if a DI instruction is executed (interrupt disable), then interrupts are disabled. As a result, all interrupts will be held until the next EI instruction (interrupt enable) is issued. In addition, this interrupt detection time is also required after executing the EI instruction, which means that a minimum of 7 clock cycles must elapse before interrupts can be acknowledged after the EI instruction has been executed. For this reason, if the DI instruction is executed less than 7 clock cycles after the EI instruction is executed, interrupts are held pending.

<Program example>

```
DI
 :              ; MK flag = 0 (enables interrupt servicing)
 :              ← Interrupt request generated (IF flag = 1)
EI
JR LP1
 :               ; Less than 3 clock cycles elapse from EI to DI (3 clock cycles)
 :
LP1:
DI              ; Interrupt request is not acknowledged.
:
```

[Workaround]

In order for interrupts to be able to be acknowledged, be sure to insert seven clock cycles worth of instructions[Note] between the EI instruction and the subsequent DI instruction.

Note Use instructions other than the following.

- IDLE/STOP mode setting instructions
- EI instruction
- DI instruction
- RETI instruction
- LDSR instruction (for PSW)
- Access to interrupt control registers (xxICn)

<Example of modified program>

```
        DI
        :               ; MK flag = 0 (enables interrupt servicing)
        :               ; Interrupt request issued (IF flag = 1)
        EI
        NOP             ; 1 system clock cycle          }
        NOP             ; 1 system clock cycle          }
        NOP             ; 1 system clock cycle          } 7 clocks
        NOP             ; 1 system clock cycle          }
        JR LP1          ; 3 system clock cycles (branch to LP1 routine)  }
        :
LP1:                    ; LP1 routine
  DI                    ; Interrupt servicing is executed at 8th clock cycle after the EI instruction.
        :
```

No. 5 Caution on power save mode release

[Description]

If the affected products are used under the following conditions, a discrepancy may occur between the address indicated by the program counter (PC) and the address at which the instruction is actually read after the release of a power save mode. This may result in the CPU ignoring a 4- or 8-byte instruction from between 4 bytes and 16 bytes after an instruction is executed to write to the PSC register, which could in turn result in the execution of an erroneous instruction.

This bug occurs only if all of conditions (1) to (3) below are met.

(1) A power save mode (IDLE or STOP) is set while an instruction is being executed on the external ROM.
(2) The power save mode is released by an NMI servicing.
(3) The subsequent instruction is executed while interrupts are held pending after the release of the power save mode.
Note that interrupts are held pending when the NP flag of the PSW register is 1 (NMI servicing in progress/set by software).

The operation of the bug is shown below using the power save mode setting example from the user's manual.
(rD: PSC setting value, rX: Value written to PSW, rY: Value written back to PSW, assuming PSW has been set)

<Program example>

```
ldsr  rX,5              ; Sets PSW to the value of rX
st.b  r0,PRCMD[r0]      ; Writes to PRCMD
st.b  rD,PSC[r0]        ; Sets the PSC register        (PSC setting)
ldsr  rY,5              ; Returns the value of PSW     (After 4 bytes)
nop                     ; 2 to 5 NOP instructions      (After 6 bytes)
nop                     ;                              (After 8 bytes)
nop                     ;                              (After 10 bytes)
nop                     ;                              (After 12 bytes)
nop                     ;                              (After 14 bytes)
(Next instruction)      ;                              (After 16 bytes)
```

Bug occurs here
<1>Discrepancy with PC
<2>Instructions ignored

[Workaround]

Implement either of the following workarounds.

(1) Do not use a power save mode (IDLE or STOP) while an instruction is being executed on the external ROM.

(2) If it is necessary to use a power save mode (IDLE or STOP) while an instruction is being executed on the external ROM, take the software countermeasures shown below.

<1> Insert 6 NOP instructions 4 bytes after an instruction that writes to the PSC register.

<2> Insert the br $+2 instruction after the NOP instructions to eliminate the PC discrepancy.

[Preventive program example]

(rD: PSC setting value, rX: Value written to PSW, rY: Value written back to PSW, assuming PSW has been set)

```
ldsr  rX,5              ; Sets PSW to the value of rX
st.b  r0,PRCMD[r0]      ; Writes to PRCMD
st.b  rD,PSC[r0]        ; Sets the PSC register
ldsr  rY,5              ; Returns the value of PSW

nop                     ; <1> 6 or more NOP instructions
nop
nop
nop
nop
nop

br  $+2                 ; <2> Eliminates PC discrepancy
```

No. 6 Caution related to A/D converter status flag CS

[Description]

The CS bit of A/D converter mode register 0 (ADM0) is a flag used to indicate the A/D converter status. It takes 3 clocks for the CS bit to become 1 (indicating A/D conversion in progress) from the start of A/D conversion. Confirm the completion of A/D conversion by checking bit 7 (ADIF) of the interrupt control register (ADIC).

A program example in which an incorrect conversion value is read is shown below.

<Program example>

```
            set1    7,ADM0[r0]      ; Enables A/D conversion
  WAIT:
            tst1    6,ADM0[r0]      ; Confirmation of A/D conversion operation (1 clock
                                    ; elapsed after A/D conversion was enabled)
            jnz     WAIT
            ld.h    ADCR0[r0],r10   ; Read A/D conversion value
                                    ; (an incorrect conversion value is read)
            :
```

[Workaround]

Implement the following workaround to avoid this error.

Confirm the completion of A/D conversion by checking bit 7 (ADIF) of the interrupt control register (ADIC). Read the A/D conversion value when ADIF = 1.

<Example of preventive program>

```
            set1    7,ADM0[r0]      ; Enables A/D conversion
  WAIT:
            tst1    7,ADIC[r0]      ; Confirmation of A/D conversion operation
            jz      WAIT
            ld.h    ADCR0[r0],r10   ; Read A/D conversion value
                                    ; (a correct conversion value is read)
```

No. 7 Caution on flash memory programming

[Description]

A new flash memory programming mode will be added with the aim of reducing the internal flash memory write time. This mode is called the handshake mode, or HS mode. HS is a 4-wire serial interface that uses CSI0 and P21.

The conventional product and the product with improved characteristics can be identified by their ranks. The rank is indicated by the fifth character from the left in the lot number marked on the package.

Example K rank: ****K**** (fifth character from the left in the lot number)

Comparison of Flash Memory Characteristics

Product Name	μPD70F3025AGC-25-8EU, μPD70F3025AGC-33-8EU	
Rank[Note 1]	X	M (other than K, E, P, or X)
Handshake support [Note 2]	Not supported	Supported
Write time (ref.)	140 seconds [Note 3]	40 seconds [Note 4]
Environment for using flash programmer PG-FP2	Firmware: V2.50f or later GUI: V3.02 or later Parameter file: 70F3025A.PRC (V1.04) 70F3025A_1000.PRC (V2.02) [Note 5]	Firmware: V2.51a GUI: V3.07b Parameter file: 70F3025A_A.PRC (V1.01) 70F3025A_1000_A.PRC (V2.01) [Note 5]
Environment for using flash programmer PG-FP3	Firmware: V3.04d or later GUI: V3.02 or later Parameter file: 70F3025A.PRC (V1.04) 70F3025A_1000.PRC (V2.02) [Note 5]	Firmware: V3.05d GUI: V3.06a Parameter file: 70F3025A_A.PRC (V1.01) 70F3025A_1000_A.PRC (V2.01) [Note 5]

Notes 1. There is also a product rank I, however rank I applies only to ES products. Operations of ES products are not guaranteed.

2. The PG-FP3 can be used. The PG-FP2 is not supported.

3. With transfer mode SIO, transfer clock 1 MHz, and CPU clock 20 MHz.

4. With transfer mode SIO ch-3 + handshake, transfer clock 1 MHz, and CPU clock 20 MHz when the PG-FP3 is used.

5. Version that supports CPU clock of 10 MHz or over

Caution There is basically a separate parameter file for each rank. The parameter file for X rank products cannot be used when writing products with M rank (other than K, E, P or X), because the programming process is different. Be sure to change the parameter file in accordance with the rank.

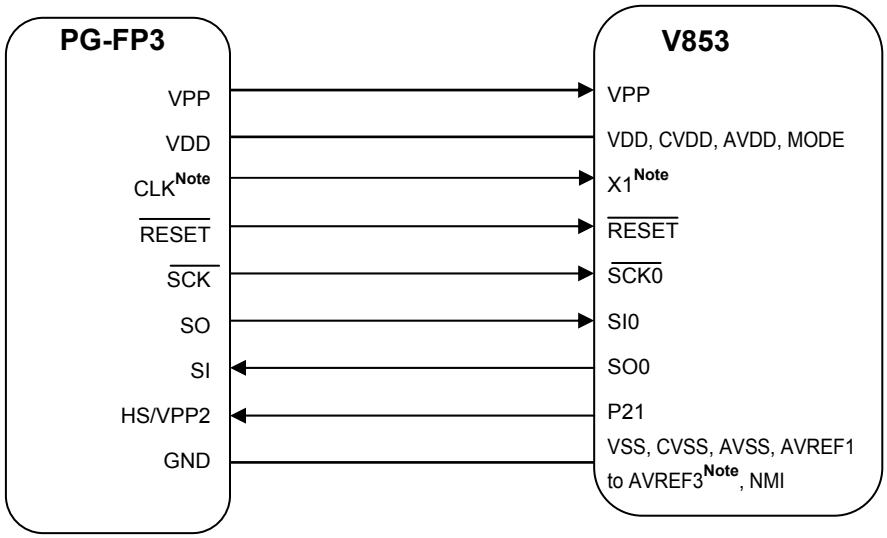
Handshake mode for flash memory programming

The μPD70F3025A (rank M) and μPD70F3003A support high-speed flash memory programming using a 3-wire serial handshake mode. The PG-FP2 is not supported.

The high-speed writing process is as follows.

(1) Directly connect the HS pin (or Vpp2 pin) of the target interface of the NEC Electronics flash programmer PG-FP3 to pin 21 of the device.
(2) Change the COMM PORT setting to SIO ch-3+handshake on the GUI (host PC).
(3) Start programming.

CSI Communication Mode with Handshake Supported (MSB-first transfer)



Note Change the connection according to the environment used.

No. 8 Cautions on A/D converter conversion operation time

[Description]

Time to initialize the A/D converter is required before the A/D converter is activated.

The time required for initializing the A/D converter is shown below.

Trigger Interval in External or Timer Trigger Mode

FR2	FR1	FR0	Number of Conversion Clocks	Number of Initialization Clocks	Minimum Trigger Interval [μs]			
					Number of Clocks	ϕ = 33 MHz	ϕ = 25 MHz	ϕ = 16 MHz
0	0	0	36	5	41 Note 1	–	–	2.57 Note 2
0	0	1	48	6	54	–	2.16	3.38
0	1	0	60	7	67 Note 1	2.03 Note 2	2.68 Note 2	4.19 Note 2
0	1	1	72	8	80	2.43	3.20	5.00
1	0	0	96	10	106	3.22	4.24	6.63
1	0	1	120	12	132	4.00	5.28	8.25
1	1	0	144	14	158	4.79	6.32	9.88
1	1	1	192	18	210	6.37	8.40	13.2

Notes 1. In timer trigger mode, the minimum count clock value of timer 1 that can be set is $\phi \times 2$. To obtain the number of clocks for the minimum trigger interval, add 1 to the value in the above table. For example, the minimum trigger interval is 42 clocks when FR2 = FR1 = FR0 = 0.

2. Minimum trigger interval in external trigger mode

Remark ϕ = Internal system clock frequency

Number of Clocks from CE Setting to Sampling Start in A/D Trigger Mode

FR2	FR1	FR0	Number of Conversion Clocks	Number of Initialization Clocks
0	0	0	36	8
0	0	1	48	9
0	1	0	60	10
0	1	1	72	11
1	0	0	96	13
1	0	1	120	15
1	1	0	144	17
1	1	1	192	21

Caution In the A/D trigger mode, initialization is required only the first time each operating mode is set. For example, when scan mode is selected, time to initialize ANI0 is required but initialization is not required for ANI1 to ANI7. Therefore, initialization clocks for ANI1 to ANI7 are not required.

No. 9 Restriction on A/D converter operation

[Description]

If a timer match interrupt (INTCC111, INTCC112, or INTCC113) or an external pin interrupt (INTP111, INTP112, or INTP113) occurs when the 1-trigger mode of the timer trigger mode or external trigger mode is used, A/D conversion may be re-started after A/D conversion ends.

This restriction does not apply when the A/D trigger mode or 4-trigger mode of the timer trigger mode is used.

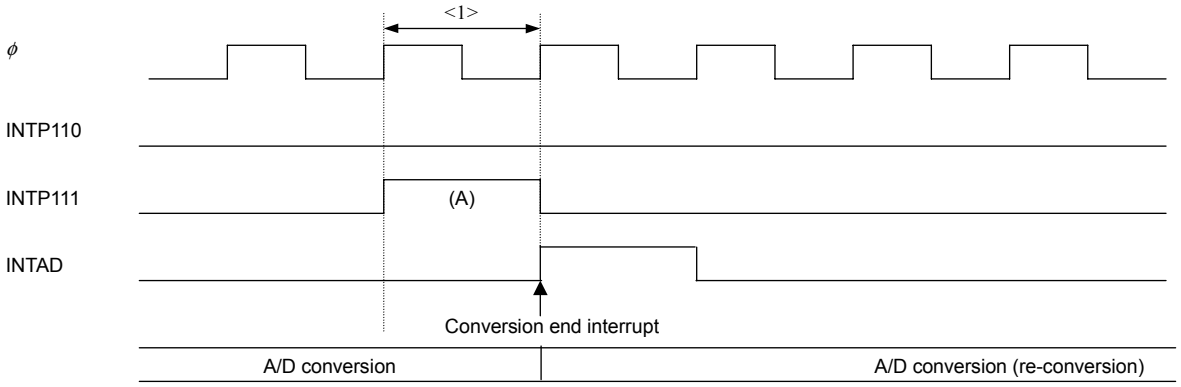
Originally, only INTCC110 can be the trigger to start the A/D converter in the 1-trigger mode, and ADTRG pin input in the external trigger mode, therefore the interrupt sources listed below should be ignored. However, if one of the interrupt sources listed below occurs immediately before the end of A/D conversion (<1> in the figure below; 1 internal system clock), it is mistakenly judged as the A/D conversion start trigger. As a result, A/D conversion is started again after the A/D conversion end interrupt (INTAD) is issued. The first A/D conversion ends correctly and the result is stored in the ADCRn register (this value can be read during the second conversion).

The restarted A/D converter performs the conversion operation correctly, issues the A/D conversion end interrupt (INTAD) and stops. The result is overwritten to the ADCRn register.

Interrupt Source That Can Trigger A/D Conversion

Timer match interrupt	INTCC111
	INTCC112
	INTCC113
External pin interrupt	INTP111
	INTP112
	INTP113

Example of Timing at Which This Restriction Applies



ϕ: Internal system clock

Caution The external interrupt signal that functions alternately as the external capture trigger input of timer 1 can also be a trigger for re-conversion. In the case of an external interrupt input, this restriction applies when a valid edge is input before the timing of (A) in the above figure by the noise eliminator (digital noise elimination (2 to 3 internal system clocks).

[Condition under which this restriction does not apply]

This restriction does not apply when the A/D trigger mode or 4-trigger mode of the timer trigger mode is used.

The condition in which this restriction does not apply in the 1-trigger mode of the timer trigger mode or external trigger mode is shown below.

- The compare match interrupt (INTCC111/112/113) does not occur during A/D conversion, and the external interrupt signal (INTP111/112/113) is not input during A/D conversion.

[Workaround]

The conversion result is correct even when this restriction occurs. If the re-conversion causes any problems, take any of the following workarounds.

(1) Start A/D conversion in the A/D trigger mode by setting the ADCE bit of the ADM0 register to 1 in the interrupt service routine of the timer match interrupt or external pin interrupt.

(2) Do not use the compare match interrupt (INTCC111/112/113) and external interrupt signal (INTP111/112/113) during A/D conversion.

No. 10 Restriction related to internal verify error during flash memory programming

[Description]

There is a path that allows more current to flow, compared to the ordinary current, to the internal flash memory macro during erase execution. This extra current causes a difference in the voltage judgment levels between when programming to the internal flash memory (successive execution of erase, write, and verify) is performed and when internal verify is performed after programming. Consequently, an internal verify error may occur.

[Influence on reliability]

Even circuits that allow extra current to flow are designed on the assumption that currents flow during operations other than erasure. Even if an extra current were to flow, therefore, it would be assumed to be within the allowable range, so there would be no problem in terms of product quality and the long-term reliability would not be affected. In addition, during internal verify, the programming level is checked at a voltage level which is stricter than that during flash memory read operation, including sufficient margin. Therefore, when the user rewrites the program because the above error has occurred, if the above error no longer occurs, it would mean that the product has sufficient margin for the operation and the written data has no problem concerning the reliability.

[Workaround]

- When using flash programmer PG-FP3:
  Execute the E.P.V. command after the Erase command is executed.
- When using flash programmer PG-FP4:
  Upgrade service will be available in conjunction with future firmware updates.

If you are using a flash programmer or programming method other than mentioned above, consult an NEC Electronics sales representative or distributor.