NEC

Customer Notification

V850/SF1™

32-Bit Single-Chip Microcontrollers

Operating Precautions

μPD703075AY
μPD703075AY(A)
μPD703076AY
μPD703076AY(A)
μPD703078AY
μPD703078AY(A)
μPD703079AY
μPD703079AY(A)
μPD70F3079AY
μPD70F3079AY(A)
μPD70F3079BY
μPD70F3079BY(A)

Document No. U18408EE3V0IF00
Date Published December 2007

DISCLAIMER

The related documents in this customer notification may include preliminary versions. However, preliminary versions may not have been marked as such.

The information in this customer notification is current as of its date of publication. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC PRODUCT(S). Not all PRODUCT(S) and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.

No part of this customer notification may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this customer notification. NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC PRODUCT(S) listed in this customer notification or any other liability arising from the use of such PRODUCT(S).

No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others. Descriptions of circuits, software and other related information in this customer notification are provided for illustrative purposes of PRODUCT(S) operation and/or application examples only. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

While wherever feasible, NEC endeavors to enhance the quality, reliability and safe operation of PRODUCT(S) the customer agree and acknowledge that the possibility of defects and/or erroneous thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects and/or errors in PRODUCT(S) the customer must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.

The customer agrees to indemnify NEC against and hold NEC harmless from any and all consequences of any and all claims, suits, actions or demands asserted against NEC made by a third party for damages caused by one or more of the items listed in the enclosed table of content of this customer notification for PRODUCT(S) supplied after the date of publication.

Applicable Law:

The law of the Federal Republic of Germany applies to all information provided by NEC to the Customer under this Operating Precaution document without the possibility of recourse to the Conflicts Law or the law of 5th July 1989 relating to the UN Convention on Contracts for the International Sale of Goods (the Vienna CISG agreement).

Düsseldorf is the court of jurisdiction for all legal disputes arising directly or indirectly from this information. NEC is also entitled to make a claim against the Customer at his general court of jurisdiction.

If the supplied goods/information are subject to German, European and/or North American export controls, the Customer shall comply with the relevant export control regulations in the event that the goods are exported and/or re-exported. If deliveries are exported without payment of duty at the request of the Customer, the Customer accepts liability for any subsequent customs administration claims with respect to NEC.

Notes: 1. "NEC" as used in this statement means NEC Corporation and also includes its direct or indirect owned or controlled subsidiaries.

2. "PRODUCT(S)" means 'NEC semiconductor products' (NEC semiconductor products means any semiconductor product developed or manufactured by or for NEC) and/or 'TOOLS' (TOOLS means 'hardware and/or software development tools' for NEC semiconductor products' developed, manufactured and supplied by 'NEC' and/or 'hardware and/or software development tools' supplied by NEC but developed and/or manufactured by independent 3rd Party vendors worldwide as their own product or on contract from NEC)

Table of Contents

(A) Table of Operating Precautions

(A).1 μPD703075AY, μPD703075AY(A), μPD703076AY, μPD703076AY(A), μPD703078AY, μPD703078AY(A), μPD703079AY, μPD703079AY(A)

No.	Outline		μPD703075AY μPD703075AY(A) μPD703076AY μPD703076AY(A) μPD703078AY μPD703078AY(A) μPD703079AY μPD703079AY(A)	
		Rev.		
		Rank[Note]	K	
1	FCAN: Resynchronisation (Specification change notice)		✗	
2	FCAN: CACT Register Access (Specification change notice)		✗	
3	FCAN: Diagnostic Mode (Specification change notice)		✗	
4	FCAN: Mode Transition (Specification change notice)		✗	
5	Conflict between writing to external memory and HLDRQ signal		✓	
6	Reading timer count register TMn of timers TM2 to TM6		✗	

✓ : Not applicable

✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(A).2 µPD70F3079AY, µPD70F3079AY(A)

No.	Outline		µPD70F3079AY µPD70F3079AY(A)	
		Rev.		
		Rank[Note]	K	
1	FCAN: Resynchronisation (Specification change notice)		✗	
2	FCAN: CACT Register Access (Specification change notice)		✗	
3	FCAN: Diagnostic Mode (Specification change notice)		✗	
4	FCAN: Mode Transition (Specification change notice)		✗	
5	Conflict between writing to external memory and HLDRQ signal		✗	
6	Reading timer count register TMn of timers TM2 to TM6		✗	

✓ : Not applicable

✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(A).3 µPD70F3079BY, µPD70F3079BY(A)

No.	Outline		µPD70F3079BY µPD70F3079BY(A)	
		Rev.		
		Rank[Note]	K	
1	FCAN: Resynchronisation (Specification change notice)		✗	
2	FCAN: CACT Register Access (Specification change notice)		✗	
3	FCAN: Diagnostic Mode (Specification change notice)		✗	
4	FCAN: Mode Transition (Specification change notice)		✗	
5	Conflict between writing to external memory and HLDRQ signal		✓	
6	Reading timer count register TMn of timers TM2 to TM6		✗	

✓ : Not applicable

✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	FCAN: Resynchronisation (Specification change notice)

Details

According to the CAN protocol specification (BOSCH CAN specification, version 2.0, Sept. 1991, part A, chapter 8, 'Bit Timing Requirements', Synchronization, Synchronization Rules, Rule 1-4, page 30) a CAN node has to perform a soft-synchronization, when acting as a transmitter sending a dominant bit if a recessive to dominant edge occurs after the sample point within phase segment 2. This scenario is only encountered in case of a disturbance. For this case the soft-synchronization is not performed. As a consequence the nominal length of an error frame that follows this disturbance can be extended by the amount of time quanta allocated for the synchronization jump width.

An impact on the application is not given since the length of error frames can not be predicted anyway due to the superposition mechanism that is defined in the CAN protocol.

No. 2	FCAN: CACT Register Access (Specification change notice)

Details

The register CxBA offers information on the current bus activity for each CAN channel in the field CACT. For the bus off status of the channel normally the code "11" is displayed which is not the case here. Instead, in bus off status the CPU will always read the activity status that preceded the bus off condition.

The CACT register is implemented to serve CAN experts while debugging new FCAN macros. The application should not use the CACT especially not for detecting a bus off condition. Instead, the bus off status can be derived from CxCTRL register (bit: BOFF).

No. 3	FCAN: Diagnostic Mode (Specification change notice)

Details

The diagnostic mode is not entered when setting MOM bit in CxDEF register to 1. This mode was considered for baud rate detection and diagnostic purposes.
As a consequence the "receive only" operation of the FCAN is not available.
Applications that need to implement automatic baud rate detection may use one of the following procedures instead of "receive only" mode:

- "Set TPE bit in CxCTRL register to 1. The transmit pin of the respective CAN module is disabled then.
- "In case the device facilitates a shared port function for the CAN transmit pin, the output latch of this port bit has to be set to 1 and corresponding bit in the port mode register can be set to output mode. This provides recessive level for the CAN transmit line.

Any message on the CAN bus will update the VALID bit in the CxDEF register. The correct baud rate is achieved if the VALID bit reads 1.

Further Precaution: Immediate Recovery from Bus Off Status

Although the "receive only" operation is not usable, the receive and transmit error counters can be reset. The respective CAN module could be transferred into initialization status by the normal initialization request (INIT =1 in CxCTRL).
Applications that used the "receive only" operation in order to recover immediately from bus off conditions need to implement a software workaround. The application needs to monitor the transmit-error counter (TEC). This can be supported by the CAN bus error interrupt (CxINT5) indicating that REC or TEC is incremented. Before the counter reaches the bus off value (TEC > 255) the application puts the CAN module into initialization status and restarts it. Since the TEC can increment by 8 for every bit sent on the CAN bus, the initialization has to be performed well ahead of a TEC reading of 255. The CAN error interrupt needs only to be enabled as long as the CAN node is in error passive state (TEC > 127).

No. 4	FCAN: Mode Transition (Specification change notice)

Details:

There are two scenarios that need to be considered separately. The first scenario named Re-Init describes the transition from normal operation mode to initialization mode of the FCAN. The second scenario (Stop mode scenario) describes the transition from Sleep mode to Stop mode of the FCAN.

Common to both scenarios is the effect that the interface between CPU and FCAN macro will stop to operate and thus even causes that the execution of any CPU instruction is prevented. The occurrence of this unexpected behavior requires that the bus traffic on all CAN bus systems coincidentally enters a certain state, a maximum access load of the host processor to the FCAN macro is present at the same point in time, and a certain configuration of the FCAN was chosen. The unexpected behavior can occur when the host processor executes the above mentioned mode transition and all above mentioned conditions are met at the same time.

(1.) RE-INIT Behavior
When the CPU requests initialization mode for a particular FCAN-channel, the state machine of the FCAN may not have enough clock cycles to execute all internal tasks under certain operational conditions causing the unexpected behavior.
The Table 1 supplies a survey of the clock budget, which the FCAN provides to finish all internal tasks at a particular baud rate (column 1000 kbps through 125 kbps) with respect to the operating frequency of the macro. The columns ’1 FCAN’, ’2 FCAN’ list the amount of clocks a certain configuration (number of active channels) demands in worst case depending on the number of active CAN channels. The rows ’TX’ and ’RX’ list the clock demand and budget with respect to the actual operational usage of all other CAN-channels (for V850/SF1: maximum 2 channels). These CAN-channels are processing a transmission or a reception of a message. Whenever the clock demand is lower than the provided clock budget, the unexpected behaviour does not apply. The grey colored areas indicate operating conditions where the unexpected behaviour is not applicable independently of any configuration.

Even those operating conditions not colored grey can be of no concern if the particular configuration requires less clocks the actual operational usage. I.e. a 2-channel FCAN normally requires 146 clocks (column ’2’, row ’Re-Init/RX’). At 16 MHZ macro clock all baud rates lower or equal to 250 kbps are not subject to suffer from the limitation when only one channel is used. Then column ’1’ applies with 73 clocks. For the row ’Re-Init/TX’ the demand is 46 clocks, which also meets the available clock budget of 64 clocks.

No. 4 FCAN: Mode Transition
(Specification change notice)

Table 1: Mode transition behavior without workaround (V850/SF1)							
Macro Clock [MHz]	TX/RX	FCAN Baud rate Clock budget (clocks available)				No of FCAN interfaces Clocks required	
16		1000 KBPS	500 KBPS	250 KBPS	125 KBPS	1 FCAN	2 FCAN
Re-Init	TX	16	32	64	128	46	104
	RX	32	64	128	256	73	146
Stop Mode	TX	48	96	192	384	46	104
	RX	64	128	256	512	63	146

Grey fields: Mode transition behavior does not apply for these ranges or lower baud rates independent of the configuration (number of active FCAN channels).

(2.) Stop Mode Behavior
Similar to the behavior at the mode transition from normal operating mode to initialization mode (Re-Init), the unexpected behavior can also occur when transferring a FCAN-channel from Sleep mode to Stop mode (continuous sleep mode without wake-up capability). However the FCAN provides a higher clock budget for this scenario that reduces the probability of the occurrence of the unexpected behavior. Table 1 lists the applicable amount of clocks in the row 'Stop Mode'. Again columns '1000 kbps' through '125 kbps' list the clocks that the FCAN provides until all internal tasks have to be finished (clock budget). The columns '1 FCAN' , '2 FCAN' list the amount of clocks a certain configuration needs in a worst case scenario (demand). The grey colored area indicates baud rates that can not cause the unexpected behavior independently of any configuration.

Even the areas not colored grey may not cause the unexpected behavior. Whenever the clock budget is higher than the demand for a particular configuration, the application will not be affected by the mode transition behavior.

Impact on Application:
Most applications do not re-initialize their FCAN macro once the communication system went online. Neither many applications use the Stop mode because the wake-up by CAN-bus activity is disabled then. However if an application uses a transition from online to initialization mode or from Sleep to Stop mode, the impact is severe as the host CPU can stop. Once the application has entered this state only a Reset will recover the system.

The unexpected behavior can be prevented by a software workaround with considerably low efforts.

No. 4 FCAN: Mode Transition
(Specification change notice)

Workaround:

There are two methods to prevent the unexpected behavior where the second method includes the first method.

(1.) TRQ-Clear Workaround
The first method eliminates the influence of transmitted messages by clearing all transmission requests for the FCAN-channel that shall be put to initialization state (Re-Init) or transferred to Stop mode. For this purpose the post processor clears all TRQ of the respective channel. Then it waits for a few bit times in order to detect if a transmission request was serviced by the FCAN just before the CPU cleared the respective bit in the FCAN message buffer area. When this potential transmission has finished successfully, the transition to initialisation or Stop mode can be issued without limitations.

Note that for the mode transition from Sleep to Stop mode this suggested procedure is typically already applied in your program as a standard algorithm. This workaround delivers safe operating conditions for baud rates up to 500 kbps at any configuration of a FCAN macro. Table 2 shows the remaining combination that can still cause the unexpected behavior.

Table 2:
Mode transition behavior when applying TRQ-Clear workaround

Macro Clock [MHz]	TX/RX	FCAN Baud rate Clock budget (clocks available)				No of FCAN interfaces Clocks required	
16		1000 KBPS	500 KBPS	250 KBPS	125 KBPS	1 FCAN	2 FCAN
Re-Init	TX	16	32	64	128	13	35
	RX	32	64	128	256	18	40
Stop Mode	TX	48	96	192	384	13	35
	RX	64	128	256	512	18	40

Grey fields: Mode transition behavior does not apply for these ranges or lower baud rates when TRQ-Clear workaround is applied independent of the configuration (number of active FCAN channels).

Note that at least one transmission request remains active when the ’bus off’ state was entered even if the host processor has cleared all transmission requests in the message buffer memory. In that case the application needs to wait until the FCAN-channel leaves ’bus off’ state and transmits the message pending in the CAN protocol core before resuming with the mode transition into initialization or Stop mode.

No. 4	FCAN: Mode Transition (Specification change notice)

(2.) Re-Initialization via Stop Mode
The second method eliminates the remaining constellation from the first method. As the reception of a message can not be predicted, the transition into initialization state can not be issued directly without suffering the mode transition behavior. To eliminate the remaining combination that can cause the unexpected behavior, the FCAN-channel needs to be transferred into Stop mode at first. Then this FCAN-channel can be put to initialization mode safely. With this countermeasure in addition to the TRQ-Clear workaround all potential scenarios that can cause the unexpected behavior are prevented.

No. 5	Conflict between writing to external memory and HLDRQ signal

Details
If a write operation (R/W signal = Lo) to the external memory and the acknowledgement of a bus hold request (HLDRQ) conflict at a specific timing, the R/W signal becomes Hi-Level (read) though the bus cicle is in the write state. As a consequence the write operation to an external device canot be performed normally if the above conflict occurs.
The behaviour applies only to flash devices of V850/SF1.

Workaround
There is no workaround. The behaviour does not apply to the mask version of V850/SF1A and to V850/SF1B (µPD70F3079BY, µPD70F3079BY(A)).

No. 6	Reading timer count register TMn of timers TM2 to TM6

Details
If the 16-bit timer count register TMn (n=2...6) is read out during timer operation, an unexpected additional count of the upper half of the timer count register may occur.

Workaround
Do not read the 16-bit timer count register TMn (n=2...6) during timer operation.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	August 2005	U14665EJ5V0UD00	V850/SF1 32-Bit Single-Chip Microcontroller Hardware (User's Manual including electrical specifications)
2	March 2001	U10243EJ7V0UM00	V850 32-Bit Microprocessor Core Architecture (User's Manual)

(D) Revision History

Item	Date published	Document No.	Comment
1	March 2004	TPS-HE-B-2151	First release in new format. Additional operating precaution No. 4.
2	June 2006	TPS-HE-B-2152	Added item No. 5.
3	December 2007	U18408EE3V0IF00	Added item No. 6.