NEC

Customer Notification

V850ES/SG2, V850ES/SJ2

32-bit Single-Chip Microcontrollers

Operating Precautions

μPD70F326xY,
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μPD70F328xY,
μPD70328xY

Document No. U18075EE6V0IF00
Date Published October 2006

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(A) Table of Operating Precautions

No.	Outline		V850ES/SG2 (Flash): μPD70F3261Y, μPD70F3263Y, μPD70F3281Y, μPD70F3283Y		
		Rev.			
		Rank[Note1]	K	E	P
1	Continuous write to WDTM2 register (Specification change notice)		✗	✗	✗
2	Rewriting ADC control register and external/timer trigger input during ADC operation (Specification change notice)		✗	✗	✗
3	AFCAN: Sleep Mode Wakeup[Note2] (Specification change notice)		✗	✗	✗
4	Stand-by Mode Release (Specification change notice)		✗	✗	✗

✓ :Not applicable

✗ : Applicable

Notes: 1. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

2. Applies only to device version containing a CAN interface (μPD70F328xY).

No.	Outline		V850ES/SG2 (Mask): μPD703260Y, μPD703261Y, μPD703262Y, μPD703263Y, μPD703280Y, μPD703281Y, μPD703282Y, μPD703283Y		
		Rev.			
		Rank[Note1]	K	E	
1	Continuous write to WDTM2 register (Specification change notice)		✗	✗	
2	Rewriting ADC control register and external/timer trigger input during ADC operation (Specification change notice)		✗	✗	
3	AFCAN: Sleep Mode Wakeup[Note2] (Specification change notice)		✗	✗	
4	Stand-by Mode Release (Specification change notice)		✗	✗	

✓ : Not applicable

✗ : Applicable

Notes: 1. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

2. Applies only to device version containing a CAN interface (μPD70F328xY).

No.	Outline		V850ES/SJ2 (Flash) μPD70F3264Y, μPD70F3266Y, μPD70F3284Y, μPD70F3286Y, μPD70F3288Y		
		Rev.			
		Rank[Note1]	K	E	
1	Continuous write to WDTM2 register (Specification change notice)		✗	✗	
2	Rewriting ADC control register and external/timer trigger input during ADC operation (Specification change notice)		✗	✗	
3	AFCAN: Sleep Mode Wakeup[Note2] (Specification change notice)		✗	✗	
4	Stand-by Mode Release (Specification change notice)		✗	✗	

✓ :Not applicable

✗ : Applicable

Notes: 1. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

2. Applies only to device version containing a CAN interface (μPD70F328xY).

No.	Outline		V850ES/SJ2 (Mask) μPD703264Y, μPD703265Y, μPD703266Y, μPD703284Y, μPD703285Y, μPD703286Y, μPD703287Y, μPD703288Y		
		Rev.			
		Rank[Note1]	K		
1	Continuous write to WDTM2 register (Specification change notice)		✗		
2	Rewriting ADC control register and external/timer trigger input during ADC operation (Specification change notice)		✗		
3	AFCAN: Sleep Mode Wakeup[Note2] (Specification change notice)		✗		
4	Stand-by Mode Release (Specification change notice)		✗		

✓ :Not applicable

✗ : Applicable

Notes: 1. The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

2. Applies only to device version containing a CAN interface (μPD70F328xY).

(B) Description of Operating Precautions

No. 1	Continuous write to WDTM2 register (Specification change notice)
	Details When a write access is made to the WDTM2 register twice or more after a reset, the CPU judges that the program is inadvertently looping and forcibly generates an overflow signal. However, an overflow signal cannot be generated during a continuous write to WDTM2. The overflow signal is generated after the continuous write is suspended. *Workaround* Do not write to the WDTM2 register three times or more after a reset release, until the next reset is applied.

No. 2	Rewriting ADC control register and external/timer trigger input during ADC operation (Specification change notice)

Details

(1) After the A/D conversion operation is enabled, if a reconversion trigger input[Note 2] conflicts with the timing at which a stabilization time[Note 1] to be inserted for the A/D converter setup ends, the stabilization time is reinserted for 64 clocks. Furthermore, if the end timing of the reinserted stabilization time conflicts again with another reconversion trigger input[Note 2], the stabilization time will be inserted again. Although the stabilization time is reinserted, the conversion operation ends normally.

(2) In normal conversion mode, if a reconversion trigger[Note 2] input conflicts with the timing at which the conversion of a one-shot select conversion operation or external/timer trigger select conversion operation ends (prior to wait time)[Note 1], then the conversion operation that should be restarted from the beginning is not performed, and the conversion operation is stopped while A/D conversion operation remains enabled (ADA0CE = 1) and A/D conversion has been stopped (ADA0M0.ADA0EF = 0). (No A/D conversion end interrupts occur, and the conversion result is not stored).
To continue A/D conversion following this state in one-shot select conversion operation, the A/D conversion operation must be once stopped (ADA0CE = 1 -> 0), and then the conversion operation must be enabled (ADA0CE = 0 -> 1) again. When the external/timer trigger operation is performed, when the selected trigger signal is input and the wait time and stabilization time have elapsed, the conversion operation then starts.

(3) In normal conversion mode, the A/D conversion end timing (prior to wait time)[Note 1] conflicts with a reconversion trigger[Note 2] input, the conversion operation that should be restarted from the beginning is not performed, and the conversion operation is stopped while A/D conversion operation remains enabled (ADA0CE = 1) and A/D conversion is operating (ADA0M0.ADA0EF = 1). (No A/D conversion end interrupts occur, and the conversion result is not stored). If a reconversion trigger[Note 2] occurs in this state, the conversion operation starts again.

(4) In high-speed conversion mode and software conversion start trigger mode, if the conversion end timing[Note 1] of one-shot select or one-shot scan conversion operation conflicts with a reconversion trigger[Note 2] input, the conversion operation that should be restarted from the beginning is not performed, and the conversion operation is stopped while A/D conversion operation remains enabled (ADA0CE = 1) and the A/D conversion has been stopped (ADA0M0.ADA0EF = 0). (No A/D conversion end interrupts occur, and the conversion result is not stored). In this state, if “1” is overwritten to the ADA0CE bit, or if A/D conversion operation is stopped (ADA0CE = 1 -> 0) and then conversion operation is enabled again (ADA0CE = 0 -> 1), the the conversion operation starts again.

Notes 1. For details on each timing during a conversion operation, refer to the user’s manual for each product.
2. There are two types of reconversion triggers:
(a) Write to an A/D conversion register (ADA0M0, ADA0M2, ADA0S, ADA0PFM, or ADA0PFT).
(b) External trigger (detection of the ADTRG pin’s edge) or timer trigger (TMP2 compare match interrupt request signal)
* If a reconversion trigger occurs during A/D conversion operation, then the conversion is suspended and restarted from the beginning.

No. 2	Rewriting ADC control register and external/timer trigger input during ADC operation (Specification change notice)

Behaviour corresponding to ADC operation mode

Conversion Trigger	Conversion Mode	High-Speed Conversion Mode (without intermittent operation)				Normal Conversion Mode (with intermittent operation)			
		(1)Note5	(2)Note5	(3)Note5	(4)Note5	(1)Note5	(2)Note5	(3)Note5	(4)Note5
Software trigger	Continuous select	✗	-	-	✓	✗	✓	✗	-
	Continuous scan	✗	-	-	✓	✗	✓	✗	-
	One-shot select	✗	-	-	✗	✗	✗Note4	✗Note4	-
	One-shot scan	✗	-	-	✗	✗	✓Note3	✗	-
External/ timer trigger	Select	✗	-	-	✓	✗	✗Note4	✗Note4	-
	Scan	✗	-	-	✓	✗	✓Note3	✗	-

✓ :Not applicable
✗ : Applicable
- : Not relevant

Notes 3. This behaviour applies if ADA0S = 00H in scan mode.
4. Either (2) or (3) occurs depending on the internal status when the conversion end and reconversion trigger input conflict.
5. Numbering refers to the above mentioned descriptions.

Workaround

1. When the external or timer trigger is selected, set high-speed conversion mode, and do not input a trigger during the stabilization time that is inserted only once after the A/D conversion operation is enabled (ADA0CE bit = 0 -> 1).

2. Before writing to an A/D control register**Note** in normal conversion operation mode, or during oneshot conversion operation in high-speed conversion mode, stop the A/D conversion operation (ADA0M0.ADA0CE = 0), and then enable the A/D conversion operation (ADA0M0.ADA0CE = 1).

Note A/D control register: ADA0M0, ADA0M2, ADA0S, ADA0PFT, and ADA0PFM registers.

No. 3	AFCAN: Sleep Mode Wakeup (Specification change notice)

Details:

1. Exclusions

This Operating Precaution is ***only applicable*** to applications, which are fulfilling at least one of the following three conditions:

- SLEEP Mode of AFCAN is used ***and*** the possibility to wake up AFCAN by CAN-Bus events is given (see Remarks: 1.)
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see Remarks: 2.) ***and***
  - after waking up from SLEEP mode of the AFCAN macro, the application software does ***not*** wait until the SLEEP mode is released by polling the CnCTRL (PSMODE) register, before continuing operation with the AFCAN macro (see Remarks: 3.) ***and***
  - the CPU can reach instructions, where AFCAN registers are accessed while the AFCAN macro is still in SLEEP mode, due to the missing waiting condition.
- During SLEEP mode of the AFCAN macro, a CAN-Bus wakeup condition occurs, while the AFCAN macro is supplied with clock (see Remarks: 2.) ***and***
  - after waking up from SLEEP mode of the AFCAN macro, the CAN Bus Transceiver generates a ***long-lasting or permanent dominant level*** to the CRXD input of the AFCAN macro, instead of the propagated CAN-Bus level.

Remarks: 1. If the CAN-Bus Transceiver does not propagate the CAN-Bus signal, while the AFCAN macro is in SLEEP mode, and also does not forward a wakeup signal to CRXD, ***this Operating Precaution is not applicable.***

2. The clock supply to the AFCAN macro can be stopped, depending on the features of the device, and the system design of the application. If the clock supply to the AFCAN macro is stopped, while a wakeup condition occurs, ***this Operating Precaution is not applicable***.

3. The maximum waiting time for this loop can be up to 10 bits of the CAN-Bus Baudrate.
Waiting while retrying to clear CnINTS (Bit 5) can be used alternatively.

All other applications are not affected by this Operating Precaution.

2. Description

When the AFCAN macro is set into SLEEP mode, it can be woken up by CAN bus activity.

This waking up is asynchronous to the operation of the macro and the CPU. By configuration setting, a WAKEUP interrupt can be generated by the AFCAN macro on the wakeup event.

While the interrupt is generated asynchronously, the AFCAN macro may need another dominant edge on the CAN bus, or software clearing of the SLEEP mode, in order to restart its synchronous operation.

During the time, after the interrupt already has been indicated, and before the CAN macro has restarted its synchronous operation, the registers of the AFCAN macro will not operate, because the AFCAN macro still remains in SLEEP mode. This time we will refer to as “wakeup dead time” in the following context.

No. 3	AFCAN: Sleep Mode Wakeup (Specification change notice)

To resolve from the wakeup dead time, software and/or hardware measures are required.

Note: However, this Precaution does *not apply to all* applications. Only dedicated applications are affected (see above).

3. Application Dependency

3.1 Overview

The following flowchart illustrates, how and whether additional measures have to be taken in software, to avoid the *wakeup dead time*.

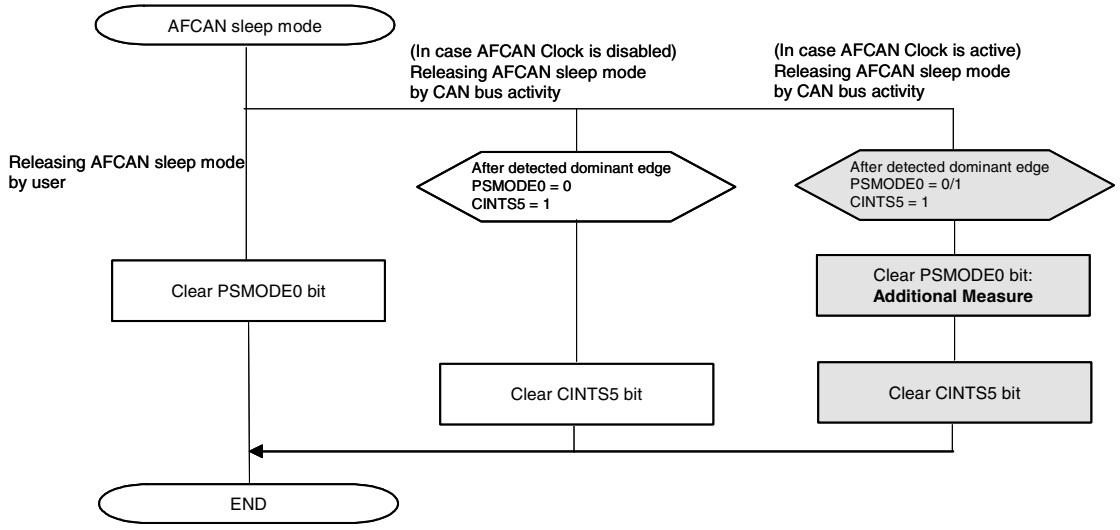


Figure 3-1: Additional Measures in case AFCAN clock is active when waking up

3.2 Not affected Applications

3.2.1 Applications not using SLEEP mode

If SLEEP mode is not used, ***this Operating Precaution is not applicable.***

3.2.2 Applications waking up from SLEEP mode by User Request only

If there is no condition, when SLEEP mode can be left by CAN-Bus activity, but only on User Request (by clearing the PSMODE flag by software), ***this Operating Precaution is not applicable.***

No. 3	AFCAN: Sleep Mode Wakeup (Specification change notice)

3.2.3 Applications using a CPU Power Save Mode

If the clock to the AFCAN macro is disabled, while it is woken up from SLEEP mode, ***this Operating Precaution is not applicable.***

This means, if the user selects a power save mode of the target device, which switches off the clock of the AFCAN macro, immediately after it had been set into SLEEP mode, like the *"CPU STOP"* mode, the precaution needs not to be considered.

This is associated with the software improvement hints below.

3.3 Affected Applications

3.3.1 Applications not waiting until SLEEP mode is left

If Bus Transceivers are used in conjunction with AFCAN, which will *propagate the CAN-Bus signal* to AFCAN permanently (not switched off or not in power saving modes), or, if Bus Transceivers are used in conjunction with AFCAN, which will *propagate the unmodified CAN-Bus signal* when waking up from a power save mode, the *wakeup dead time* lasts from the first recessive-to-dominant edge of the CAN-Bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN-Bus signal.

The worst case (maximum length) of the *wakeup dead time*, is given by the CAN bus speed and the rule of the CAN bus about the frequency of recessive-to-dominant edges. Given by the stuffing rule, at least every 10 bits, a recessive-to-dominant edge must occur.

If during the *wakeup dead time,* the CPU waits until the SLEEP mode is indicated to be cleared (either by polling the PSMODE flag, or by retrying to clear CnINTS[5]), ***this Operating Precaution is not applicable. In this case, the Improvement Hint according to 4.2.2 is followed implicitly.***

If during the *wakeup dead time,* the CPU does not perform any access to the AFCAN macro in any case, ***this Operating Precaution is not applicable.***

3.3.2 Applications using Bus Transceivers generating long-lasting dominant CAN-Bus Signals

If Bus Transceivers are used in conjunction with AFCAN, which *generate a permanent or long-lasting dominant level* when waking up from a power save mode, the Operating Precaution must be considered in any case.

In this case, the *wakeup dead time* lasts from the first recessive-to-dominant edge of the CAN-Bus signal, which generates the wake-up, until the next recessive-to-dominant edge of the CAN-Bus signal, depending on the behaviour of the CAN-Bus Transceiver.

If no further dominant edge on the CAN bus occurs (in case of some CAN Transceivers, which only provide one single edge on waking up), the time until SLEEP mode is left may become endless. Therefore, the waking up procedure of AFCAN regarding software, must be adjusted according to 4.1.1.

No. 3	AFCAN: Sleep Mode Wakeup (Specification change notice)

4. Software Improvement Hints

4.1 Recommended WAKEUP Handling by Software

4.1.1 Clearing the SLEEP Mode by Software

Within the WAKEUP interrupt routine, before accessing any other register or area of AFCAN, the SLEEP mode can be canceled by software, followed by a clearance of the WAKEUP interrupt flag.

Doing so, the AFCAN macro will start its synchronous operation right after these accesses.

In the following C-code example, replace the objects in “<>” brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User’s Manual.

```
WAKEUP INTERRUPT VECTOR -->
                          <CnCTRL_PSMODE> = 0;   /* Clear SLEEP Mode */
                          <CnINTS_CINTS5> = 1;   /* Clear INTS5      */
                          ...
                        /* following other parts of interrupt routine */
                          ...
```

Note: Clearing INTS5 is required to get another WAKEUP interrupt anyway, by specification.

4.2 Other WAKEUP Handling Hints

4.2.1 Switching off the Clock Supply to AFCAN, while in SLEEP Mode

If the clock supply to the AFCAN macro is stopped, while it is in SLEEP mode, the synchronisation of the WAKEUP works without any restriction. To achieve this, the documentation of clock controlling unit of the target device should be consulted. Usually this is performed by setting the STOP mode of the CPU of the target device.

However, the user has to consider, that there must not be any WAKEUP condition (dominant level on the CAN-Bus), while the software is executing between setting SLEEP mode and stopping the AFCAN clock.

4.2.2 Using a Waiting Loop within the WAKEUP interrupt routine

Within the WAKEUP interrupt routine, create a waiting loop, which tests the capability of clearing the WAKEUP interrupt flag within AFCAN, by checking the actual power save mode.

In the following C-code example, replace the objects in “<>” brackets by the hardware locations within your implementation. Use the appropriate access types, as described in the User’s Manual.

No. 3	AFCAN: Sleep Mode Wakeup (Specification change notice)

```
do
{
    AFCAN_SleepStatus = <CnCTRL_PSMODE>

    if( AFCAN_SleepStatus != 0 )
    {
        /* macro is still in SLEEP mode (waiting for latency time) */

        <CnINTS_CINTS5> = 1;    /* repeated trying to clear CINTS5 */
    }

} while( AFCAN_SleepStatus != 0 );
```

This improvement hint *cannot be applied*, if a CAN-Bus-Transceiver is attached to AFCAN, which generates a *permanent or long-lasting dominant level to the CRXD* AFCAN receive input, if a wakeup condition occurs. Missing another dominant edge on the bus, the synchronisation will not happen, and the loop could run endlessly.

4.2.3 Using INIT Mode instead of SLEEP Mode

In this case, the waking up by CAN-Bus activity must be performed via another free Pin I/O Interrupt. Probably, the RX signal of CAN must be distributed on the CRXD of the AFCAN macro, and another Pin I/O in parallel.

Using this Pin I/O Interrupt, the AFCAN macro can be put back into the previous Operation mode.

This implementation will *not* use the SLEEP mode of AFCAN at all, and use the INIT mode instead.

No. 4	Stand-by Mode Release (Specification change notice)

Description:

If a stand-by mode request and a wake-up event coincide with the same timing, the µC may enter the power save mode in a way that the power save mode can be released by Reset (external or internal) only.
This happens only if the stand-by mode request and the wake-up event occur within a timing window of 0.46 nsec width.

The term “stand-by mode” of the above description refers to all stand-by modes which are selected by the Power Save Control Register (PSC).
The term “wake-up event“ of the above description refers to any event which is configured to release the microcontroller from a stand-by mode. This can be any unmaskable or unmasked maskable interrupt (internal or external) except reset.

Affected stand-by modes are:
- Idle1 Mode,
- Idle2 Mode,
- Sub-Idle Mode and
- Stop Mode

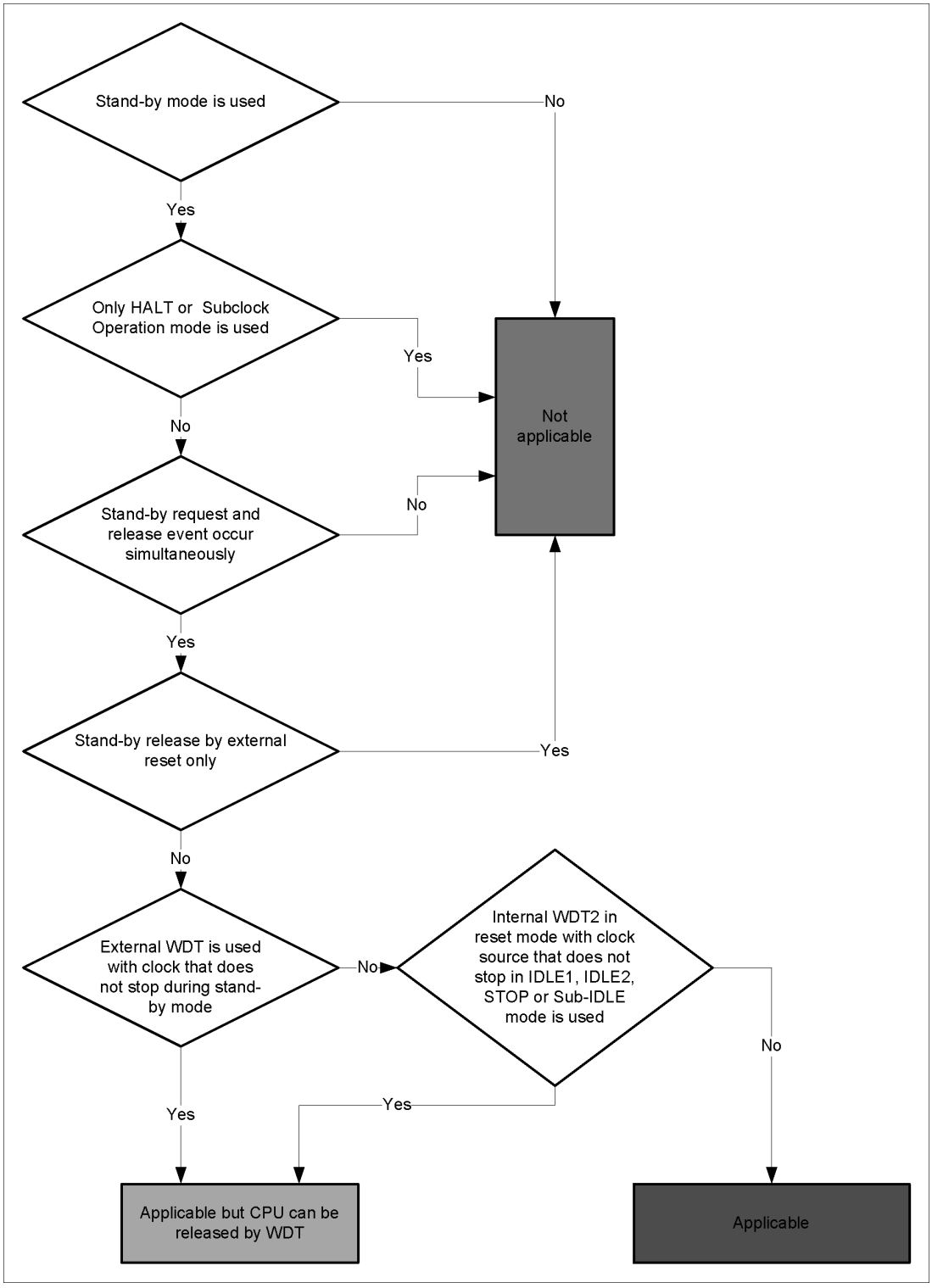
Not affected stand-by mode:
- Halt Mode

Please see the flowchart on the following page.

No. 4	Stand-by Mode Release (Specification change notice)

Description (continued):

Please see the following flowchart to check if the described behaviour might be relevant for a particular application:



(C) Valid Specification

Item	Date pulished	Document No.	Document Title
1	June 2005	U16603EJ4V0UD00	V850ES/SJ2 Hardware (User's Manual)
2	July 2005	U16541EJ4V0UD00	V850ES/SG2 Hardware (User's Manual)
3	April 2004	U15943EJ3V0UD00	V850ES Architecture (User's Manual)

(D) Revision History

Item	Date pulished	Document No.	Comment
1	August 2006	U18075EE5V0IF00	New List
2	October 2006	U18075EE6V0IF00	Added item 4